**Signals**

|  |  |  |  |
| --- | --- | --- | --- |
| **Short Name** | **Full Name** | **Direction** | **Width (bits)** |
| CLK | CLOCK | IN | 1 |
| NRST | NOT\_RESET | IN | 1 |
| D | DATA | IN | 8 |
| DS | DATA\_SET | IN | 1 |
| SCLK | STANDART\_CLK | OUT | 1 |
| MOSI | MASTER\_ OUTPUT | OUT | 1 |
| TI | TRANSMISSION\_INDICATION | OUT | 1 |

DATA – 8-bit wire for input data.

DATA\_STORE – signal to update the data in the buffer.

MASTER\_ OUTPUT - sequentially outputs bits from the buffer starting from the most significant bit.

TRANSMISSION\_INDICATION – indicates that the data is still being transmitted.

*Take Xilinx's IP core documentation as a basis.*