## EXPERIMENT - 08

## DIFFERENTIAL AMPLIFIER

**Aim: -** To design, simulate, and implement the schematic and physical layout of a MOSFET differential amplifier using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

**Software & Technology Used:** CADENCE VIRTUOSO, 180nm

**Theory:** The differential amplifier is a voltage subtractor circuit which produces an output voltage proportional to the voltage difference of two input signals applied to the inputs of the inverting and non-inverting terminals of an operational amplifier. This means that a differential amplifier naturally eliminates noise or interference that is present in both input signals.

For a symmetric MOS differential pair biased with tail current $I_{tail}$and small-signal transconductance $g_m$per input transistor, with an effective output resistance $R_o$at each output node: Differential output gain

$$A_d = \frac{v_{out,p} - v_{out,m}}{v_{id}}$$

For a basic differential pair:

$$A_d \approx g_m R_o$$

**Procedure**

Follow the techniques, Create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

**Schematic Diagram:**

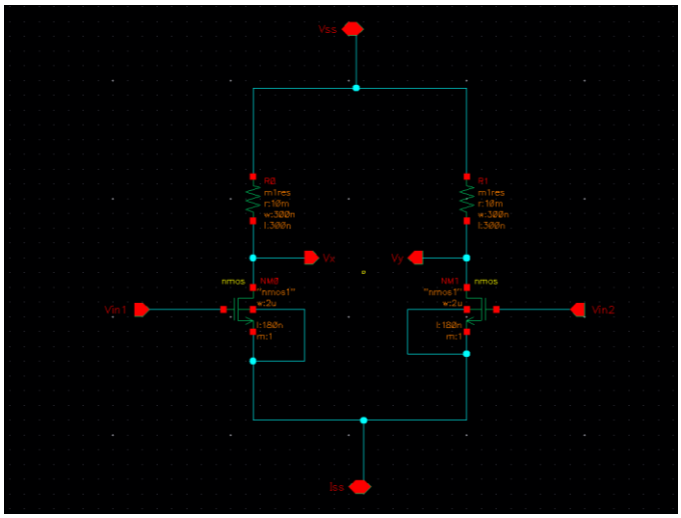



Fig: Schematic of Differential Amplifier

**Functional Stimulation:**

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of differential amplifier, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

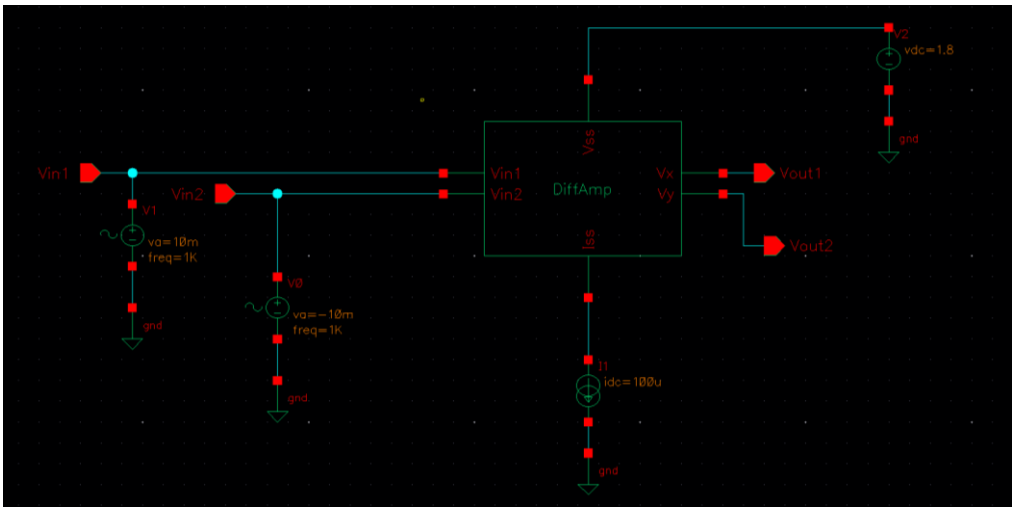



Fig: Test bench schematic of Differential Amplifier

**Properties of vdc, vsin and idc:**

| Library Name | Cell Name | Properties |
|---|---|---|
| AnalogLib | vdc | Vdd: DC voltage = 1.8V |
| AnalogLib | vsin | AC = 1V<br>Amplitude = 10mV<br>Frequency = 1KHz |
| AnalogLib | vsin | AC = 1V<br>AC phase = 180<br>Amplitude = 10mV<br>Frequency = 1KHz |
| AnalogLib | idc | DC current = 100u A |

**Simulation:**

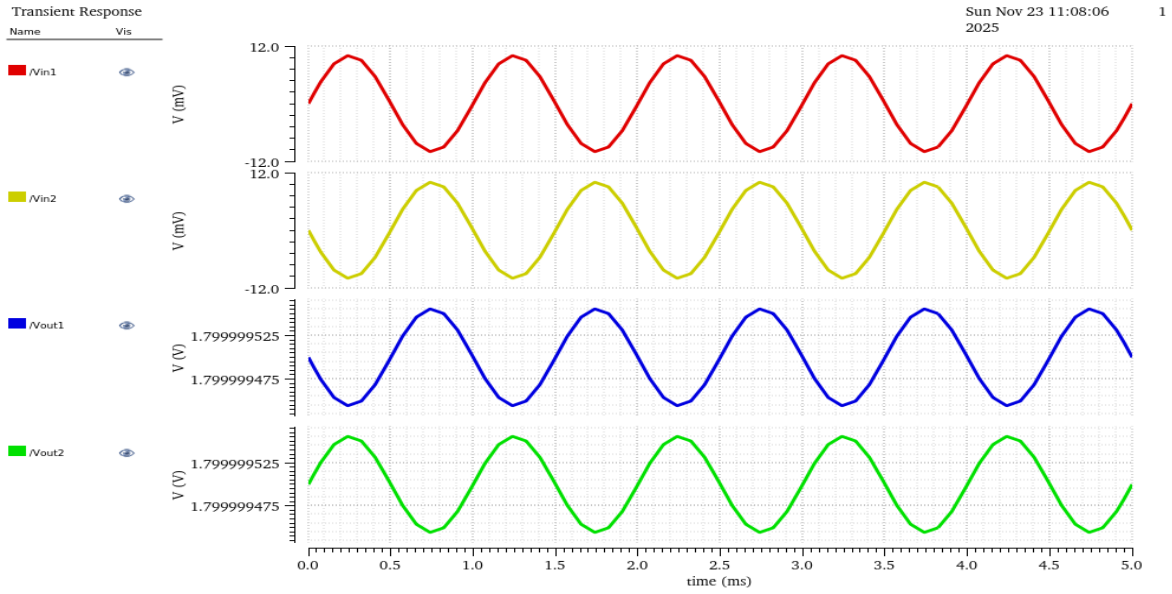
Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

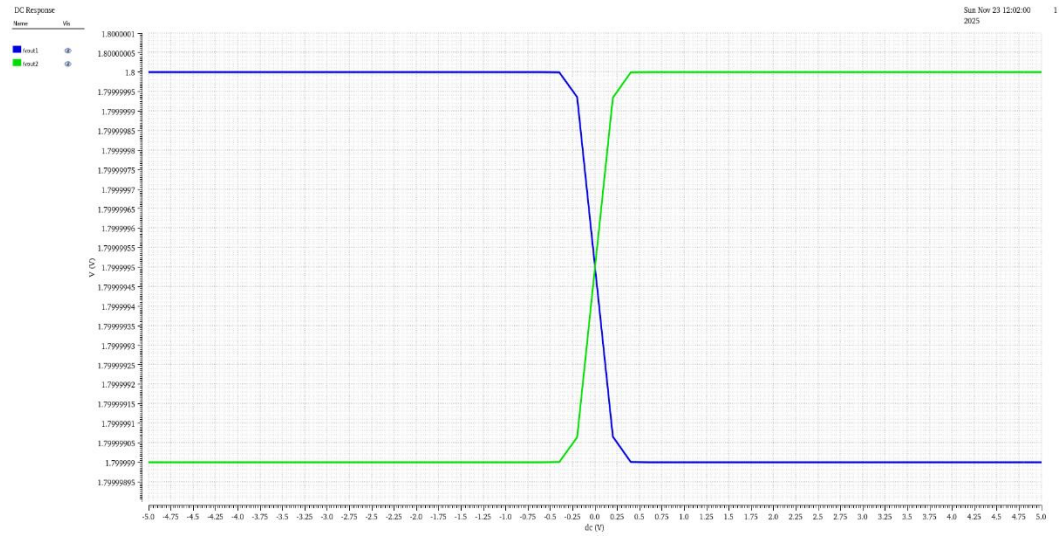
To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "-5" and "Stop" value as "5", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "10" and "Stop" value as "10G", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".

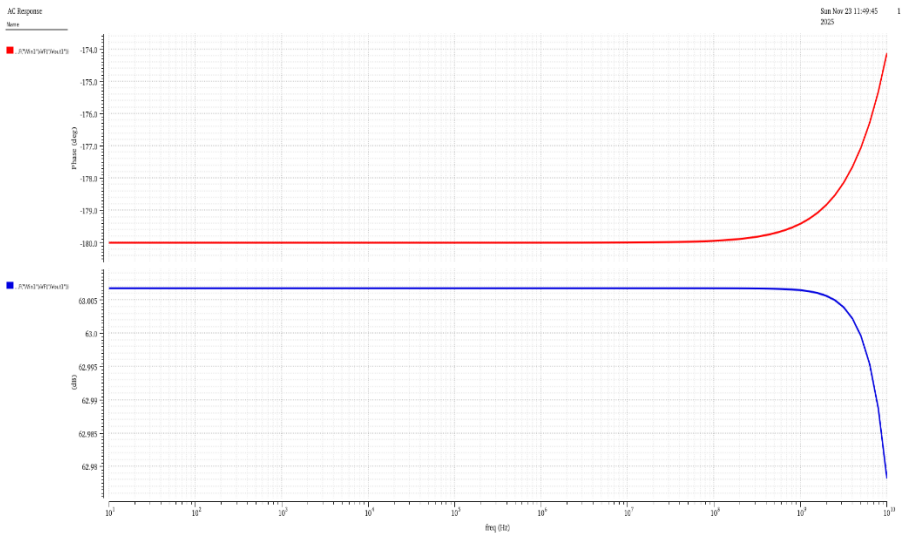
**Transient Response:**




**DC Response:**



**AC Response:**




**Layout:**

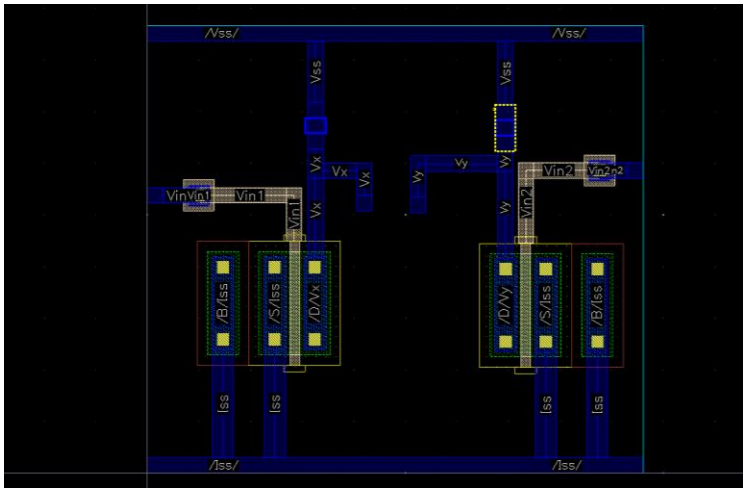



Fig: Differential amplifier layout

**DRC:**

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

**LVS:**

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

**QRC:**

To extract the Parasitics, select “Assura → Quantus”, select “Technology →gpdk180”, “Output → Extracted View” from the “Setup” option, select “Extraction Type → RC” and “Ref Node → VSS” from the “Extraction”, Disable HRCX and click on “OK”.

The result can be checked from the Library Manager.

**Conclusion:**

The differential amplifier was successfully designed and implemented using Cadence Virtuoso. Pre-layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.