ECE 5002 – ANALOG VLSI DESIGN

VIT-AP UNIVERSITY

Fall Semester 2025-26

M. Tech VLSI DESIGN

School of Electronics Engineering Lab report

Submitted to

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EXPERIMENT – 01

NMOS AND PMOS

Aim: To design, simulate, and implement the schematic and physical layout of MOSFETs nMOS and pMOS using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology used: CADENCE VIRTUOSO, 180nm

Theory: An **nMOS (n-channel MOSFET)** uses electrons as majority carriers. When a positive gate voltage is applied relative to the source, an electron inversion layer forms beneath the oxide, creating a conductive channel between drain and source. nMOS devices offer higher mobility, faster switching, and lower on-resistance, making them widely used in digital logic and high-speed circuits.

A **pMOS (p-channel MOSFET)** uses holes as majority carriers. When a negative gate voltage is applied relative to the source, a hole inversion layer forms, allowing current to flow from source to drain. pMOS devices typically have lower mobility but are essential in forming CMOS technology, where nMOS and pMOS pairs provide low static power, high noise margins, and full logic swing.

Procedure:

Create a New Library using the option File ⟶ New ⟶ Library", create a New Cell View upon selecting the newly created library using the option "File ⟶ New Cell View" and instantiate the required devices using the "Create ⟶ Instance" option.

Schematic Diagram:

nMOS:

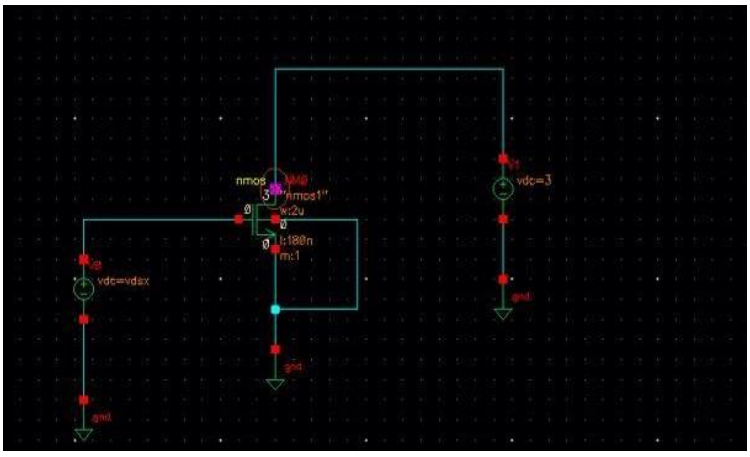


Fig: Schematic of nmos

pMOS:

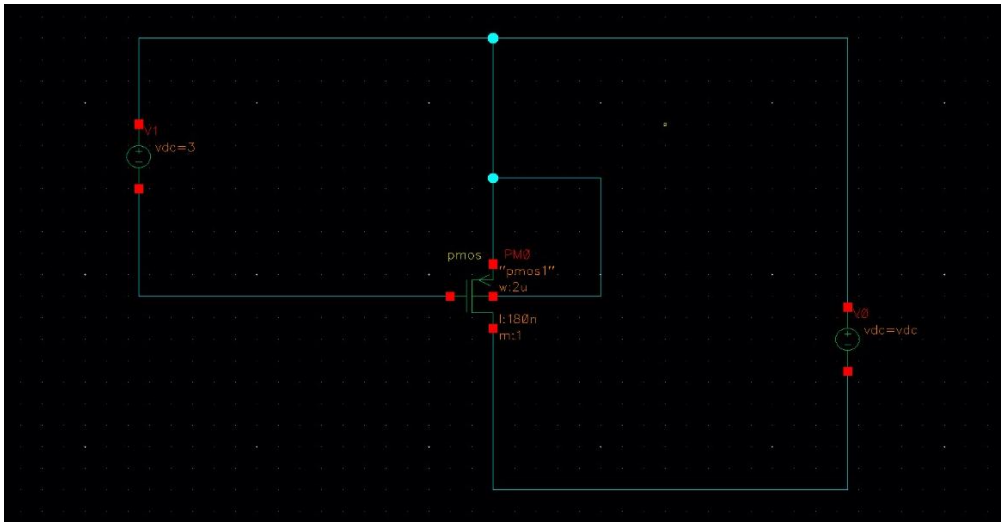


Fig: Schematic of pmos

Analysis: -

1. Transfer Characteristics (ID vs VGS)

Objective: Observe how ID changes with VGS (VDS fixed).

Steps:

1. Set VDS = 1.8 V (constant).
2. Open ADE_L → Analysis → DC.
3. Select Sweep Variable = VGS (e.g., 0 V to 1.8 V).
4. Go to Outputs → Select on Schematic → choose ID.
5. Run the simulation to get ID vs VGS plot.
6. From the graph, note:
    - Threshold Voltage (VTH)
    - Current rising region (saturation region)

2. Output Characteristics (ID vs VDS)

Objective: Observe how ID changes with VDS for different VGS.

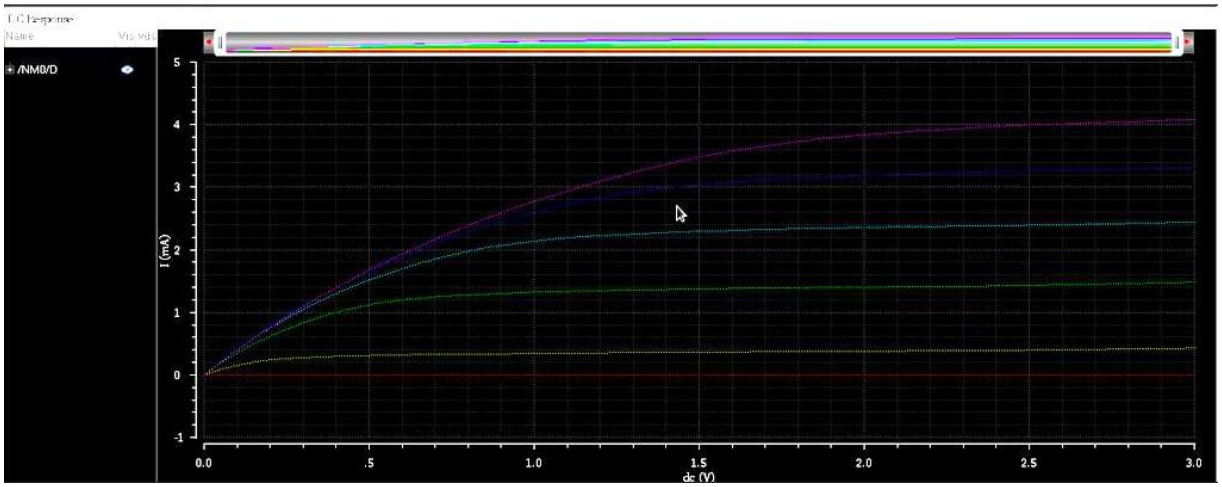
Steps:

1. Set VGS = constant values (e.g., 0.9 V, 1.2 V, 1.5 V).
2. Open ADE_L → Analysis → DC.
3. Select Sweep Variable = VDS (e.g., 0–1.8 V).

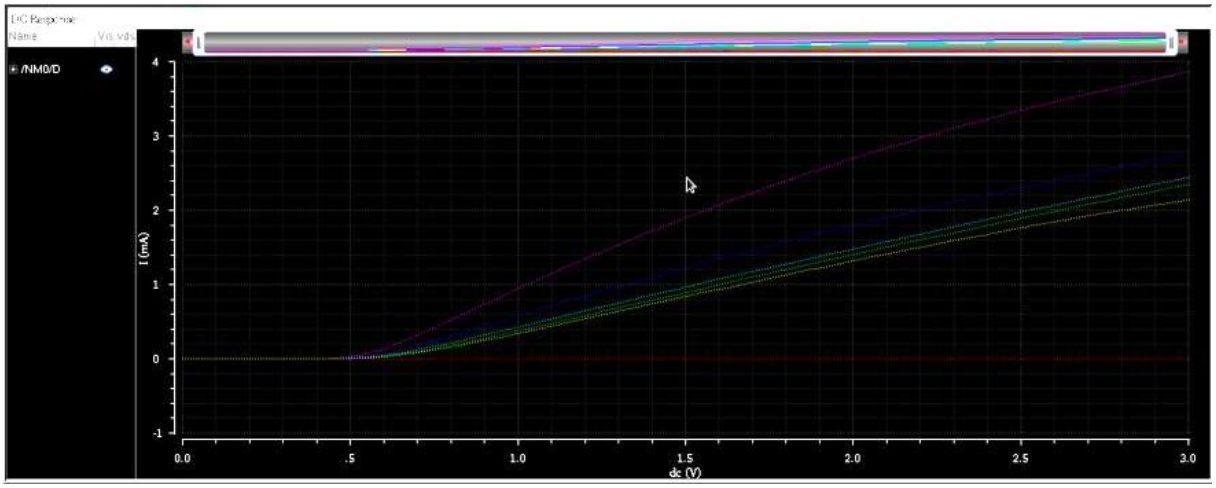
4. Go to Outputs → Select on Schematic → choose ID.
5. Run the simulation to get ID vs VDS graph.
6. Observe:
    - Linear region (small VDS)
    - Saturation region (VDS > VGS − VTH)

<u>Graphs and Observations</u>:

nMOS:

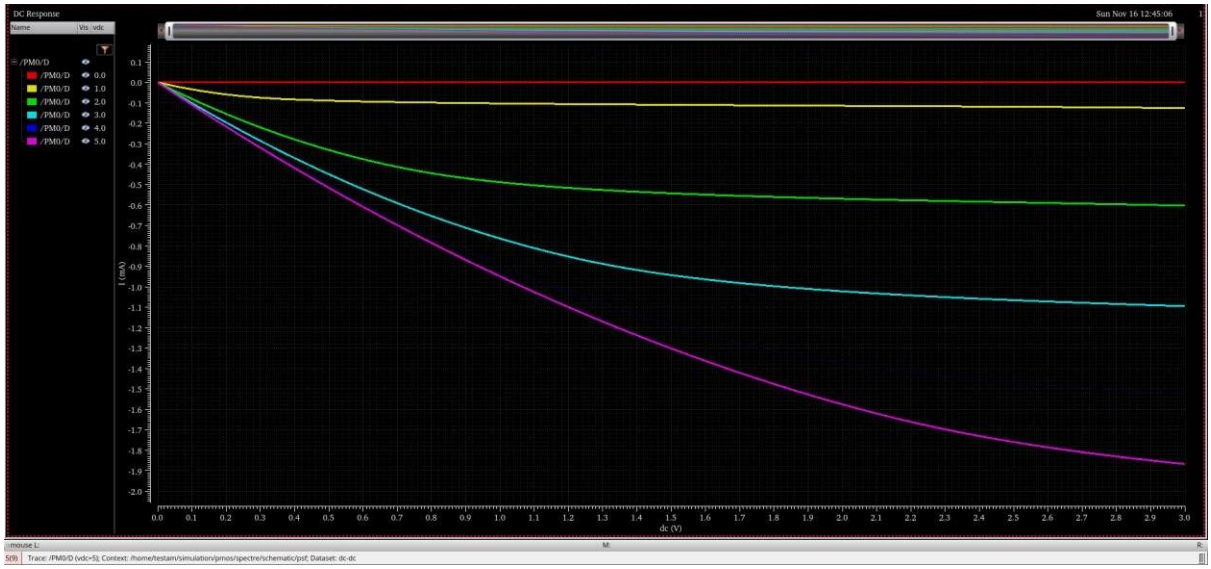


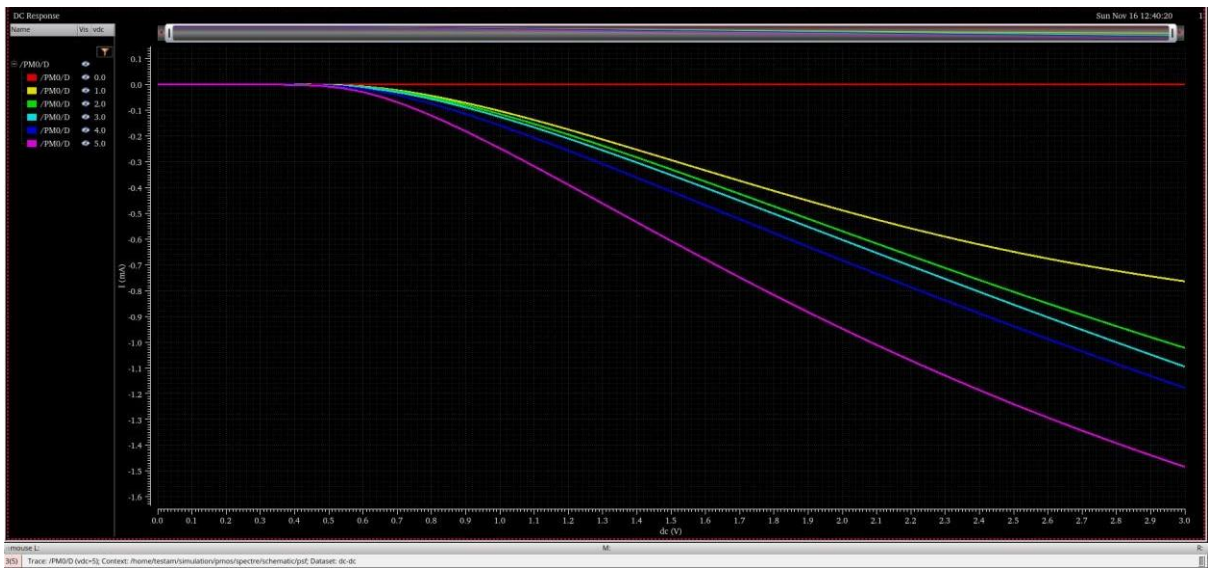
ID vs VGS (Transfer): current ≈ 0 until VGS ≈ VTH; beyond VTH, ID rises (nearly quadratic in ideal model) — use intercept to estimate VTH.



- In the **ID vs VDS** graph, observe the **linear region** and **saturation region** of the NMOS transistor.
- The **ID vs VGS** curve shows the **threshold voltage (VTH)** where conduction starts.
- Drain current increases with higher VGS due to stronger channel formation.

pMOS:





Layout:

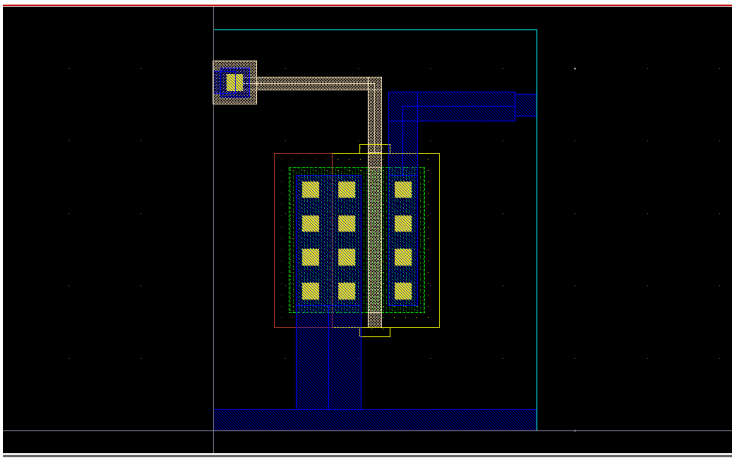


Fig: nmos Layout

Outcome:

- The **Transfer** and **Drain** characteristics of NMOS were successfully simulated using **Cadence Virtuoso**.
- The experiment demonstrates:
  - Relationship between **ID**, **VGS**, and **VDS**.
  - **Saturation** and **Ohmic regions** of NMOS operation.
  - Extraction of **Threshold Voltage (VTH)** from the ID-VGS curve.

EXPERIMENT – 02

COMMON SOURCE WITH RESISTIVE LOAD

Aim: To design, simulate, and implement the schematic and physical layout of MOSFET Common Source with Resistive Load using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules

Software & Technology used: CADENCE VIRTUOSO, 180nm

Theory: A Common Source (CS) amplifier is one of the most widely used MOSFET amplifier configurations because it provides voltage amplification with phase inversion. In this configuration, the source terminal is common to both input and output, the input is applied at the gate, and the output is taken from the drain. A resistor (RD) is used as the load, converting the drain current variations into voltage variations.

The MOSFET is biased such that it operates in the **saturation region**, where it behaves like a voltage-controlled current source.

- Saturation condition:

$$V_{DS} \geq V_{GS} - V_{th}$$

- Drain current (approx.):

$$I_D = \frac{1}{2} k_n (V_{GS} - V_{th})^2$$

Procedure:

Follow the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic:

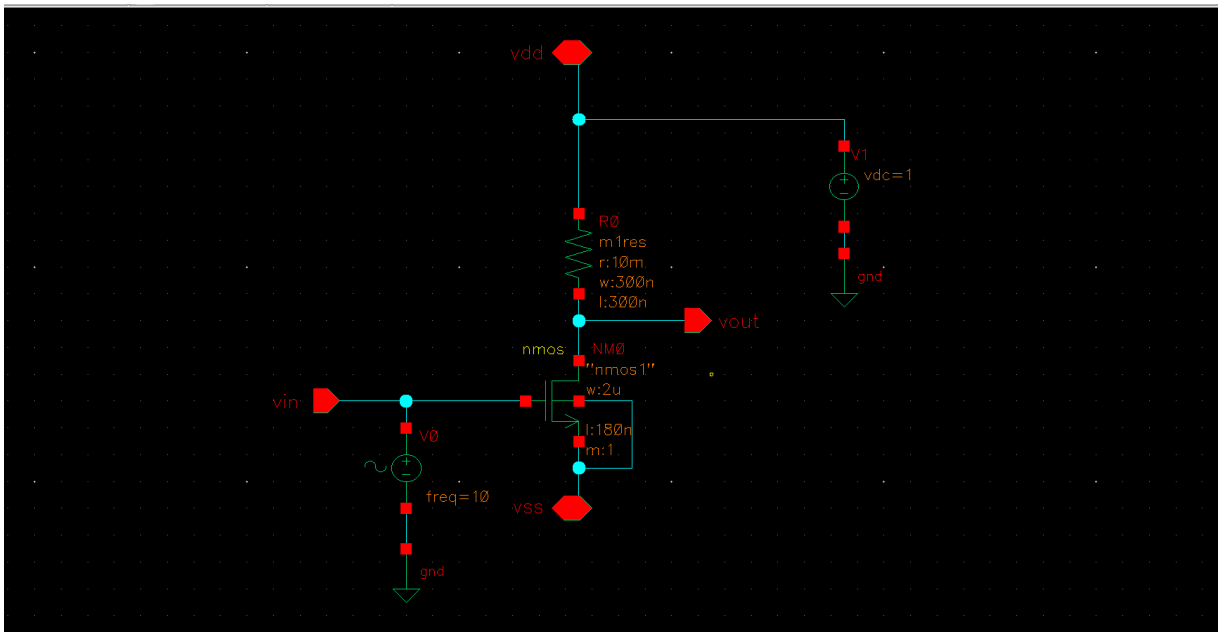


Fig: Schematic of Common Source with Resistive Load

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Common drain, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

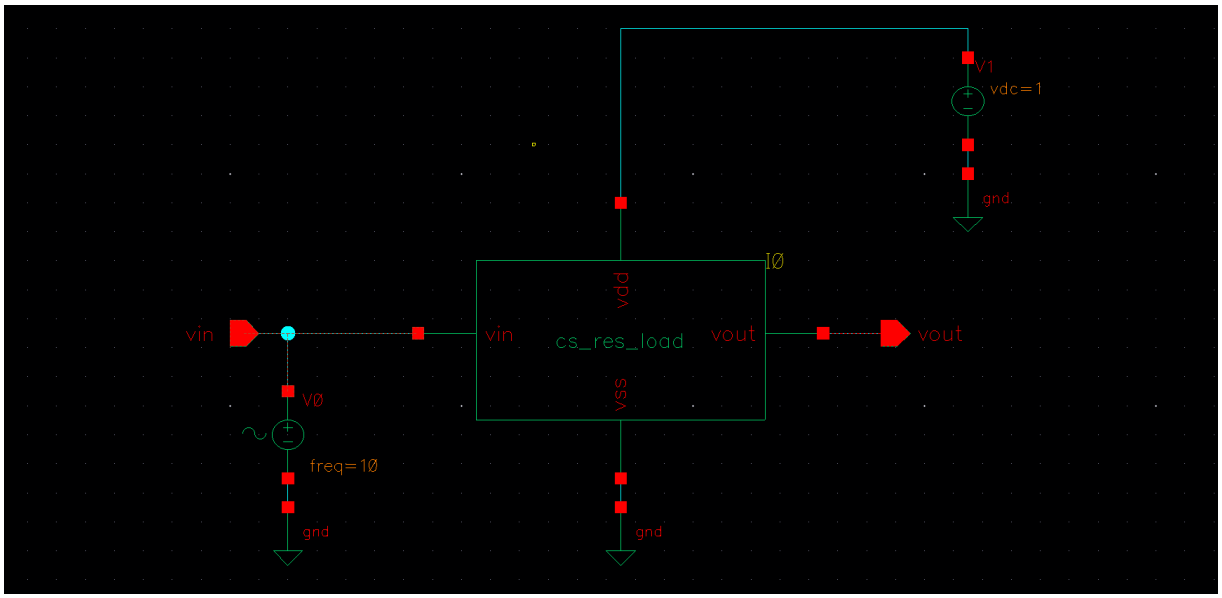


Fig: Test bench Schematic of Common Source with Resistive Load

Properties of vdc and vsin:

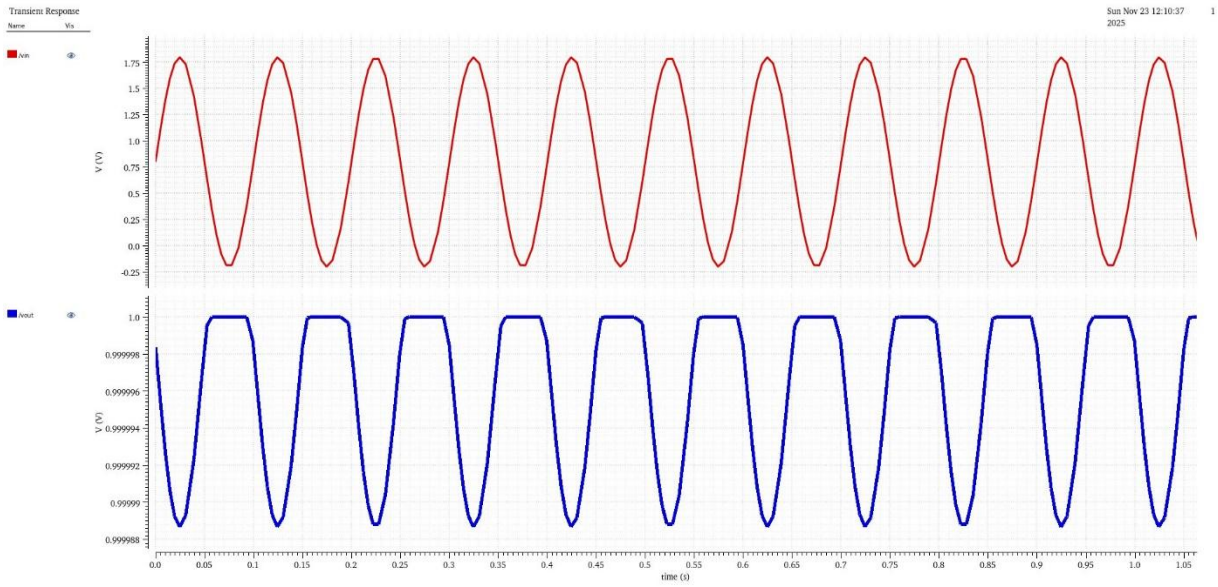
Library Name	Cell Name	Properties
AnalogLib	vdc	Vdd: DC voltage = 1V
AnalogLib	vsin	AC magnitude = 5mV DC voltage = 800.0mV Frequency = 10KHz
gpdk180	R0	R=100 ohm

Simulation:

Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

Transient Response:



Layout:

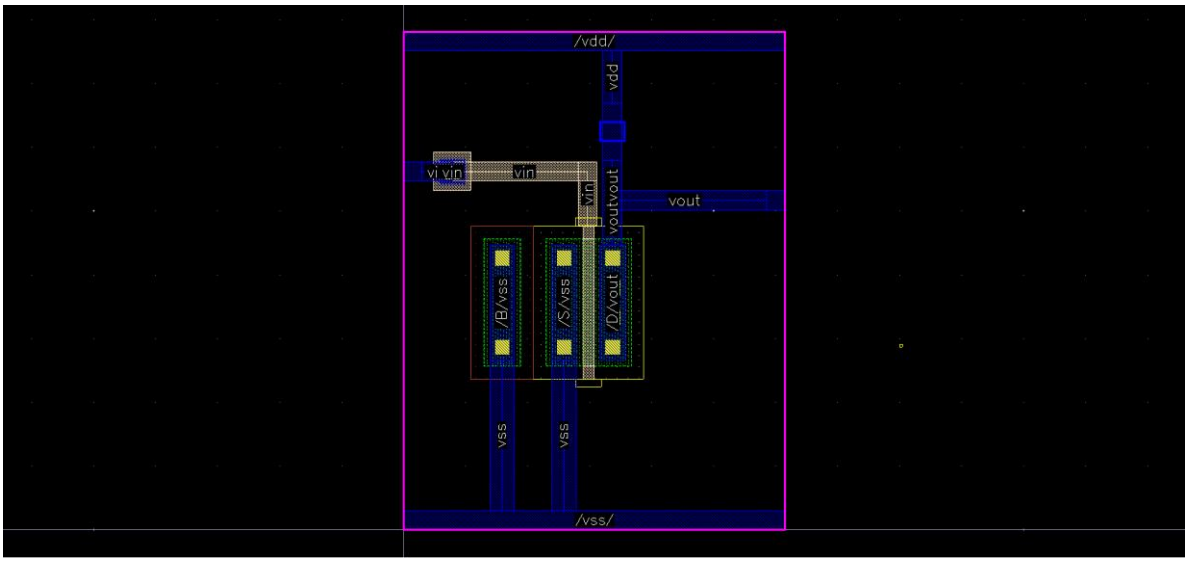


Fig: Common Source with Resistive Load Layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura - Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology - gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura - Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology - gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura - Quantus", select "Technology - gpdk180", "Output - Extracted View" from the "Setup" option, select "Extraction Type - RC" and "Ref Node - VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

Conclusion:

The Common Source amplifier with a resistive load successfully demonstrated voltage amplification with a clear 180° phase inversion between input and output. The circuit operated in the saturation region, and the small-signal gain depended primarily on the MOSFET transconductance and the load resistance. Overall, the experiment verified the fundamental behaviour of the CS configuration as a reliable voltage amplifier with high input impedance and moderate gain.

EXPERIMENT - 03

COMMON SOURCE WITH CURRENT SOURCE LOAD

Aim: To design, simulate, and implement the schematic and physical layout of a MOSFET common source with current source load using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm.

Theory: The common-source (CS) amplifier with a current source load is a high-gain MOSFET amplifier in which the input signal is applied to the gate of an NMOS transistor, and the load at the drain is provided by an active PMOS current source rather than a passive resistor. Replacing the resistor with an active load significantly increases the small-signal voltage gain, improves output swing, and enhances linearity. This configuration is widely used in analog IC design and is fundamental to differential pairs, operational amplifiers, and gain stages.

The NMOS transistor operates in saturation, where the small-signal drain current is controlled by:

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_{oN}}.$$

The PMOS transistor functions as a current source load, biased to remain in saturation and supply a nearly constant drain current I_D. Its small-signal resistance contributes to the overall load resistance.

Since both transistors are in saturation, the small-signal output node experiences the combined output resistances of the NMOS and PMOS:

$$r_o = r_{oN} \parallel r_{oP}.$$

Applying an AC input signal $v_{in}$to the gate modulates the NMOS drain current, producing a small-signal change in the output voltage at the drain:

$$v_o = -i_d(r_{oN} \parallel r_{oP})$$

The small-signal voltage gain of the common-source stage with a current source load is:

$$A_v = -g_m(r_{oN} \parallel r_{oP}).$$

In contrast, a resistor-loaded CS amplifier has:

$$A_v \approx -g_m R_D,$$

The input is applied to the MOS gate, so the input impedance is extremely high:

$$R_{in} \approx \text{gate resistance} \gg 1\ \text{M}\Omega.$$

The output impedance is the parallel combination of the two devices' output resistances:

$$R_{out} = r_{oN} \parallel r_{oP}.$$

Procedure

Follow the techniques, create a New Library using the option "File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:

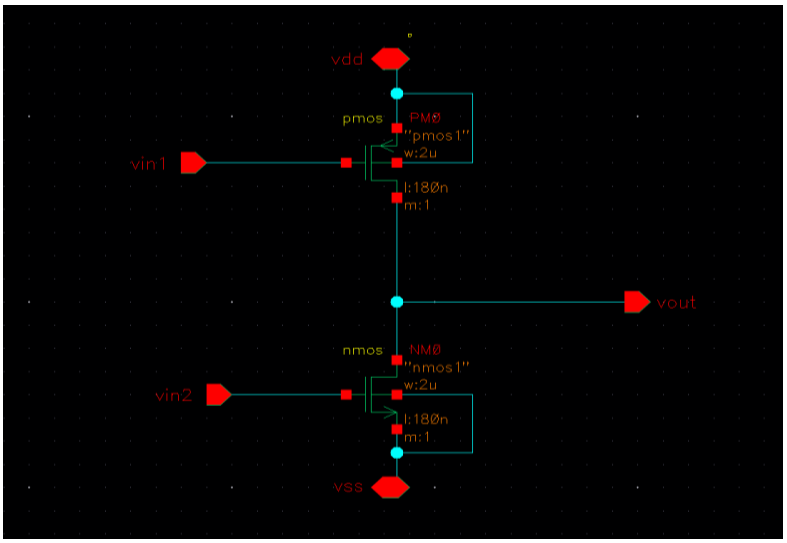


Fig: Schematic of Common Source with current source load

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Common source with current source load, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

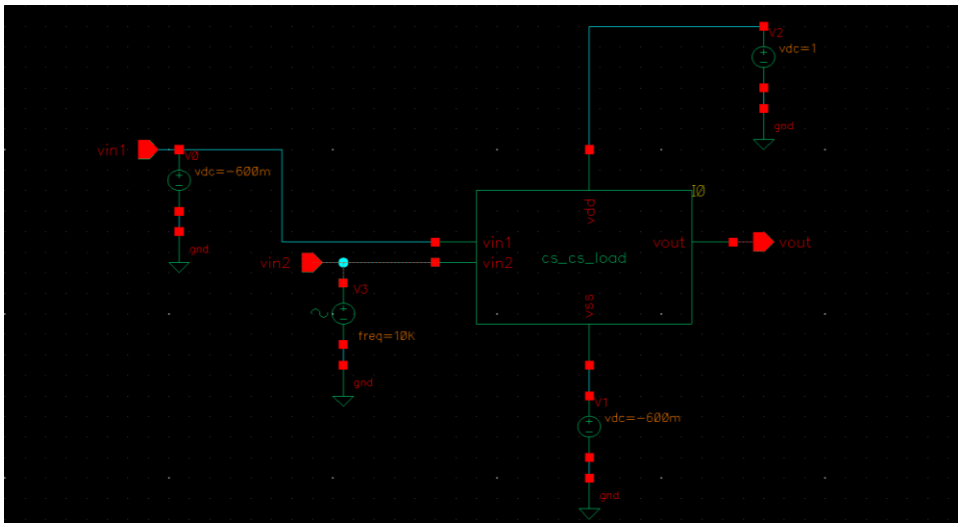


Fig: Test bench schematic of Common Source with current source load

Properties of vdc and vsin:

Library Name	Cell Name	Properties
AnalogLib	vdc	Vin1: DC voltage = -600mV
AnalogLib	vdc	Vss: DC voltage = -600mV
AnalogLib	vsin	AC magnitude = 1V Frequency = 1KHz
AnalogLib	vdc	Vdd: DC voltage = 1V

Simulation:

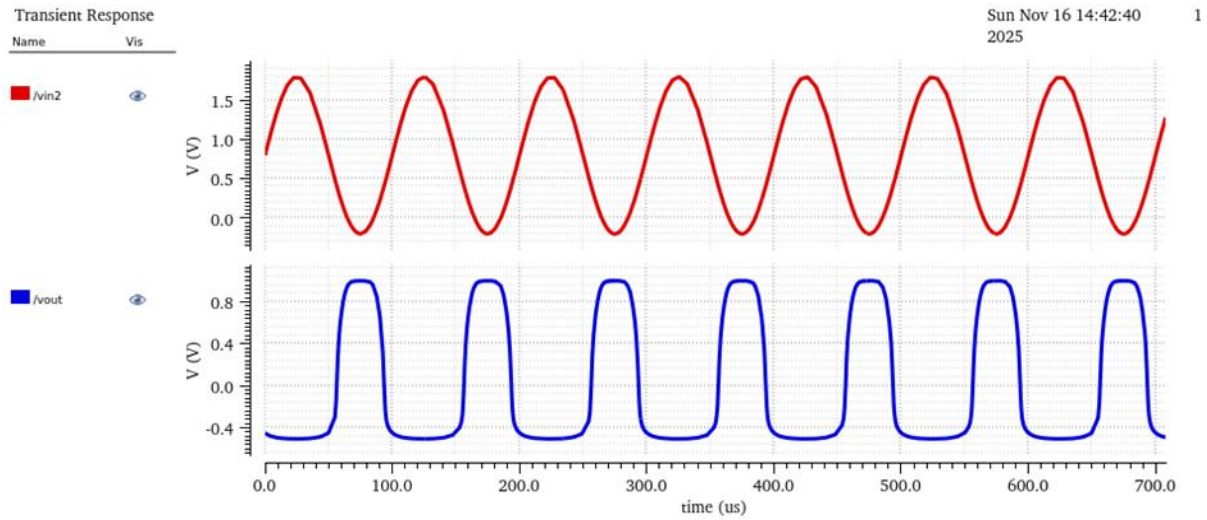
Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

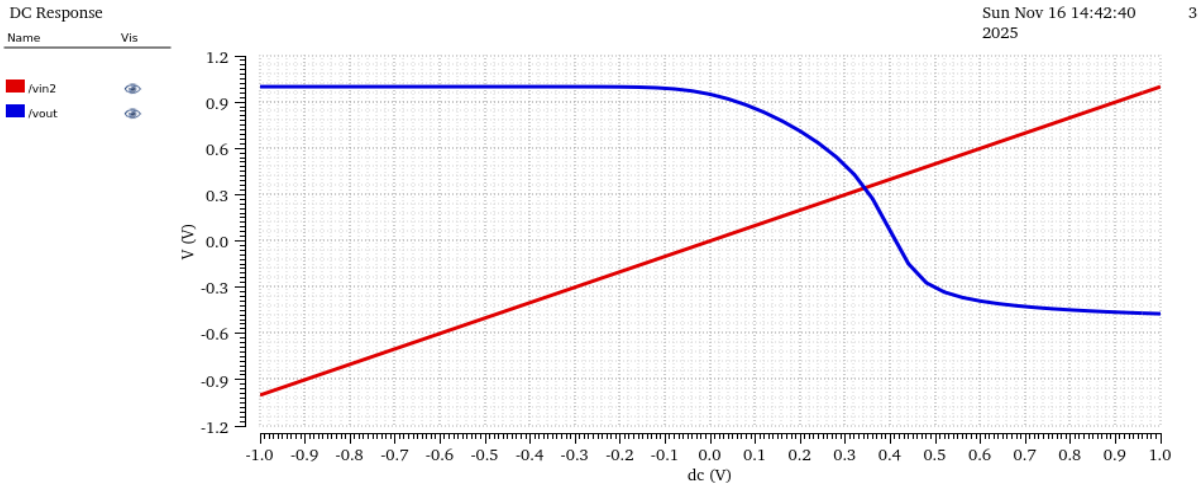
To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "-1" and "Stop" value as "1", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "0" and "Stop" value as "1M", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".

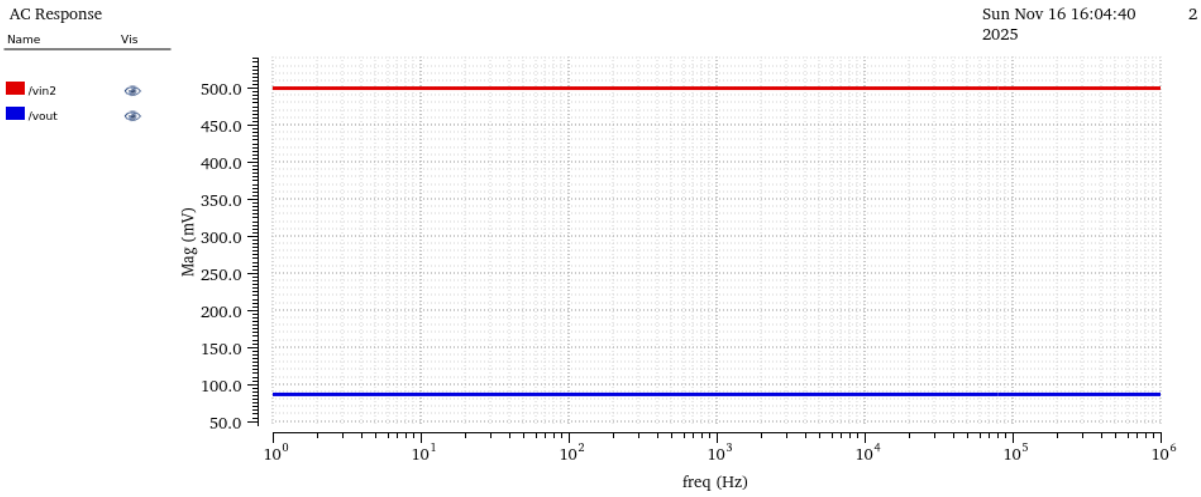
Transient Response:



DC Response :



AC Response :



Layout:

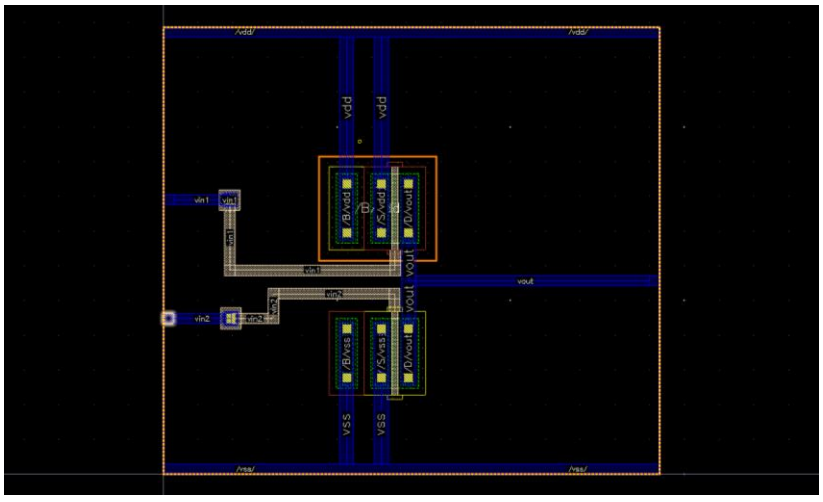


Fig: Common source with current source load layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura → Quantus", select "Technology →gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type →RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

Conclusion:

The common source with current source load was successfully designed and implemented using Cadence Virtuoso. Pre- layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.

EXPERIMENT - 04

COMMON GATE

Aim: To design, simulate, and implement the schematic and physical layout of a MOSFET common gate using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm

Theory: The common-gate (CG) amplifier is a MOSFET configuration in which the gate terminal is AC-grounded, the input signal is applied to the source, and the output is taken at the drain. Because the input enters through the source terminal, the common-gate stage exhibits low input impedance, high output impedance, and moderate voltage gain, making it useful for high-frequency and current-mode applications.

In the common-gate configuration, the MOSFET is biased such that it operates in saturation, where the drain current is

$$I_D = \frac{1}{2} k_n (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}).$$

Using the small-signal hybrid-π model, the input small-signal current is

$$i_i = g_m v_{gs} + \frac{v_{ds}}{r_o}.$$

Since the gate is AC-grounded, $v_{gs} = -v_i$and the small-signal voltage gain becomes:

$$A_v = \frac{v_o}{v_i} = g_m R_D \parallel r_o + 1.$$

In most practical cases, $g_m R_D \gg 1$, so the gain simplifies to:

$$A_v \approx g_m R_D.$$

The small-signal input impedance is:

$$R_{in} \approx \frac{1}{g_m}.$$

The drain terminal exhibits high output resistance:

$$R_{out} \approx r_o.$$

Procedure

Follow the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:

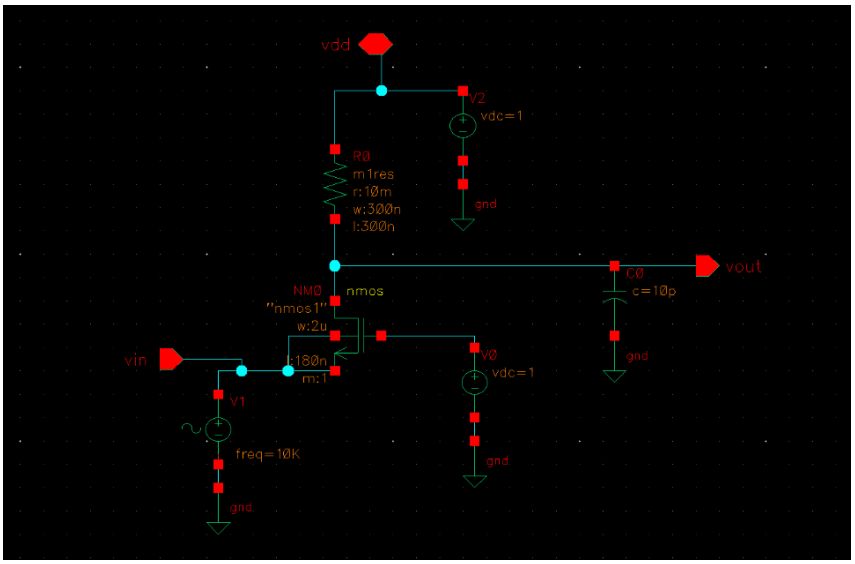


Fig: Schematic of Common Gate

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Common gate, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

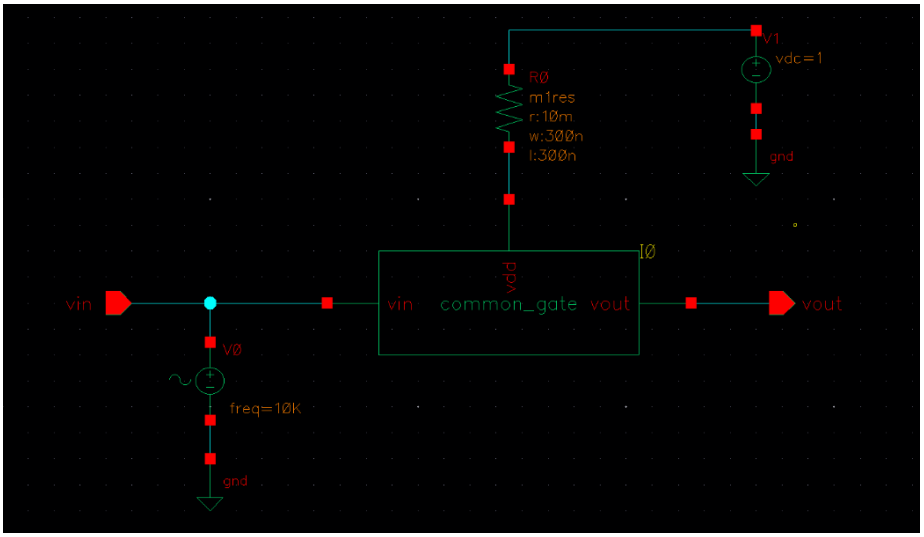


Fig: Test bench schematic of Common Gate

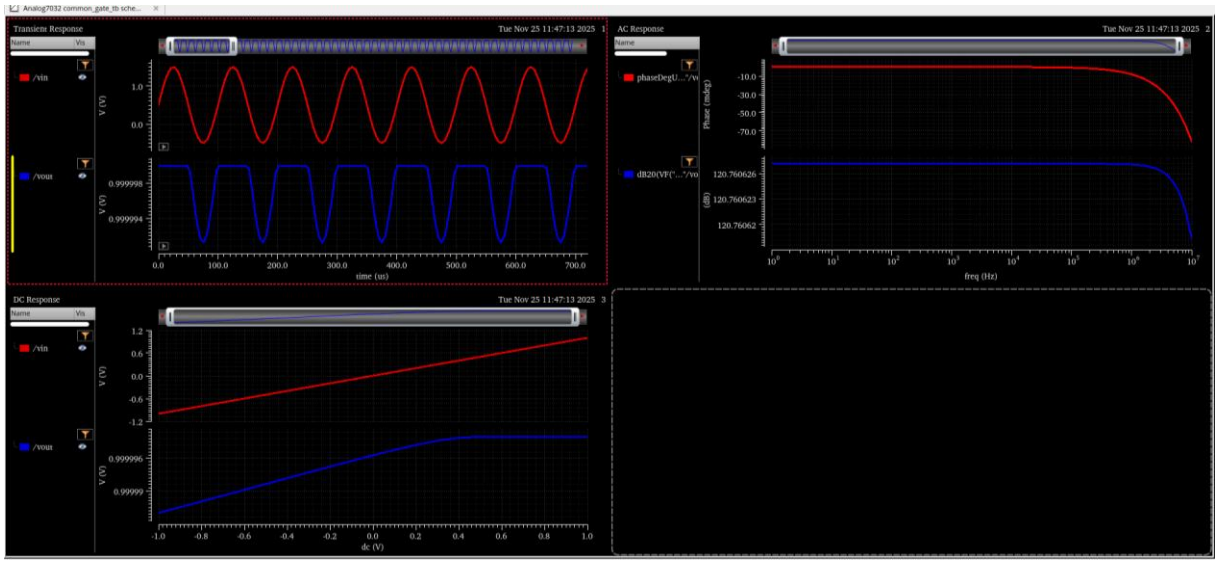
Simulation:

Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "-1" and "Stop" value as "1", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "1" and "Stop" value as "10M", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".



<u>Layout</u>:

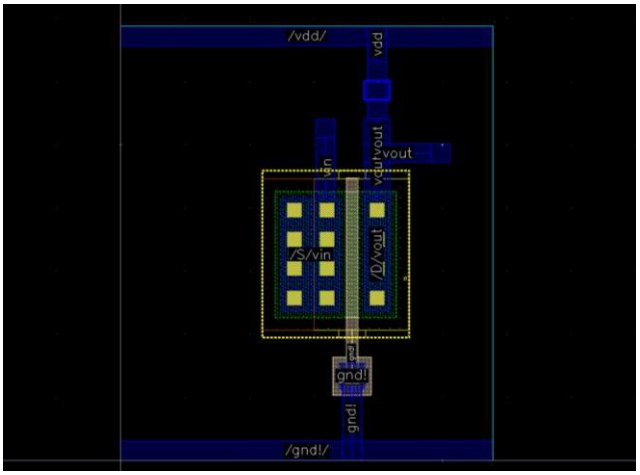


Fig: Common Gate layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura → Quantus", select "Technology →gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type → RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

Conclusion:

The common gate was successfully designed and implemented using Cadence Virtuoso. Pre-layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.

EXPERIMENT - 05

COMMON DRAIN

Aim: To design, simulate, and implement the schematic and physical layout of a MOSFET common drain using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm

Theory: The common-drain amplifier, also known as the source follower, is a MOSFET configuration in which the drain terminal is held at AC ground (usually connected to V_{DD}or through a large bypass capacitor), the input signal is applied to the gate, and the output is taken from the source. Because the output follows the input with a small voltage drop, the circuit behaves similarly to a voltage buffer.

In the common-drain configuration, the MOSFET operates in saturation, where the drain current is given by

$$I_D = \frac{1}{2} k_n (V_{GS} - V_{th})^2.$$

Since the drain is at a fixed voltage, variations in the gate voltage directly influence V_{GS}, which in turn modulates the source voltage. When the source resistor $R_S$is present, the output voltage is approximately:

$$v_o \approx v_i - V_{GS}.$$

Because $V_{GS}$is relatively constant for small-signal operation, the output "follows" the input. Using the small-signal hybrid-π model, the output voltage is determined by the transconductance $g_m$and the source resistance:

$$v_o = \frac{g_m R_S}{1 + g_m R_S} v_i.$$

Thus, the voltage gain $A_v$is:

$$A_v = \frac{v_o}{v_i} = \frac{g_m R_S}{1 + g_m R_S}.$$

For large $g_m R_S$:

$$A_v \approx 1.$$

Because the gate of a MOSFET is insulated, the input sees only the gate capacitances:

$$\mathrm{R_{in}} \approx \infty,$$

making the common-drain a very good voltage buffer.

The output impedance is dominated by the source resistance and MOSFET small-signal parameters:

$$\mathrm{R_{out}} \approx \frac{1}{\mathrm{g_m}} \parallel \mathrm{r_o}.$$

Procedure

Follow the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:

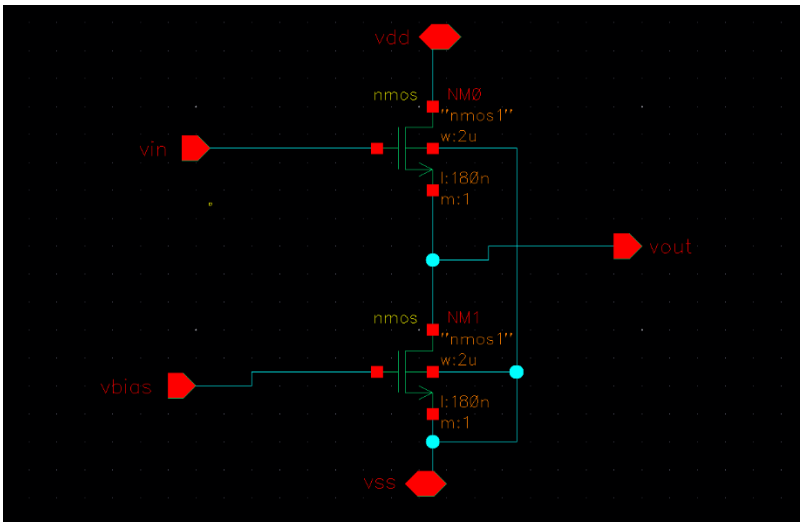


Fig: Schematic of Common Drain

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Common drain, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

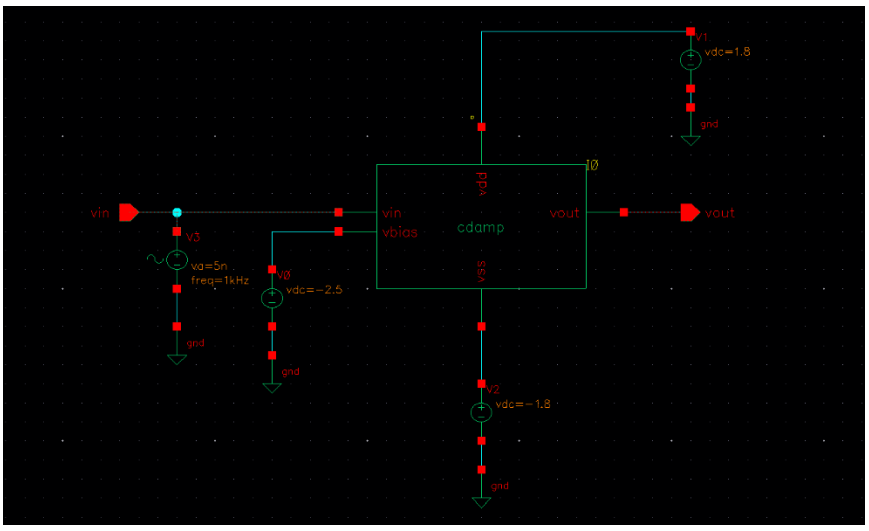


Fig: Test bench schematic of Common Drain

Properties of vdc and vsin:

Library Name	Cell Name	Properties
AnalogLib	vdc	Vdd: DC voltage = 1.8V
AnalogLib	vdc	Vss: DC voltage = -1.8V
AnalogLib	vsin	AC magnitude = 1V Amplitude = 5nV Frequency = 1KHz
AnalogLib	Vdc	Vbias: DC voltage = -2.5V

Simulation:

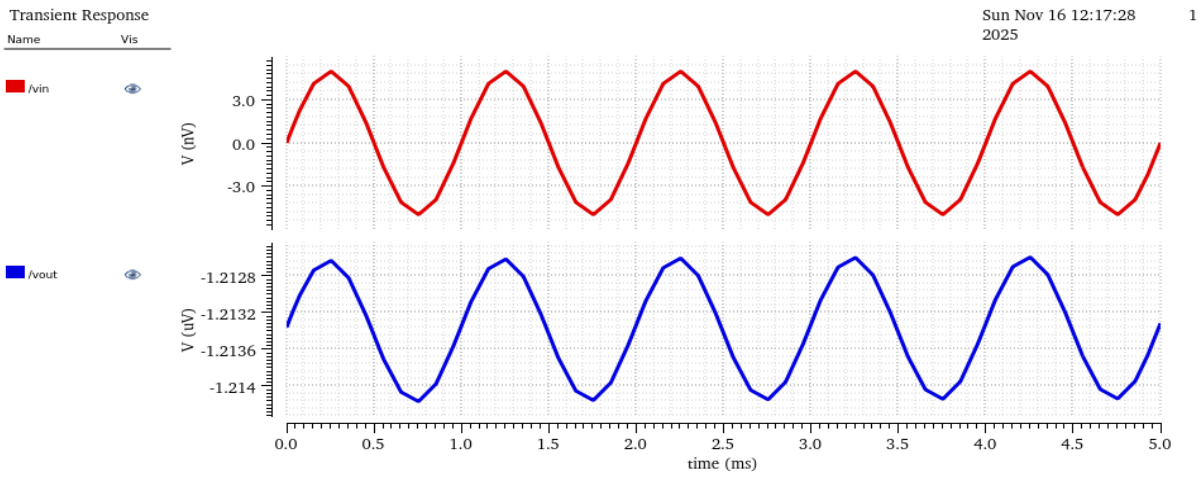
Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

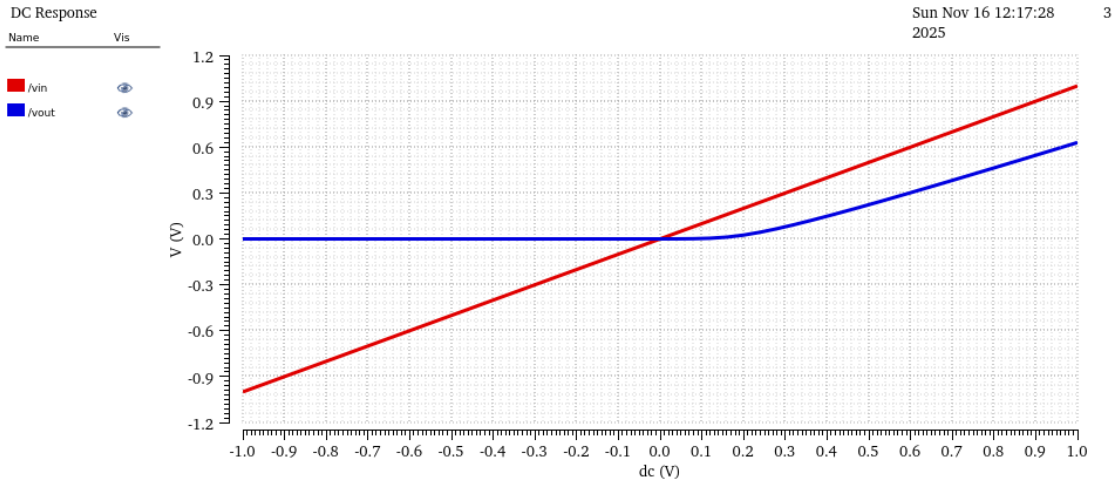
To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "-1" and "Stop" value as "1", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "1" and "Stop" value as "10M", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".

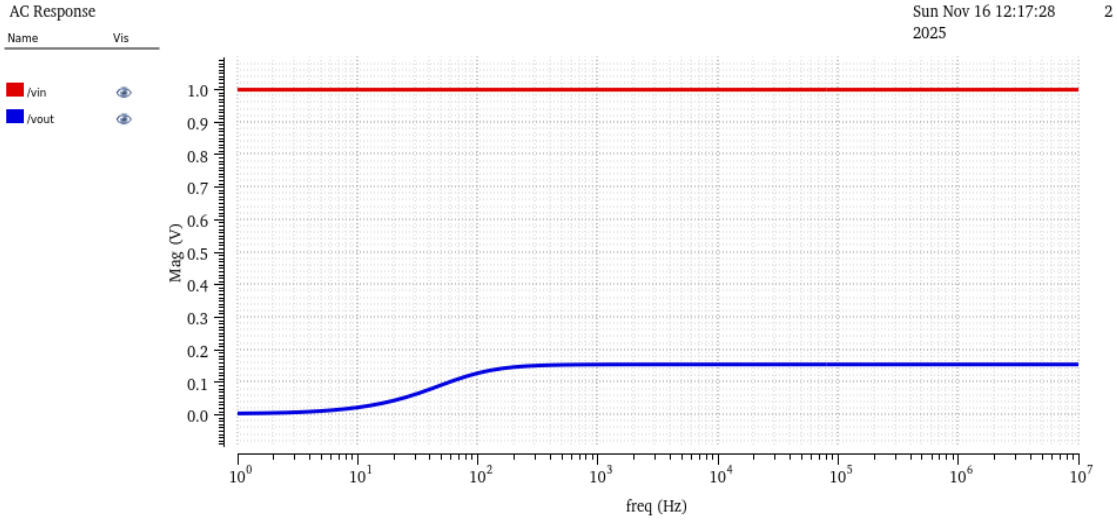
Transient Response:



DC Response:



AC Response:



Layout:

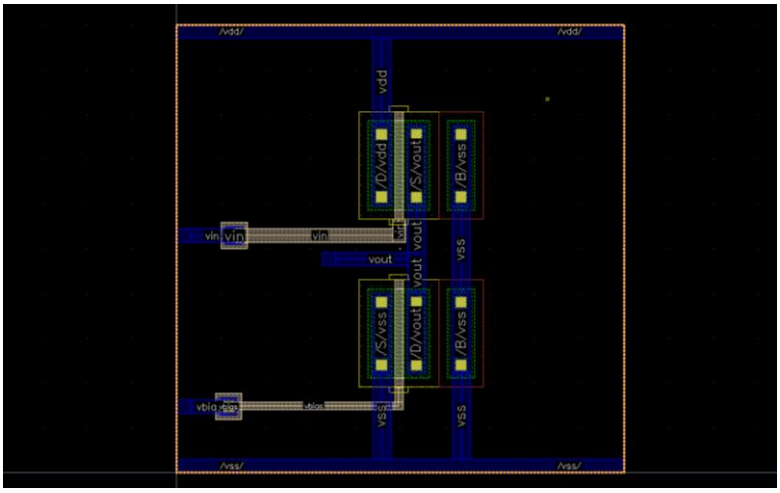


Fig: Common Drain layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura → Quantus", select "Technology →gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type →RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

Conclusion:

The common drain was successfully designed and implemented using Cadence Virtuoso. Pre-layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.

EXPERIMENT - 06

CASCODE AMPLIFIER

Aim: - To design, simulate, and implement the schematic and physical layout of a MOSFET cascode amplifier using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm

Theory: A cascode amplifier is a two-transistor configuration that combines a common-source (CS) or common-emitter stage with a common-gate (CG) or common-base stage. It is widely used in analog integrated circuit design due to its ability to achieve high gain, improved bandwidth, and enhanced output impedance. In CMOS design, the cascode topology is implemented using MOSFETs and is an essential building block in operational amplifiers, current mirrors, low-noise amplifiers, and RF circuits.

The total small-signal voltage gain of the cascode amplifier is approximately:

$$A_v \approx g_{m1} \times (r_{o1} \parallel g_{m0} r_{o0} r_{o1})$$

Because the cascode device significantly boosts output resistance, the overall gain becomes:

$$A_v \approx g_{m1} \cdot r_{o1} \cdot g_{m0} \cdot r_{o0}$$

This is much larger than that of a single common-source amplifier.

Procedure

Following the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:

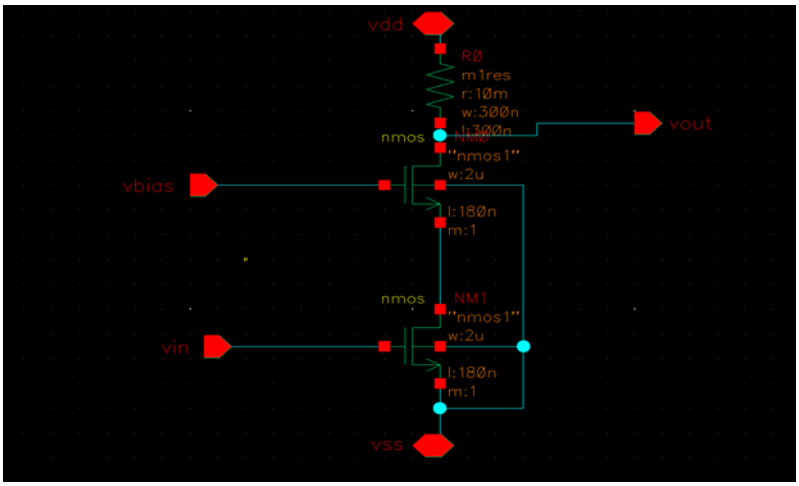


Fig: Schematic of Cascode Amplifier

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Cascode amplifier, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

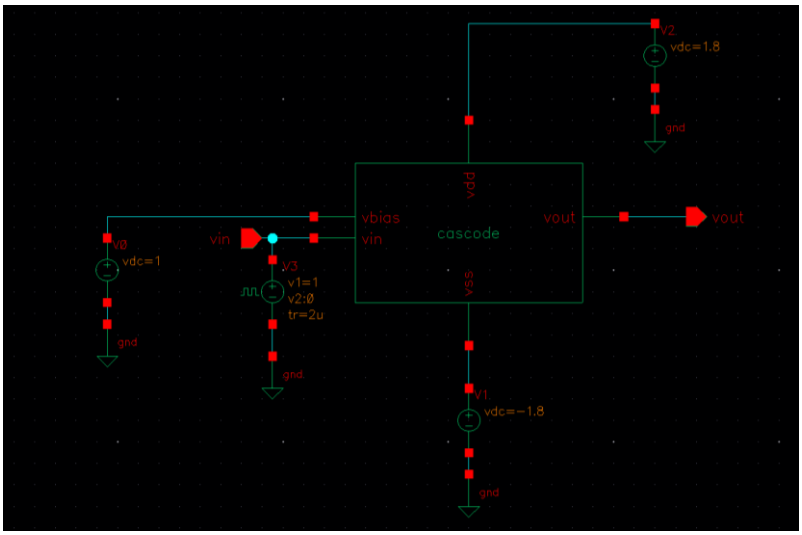


Fig: Test bench schematic of Cascode Amplifier

Properties of vdc and vpulse

Library Name	Cell Name	Properties
AnalogLib	Vdc	Vbias: DC voltage = 1V Vss: DC voltage = -1.8V Vdd: DC voltage = 1.8V
AnalogLib	Vpulse	V1 = 1V V2 = 0V Delay time = 0ns Rise time = 2ns Fall time = 2ns Pulse width = 5ns

Simulation:

Launch ADE L, import the design variables, mention the values and select the Transient Analysis, and mention the parameters and choose the signals to be plotted as shown in Figure.

To set up a "**Transient Analysis**", select "tran", mention the **Stop Time – 2m** select **Accuracy Defaults - moderate**, click on "Apply" and click on "OK".

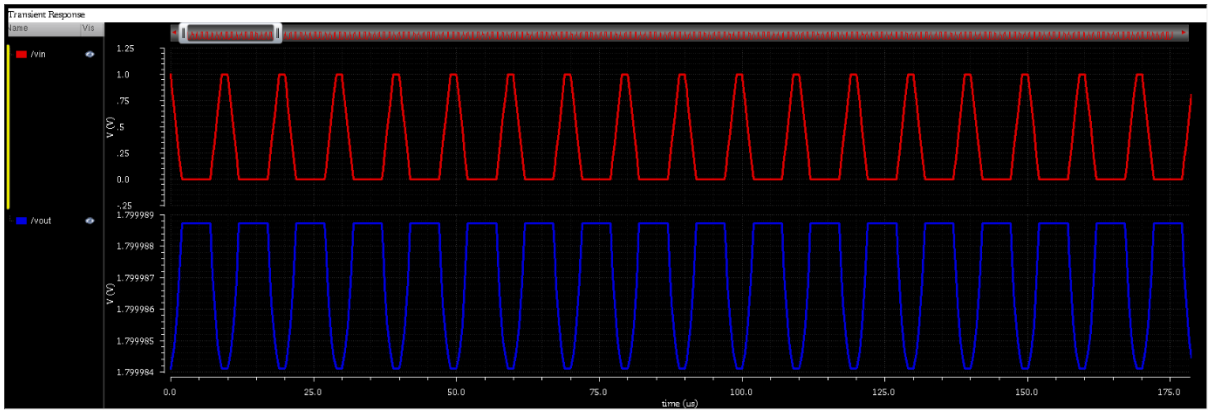


Fig: Pre-layout stimulation of Cascode Amplifer

Layout:

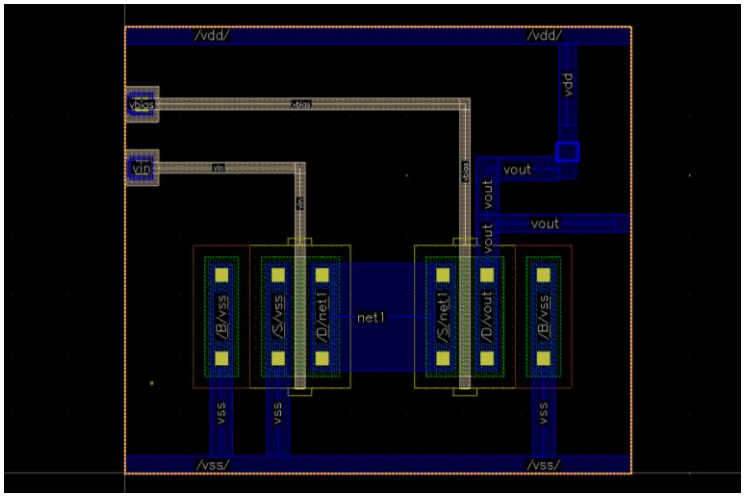


Fig: Cascode amplifier layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura → Quantus", select "Technology →gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type → RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

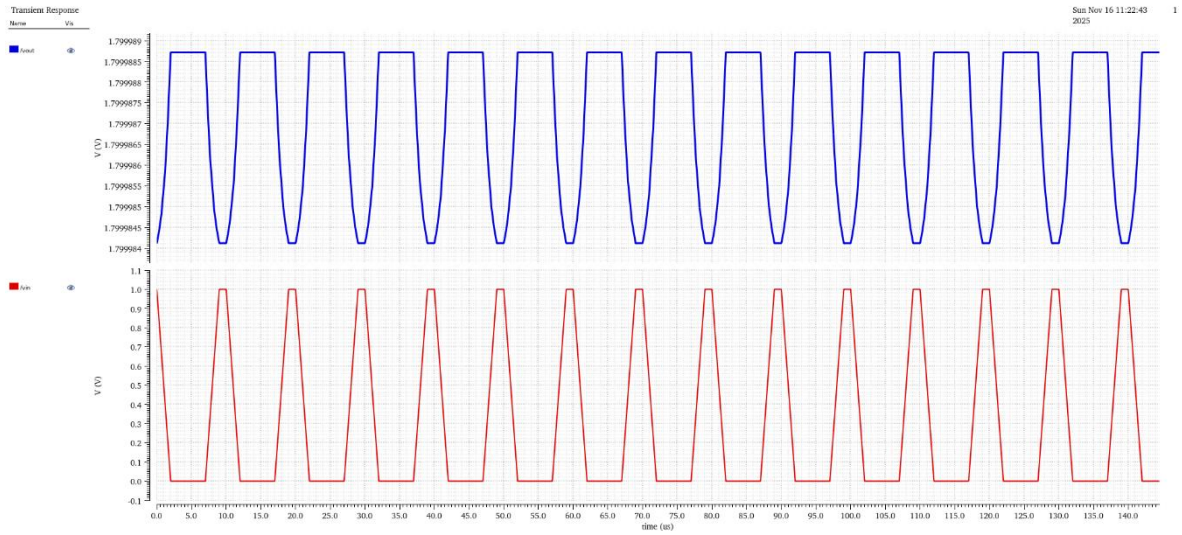


Fig: Post-layout stimulation of Cascode Amplifer

Conclusion:

The cascode amplifier was successfully designed and implemented using Cadence Virtuoso. Pre-layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.

EXPERIMENT - 07

CURRENT MIRRORS

Aim: To design, simulate, and implement the schematic and physical layout of a MOSFET current mirrors using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm

Theory: A current mirror is a circuit block which functions to produce a copy of the current flowing into or out of an input terminal by replicating the current in an output terminal. An important feature of the current mirror is a relatively high output resistance which helps to keep the output current constant regardless of load conditions. Another feature of the current mirror is a relatively low input resistance which helps to keep the input current constant regardless of drive conditions. Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well. Or it can consist of a current-controlled current source (CCCS).

If M1 and M2 are identical and operate in the same region, ideally $I_{OUT} = I_{REF}$. If sizes differ:

$$I_{OUT} \approx I_{REF} \cdot \frac{(W/L)_2}{(W/L)_1}$$

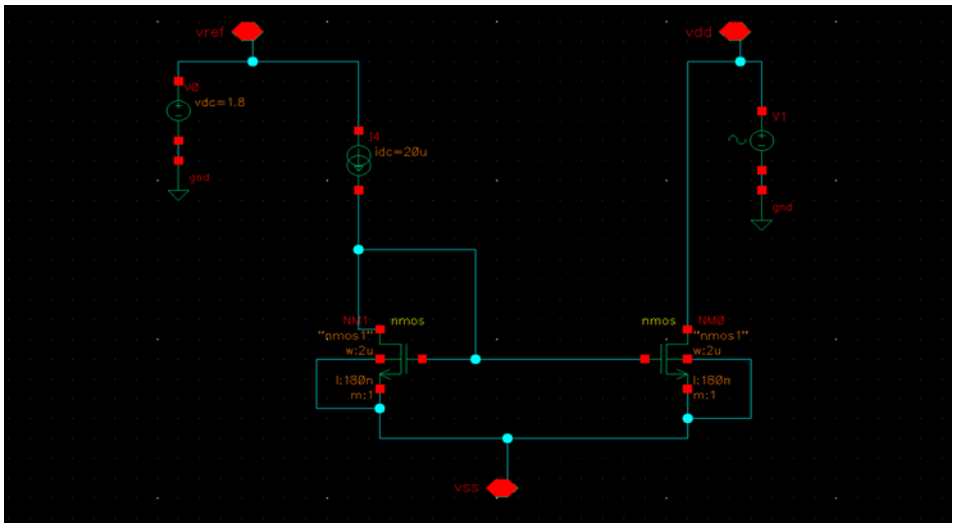
For MOS in saturation (approx):

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

Procedure

Follow the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:



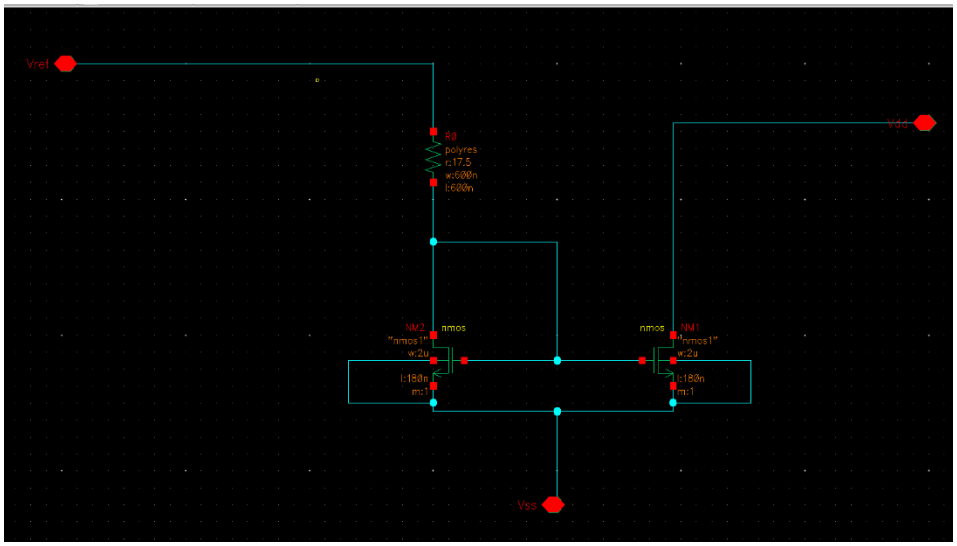


Fig: Schematic of Current Mirror

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Current mirror, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

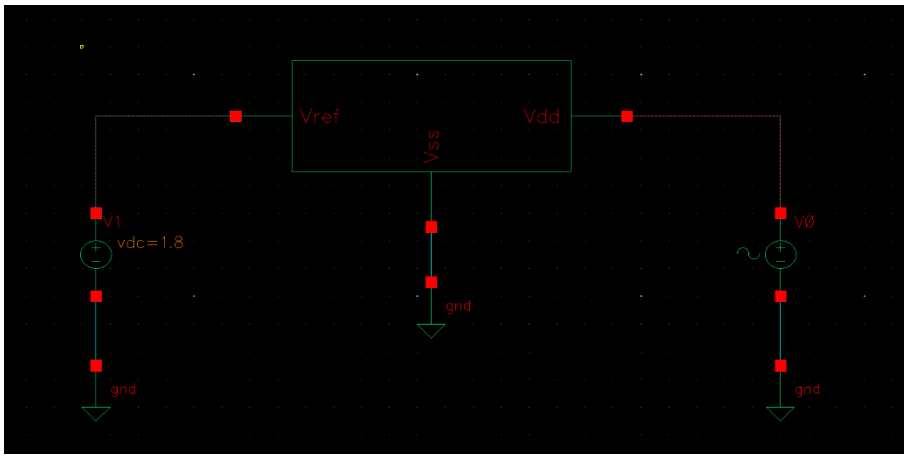


Fig: Test bench schematic of Current mirror

Properties of vdc and vsin

Library Name	Cell Name	Properties
AnalogLib	Vdc	Vref: DC voltage = 1.8V
AnalogLib	Vsin	DC Voltage = 1V AC Magnitude = 1V

Simulation:

Launch ADE L, import the design variables, mention the values and select the DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "0" and "Stop" value as "1", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "1" and "Stop" value as "1G", click on "Apply" and click on "OK".

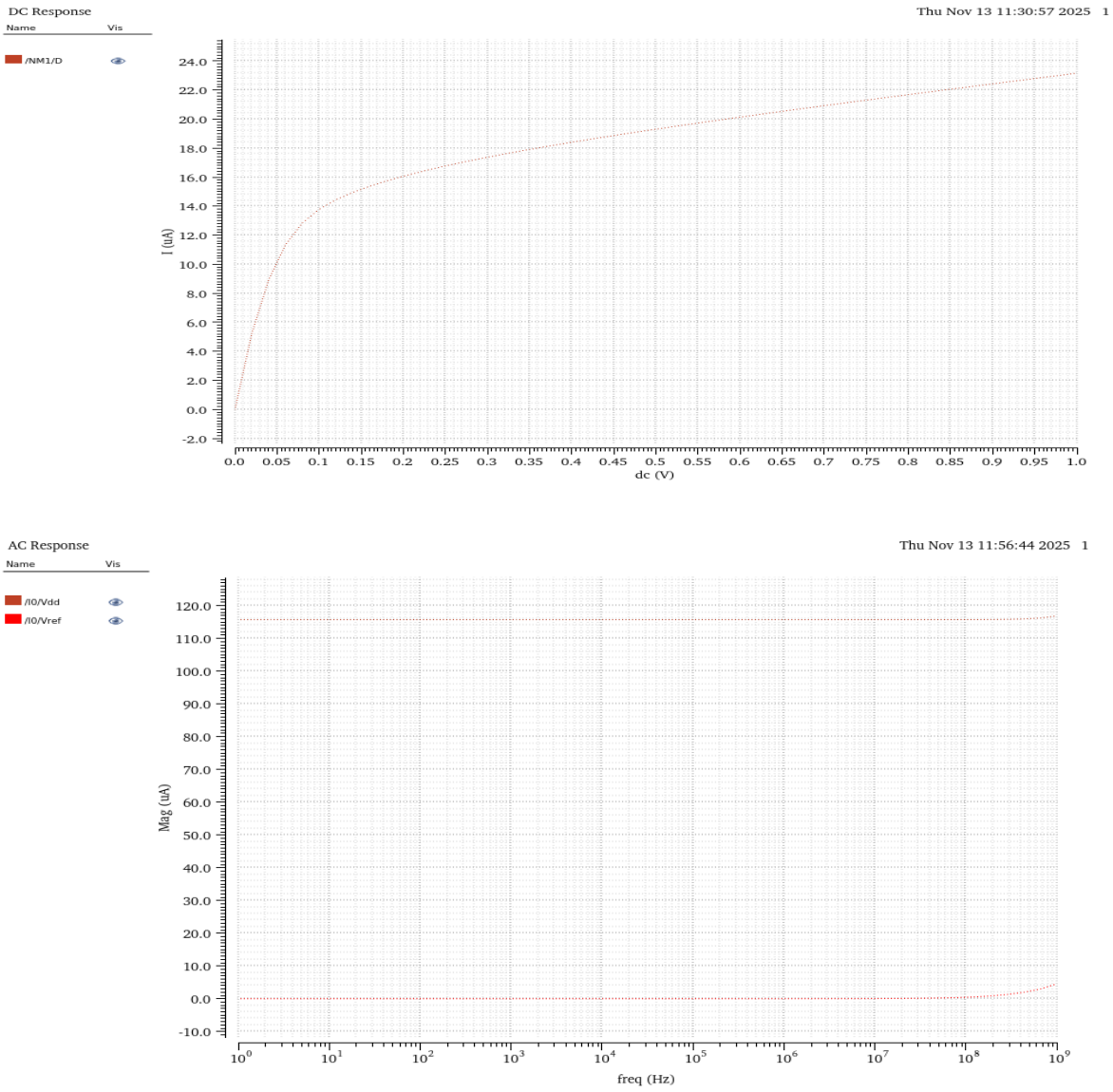


Fig: Pre-layout stimulation of Current mirror

Layout:

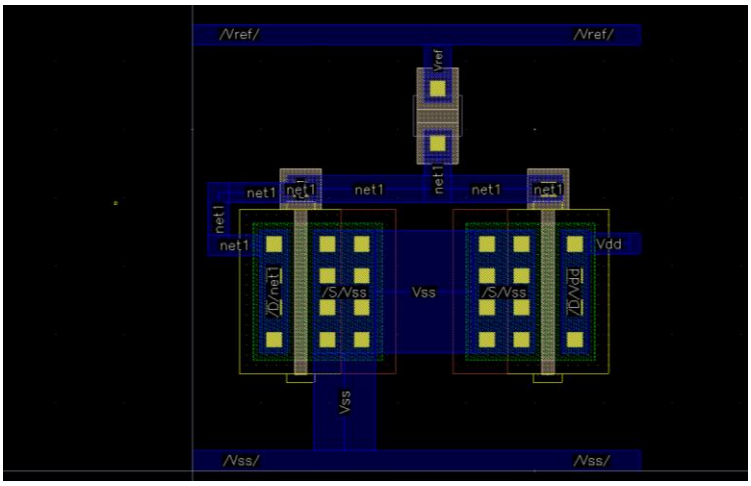


Fig: Current mirror layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura → Quantus", select "Technology → gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type → RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

Conclusion:

The current mirror was successfully designed and implemented using Cadence Virtuoso. Pre-layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.

EXPERIMENT - 08

DIFFERENTIAL AMPLIFIER

Aim: - To design, simulate, and implement the schematic and physical layout of a MOSFET differential amplifier using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm

Theory: The differential amplifier is a voltage subtractor circuit which produces an output voltage proportional to the voltage difference of two input signals applied to the inputs of the inverting and non-inverting terminals of an operational amplifier. This means that a differential amplifier naturally eliminates noise or interference that is present in both input signals.

For a symmetric MOS differential pair biased with tail current $I_{tail}$and small-signal transconductance $g_m$per input transistor, with an effective output resistance $R_o$at each output node: Differential output gain

$$A_d = \frac{v_{out,p} - v_{out,m}}{v_{id}}$$

For a basic differential pair:

$$A_d \approx g_m R_o$$

Procedure

Follow the techniques, Create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:

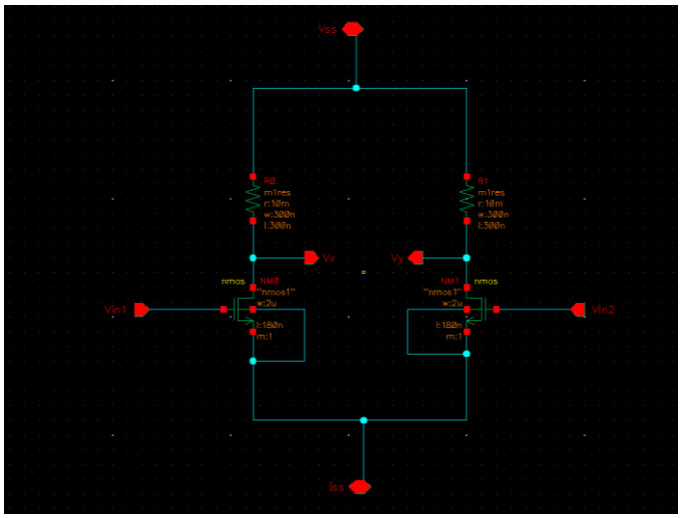


Fig: Schematic of Differential Amplifier

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of differential amplifier, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

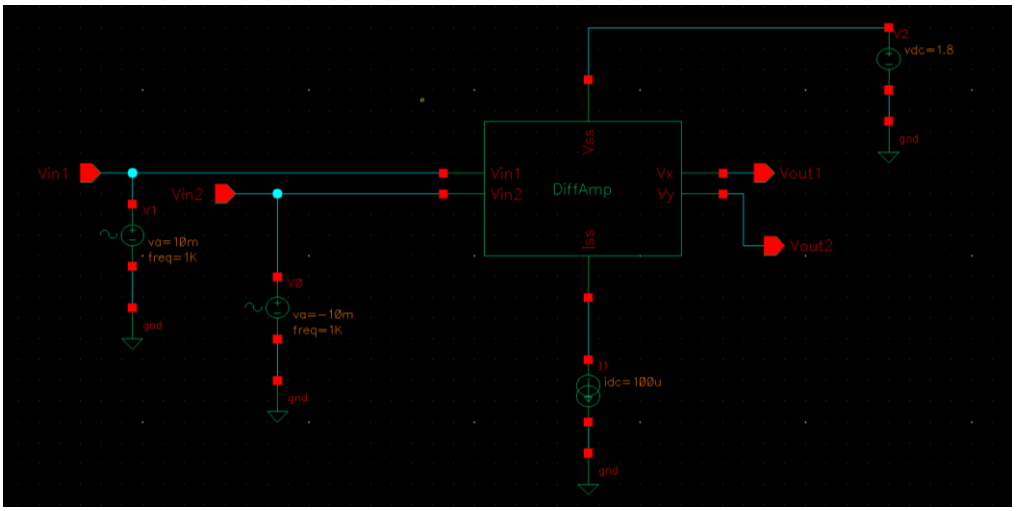


Fig: Test bench schematic of Differential Amplifier

Properties of vdc, vsin and idc:

Library Name	Cell Name	Properties
AnalogLib	vdc	Vdd: DC voltage = 1.8V
AnalogLib	vsin	AC = 1V Amplitude = 10mV Frequency = 1KHz
AnalogLib	vsin	AC = 1V AC phase = 180 Amplitude = 10mV Frequency = 1KHz
AnalogLib	idc	DC current = 100u A

Simulation:

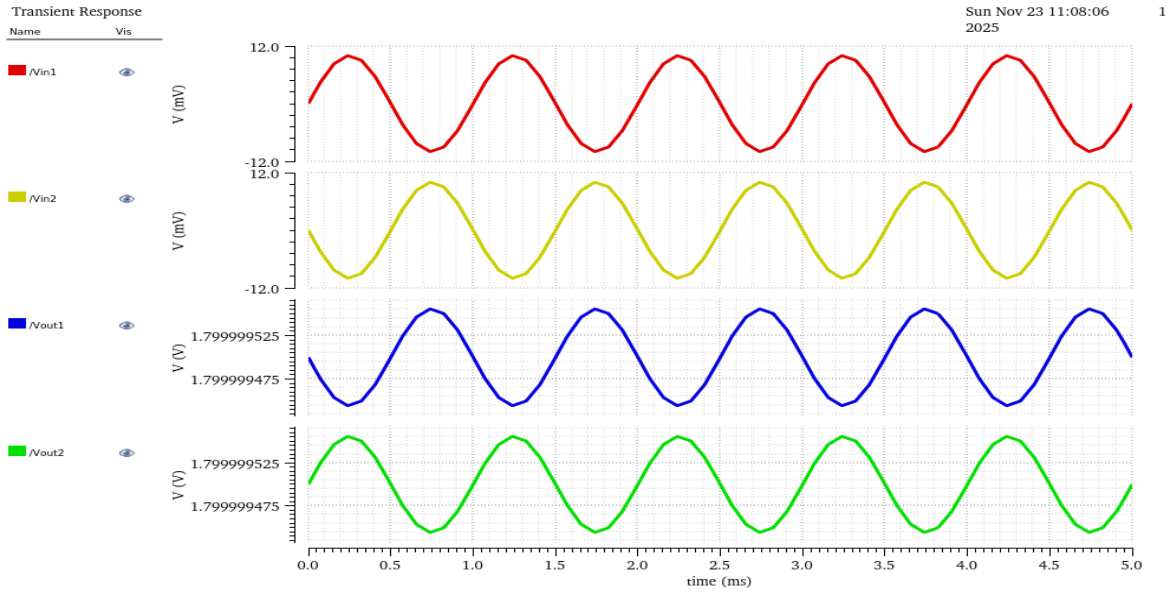
Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

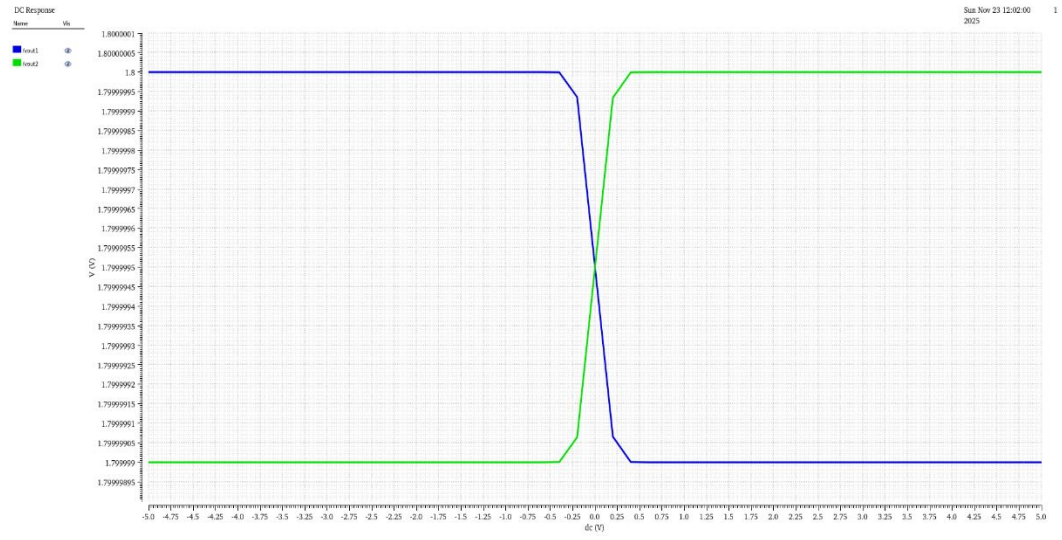
To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "-5" and "Stop" value as "5", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "10" and "Stop" value as "10G", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".

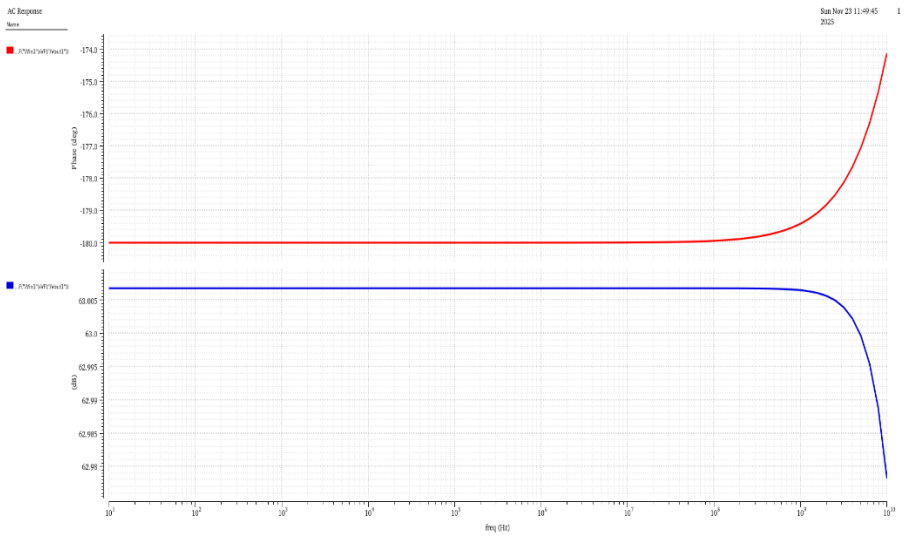
Transient Response:



DC Response:



AC Response:



Layout:

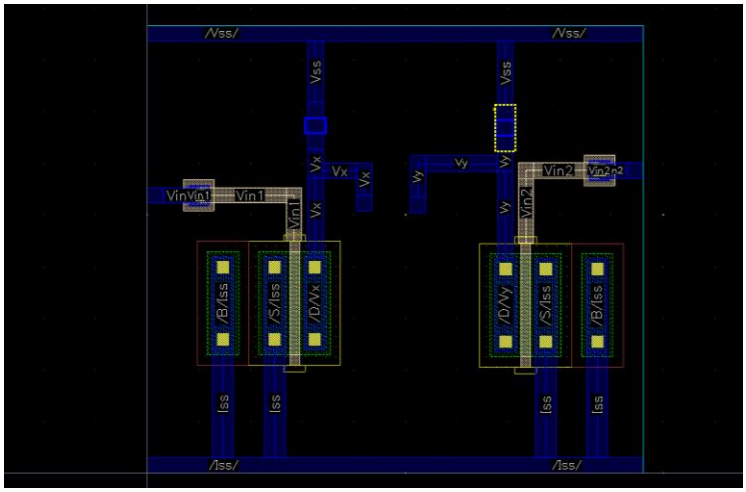


Fig: Differential amplifier layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select “Assura → Quantus”, select “Technology →gpdk180”, “Output → Extracted View” from the “Setup” option, select “Extraction Type → RC” and “Ref Node → VSS” from the “Extraction”, Disable HRCX and click on “OK”.

The result can be checked from the Library Manager.

Conclusion:

The differential amplifier was successfully designed and implemented using Cadence Virtuoso. Pre-layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.

EXPERIMENT - 09

SINGLE STAGE OPERATIONAL AMPLIFIER

Aim: To design, simulate, and implement the schematic and physical layout of a MOSFET Single stage operational amplifier using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm.

Theory: A single-stage op-amp is the simplest building block that provides voltage gain in one amplifier stage. Common MOS implementations:

- Common-source (CS) amplifier with active load — an NMOS input transistor with a PMOS current-mirror (or PMOS load) producing a high gain and single inverting stage.
- Common-source differential pair (single-ended output) — a single differential pair where one side is used and the other tied to reference (less common as "single-stage" output).

In this report we consider a single common-source stage with an active PMOS load (current mirror), biased by current sources. The stage is inverting: a small positive change at the gate produces a negative change at the output node.

For a single common-source stage with transistor M1 (input) and an active PMOS load whose small-signal resistance is $r_{o,load}$, the small-signal voltage gain (single-ended) is approximately:

$$A_v \approx -g_{m1} \cdot R_{out}$$

where the output resistance R_{out} is the parallel combination of the output resistances seen at the node:

$$R_{out} \approx r_{o1} \parallel r_{o,load}$$

So,

$$A_v \approx -g_{m1}(r_{o1} \parallel r_{o,load})$$

Procedure

Follow the techniques, create a New Library using the option "File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:

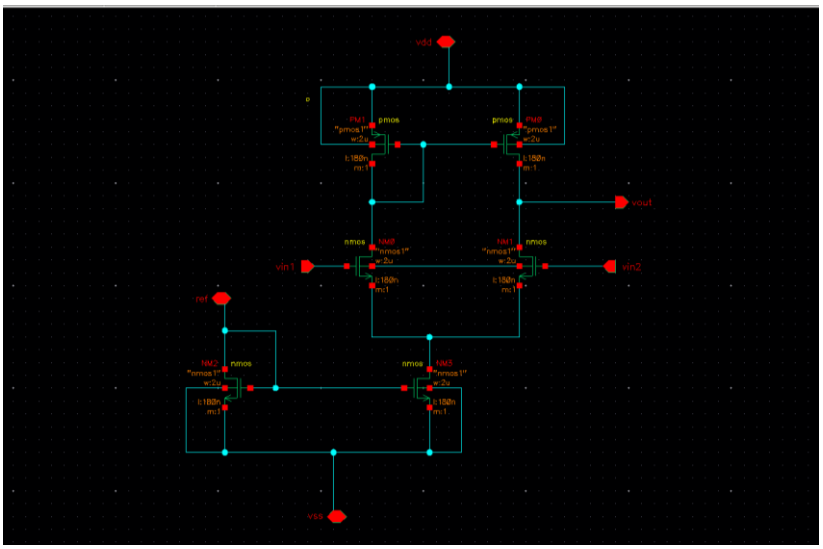


Fig: Schematic of Single Stage Operational Amplifier

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Single stage operational amplifier, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

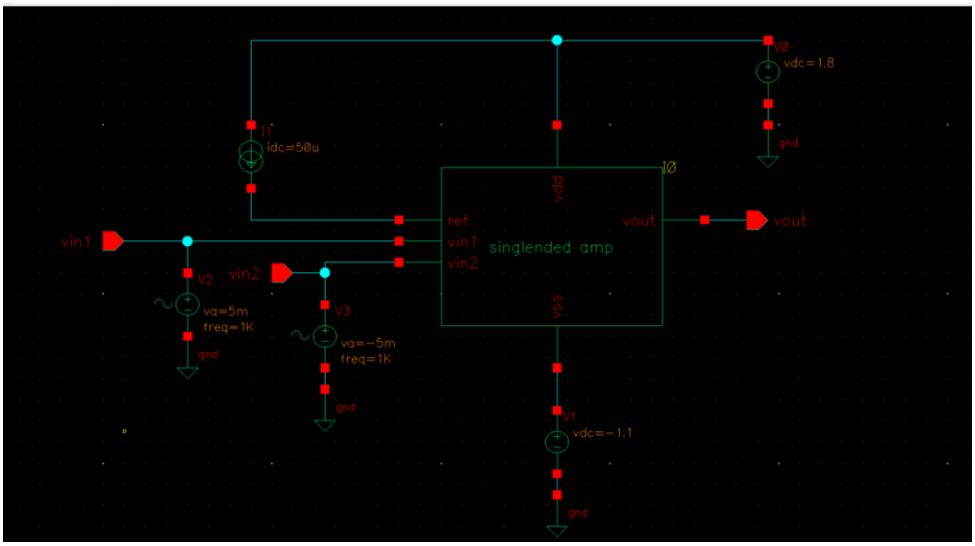


Fig: Test bench schematic of Single Stage Operational Amplifier

Properties of vdc and vsin:

Library Name	Cell Name	Properties
AnalogLib	vdc	DC voltage = 1.8V
AnalogLib	vdc	DC voltage = -1.1V
AnalogLib	vsin	AC magnitude = 1V Amplitude = 5m Frequency = 1KHz
AnalogLib	vsin	AC magnitude = 1V AC Phase = 180 Amplitude = -5m Frequency = 1KHz
AnalogLib	idc	DC current = 50u

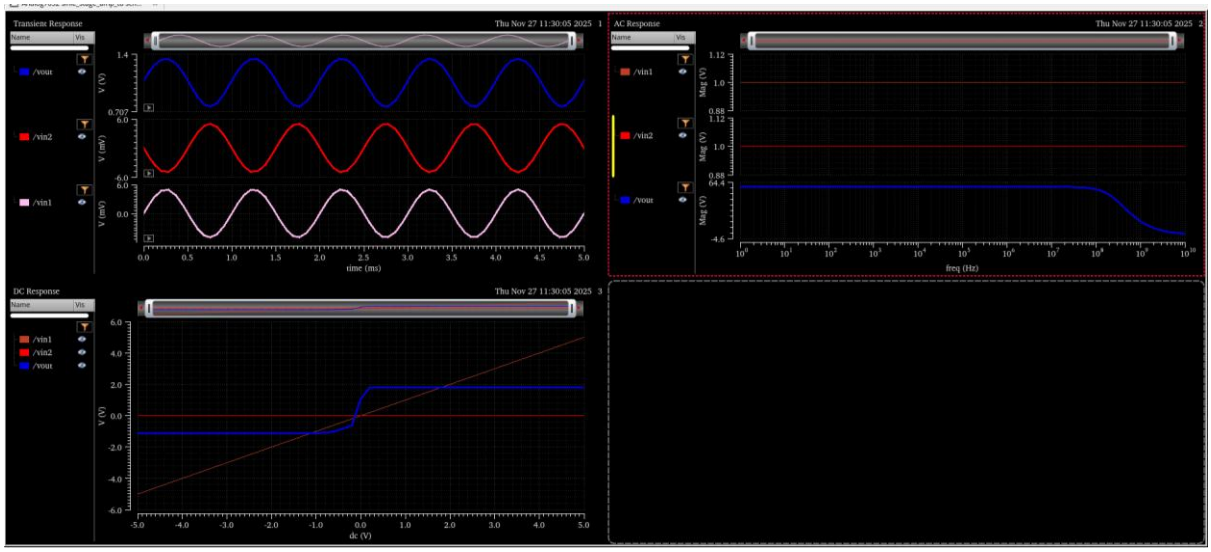
Simulation:

Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "-5" and "Stop" value as "5", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "1" and "Stop" value as "10G", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".



Layout:

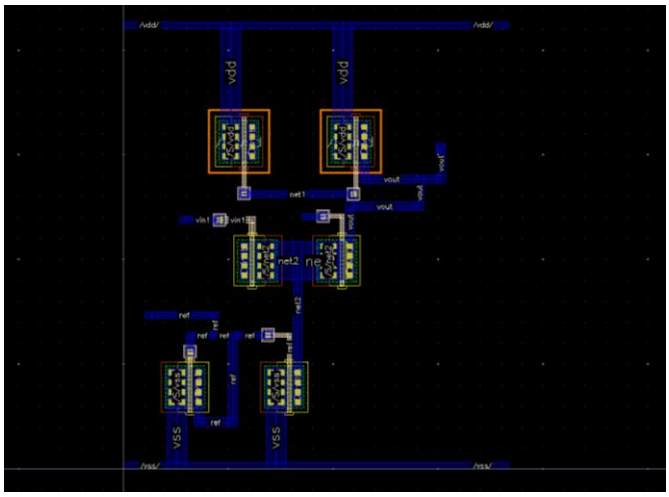


Fig: Single Stage Operational Amplifier layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura → Quantus", select "Technology →gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type →RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

Conclusion:

The Single Stage Operational Amplifier was successfully designed and implemented using Cadence Virtuoso. Pre- layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.

EXPERIMENT - 10

TWO STAGE OPERATIONAL AMPLIFIER

Aim: To design, simulate, and implement the schematic and physical layout of a MOSFET two stage operational amplifier using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm.

Theory: A two-stage CMOS operational amplifier combines high DC gain with adequate output swing and drive capability. It consists of:

1. Input differential gain stage, which converts differential input voltage into a high-gain single-ended signal.
2. Second gain/output stage, typically a common-source amplifier, which boosts gain and provides sufficient output drive.

This topology is widely used because it achieves high open-loop gain, supports moderate-to-large output swing, and can be compensated for stable operation in closed-loop configurations. In this lab, the op-amp is designed and simulated using Cadence Virtuoso.

Small-signal gain of stage 1:

$$A_1 \approx g_{m1}(r_{o1} \parallel r_{o,load})$$

Small-signal gain of stage 2:

$$A_2 \approx g_{m2}(r_{o2} \parallel r_{o,load2})$$

Overall DC Gain

$$A_v = A_1 \cdot A_2$$

Pole Expressions

$$p_1 \approx \frac{1}{(r_{o1} \parallel r_{o,load})C_1}$$

$$p_2 \approx \frac{1}{(r_{o2} \parallel r_{o,load2})C_L}$$

Procedure

Follow the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:

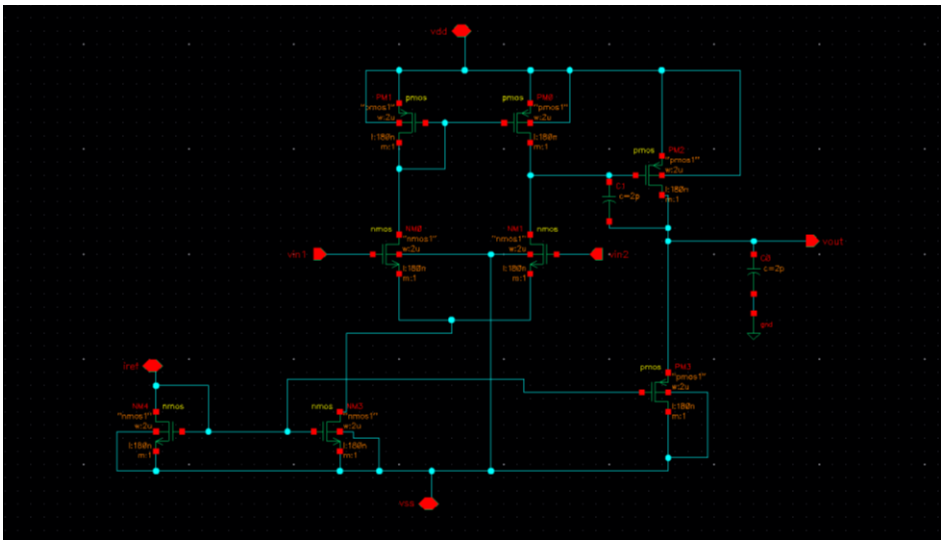


Fig: Schematic of two Stage Operational Amplifier

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of two stage operational amplifier, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

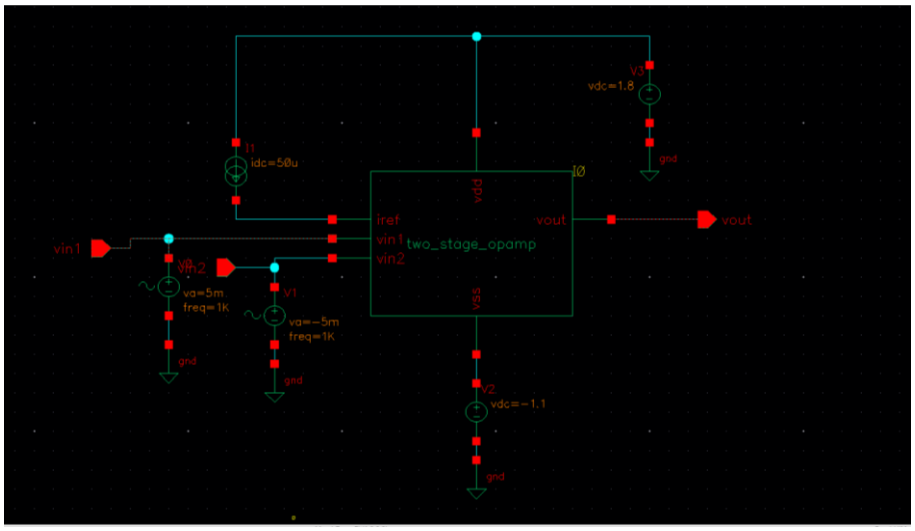


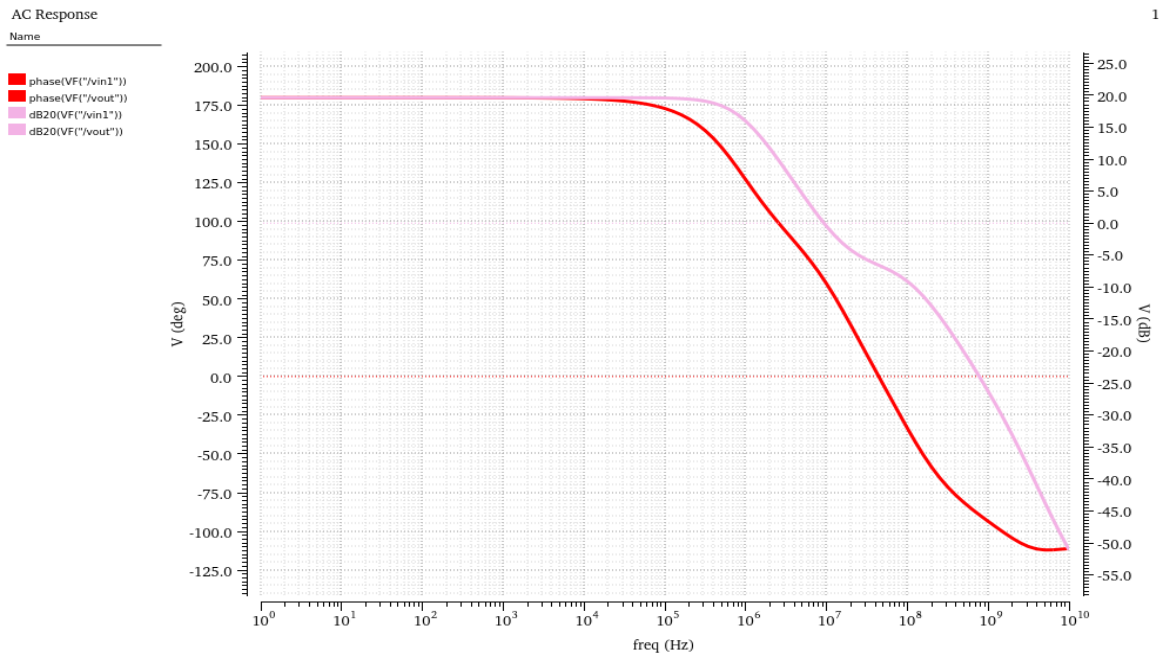
Fig: Test bench schematic of two Stage Operational Amplifier

Properties of vdc and vsin:

Library Name	Cell Name	Properties
AnalogLib	vdc	DC voltage = 1.8V
AnalogLib	vdc	DC voltage = -1.1V
AnalogLib	vsin	AC magnitude = 1V Amplitude = 5m Frequency = 1KHz
AnalogLib	vsin	AC magnitude = 1V AC Phase = 180 Amplitude = -5m Frequency = 1KHz
AnalogLib	idc	DC current = 50u

Simulation:

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "1" and "Stop" value as "10G", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".



Layout:

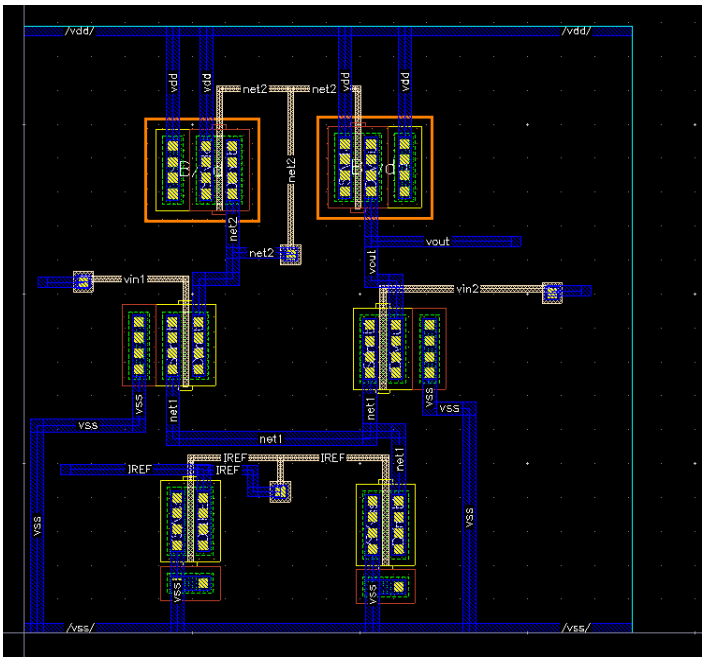


Fig: Two Stage Operational Amplifier layout

DRC:

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LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura → Quantus", select "Technology →gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type →RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

Conclusion:

The Two Stage Operational Amplifier was successfully designed and implemented using Cadence Virtuoso. Pre- layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.