EXPERIMENT – 02

COMMON SOURCE WITH RESISTIVE LOAD

Aim: To design, simulate, and implement the schematic and physical layout of MOSFET Common Source with Resistive Load using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules

Software & Technology used: CADENCE VIRTUOSO, 180nm

Theory: A Common Source (CS) amplifier is one of the most widely used MOSFET amplifier configurations because it provides voltage amplification with phase inversion. In this configuration, the source terminal is common to both input and output, the input is applied at the gate, and the output is taken from the drain. A resistor (RD) is used as the load, converting the drain current variations into voltage variations.

The MOSFET is biased such that it operates in the **saturation region**, where it behaves like a voltage-controlled current source.

- Saturation condition:

$$V_{DS} \geq V_{GS} - V_{th}$$

- Drain current (approx.):

$$I_D = \frac{1}{2} k_n (V_{GS} - V_{th})^2$$

Procedure:

Follow the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic:

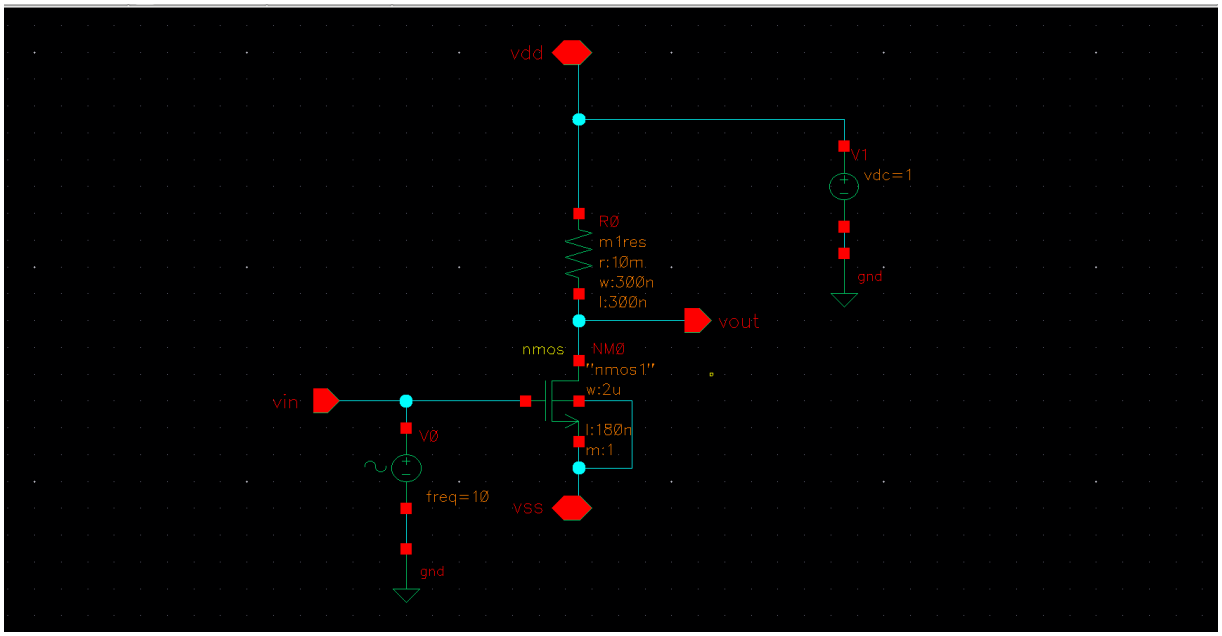


Fig: Schematic of Common Source with Resistive Load

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Common drain, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

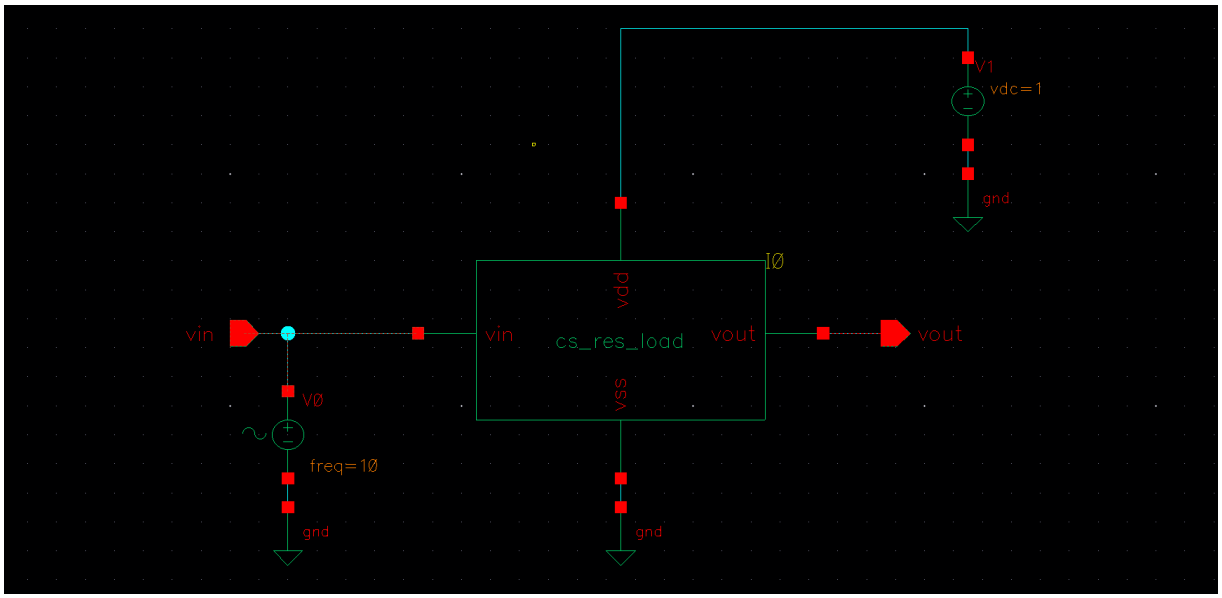


Fig: Test bench Schematic of Common Source with Resistive Load

Properties of vdc and vsin:

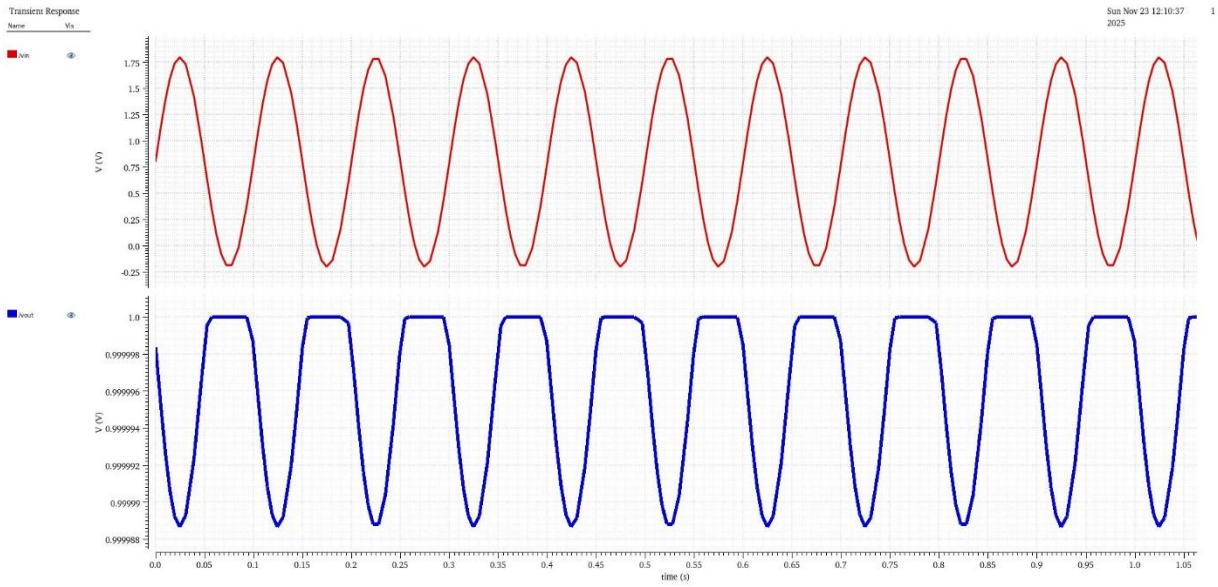
Library Name	Cell Name	Properties
AnalogLib	vdc	Vdd: DC voltage = 1V
AnalogLib	vsin	AC magnitude = 5mV DC voltage = 800.0mV Frequency = 10KHz
gpdk180	R0	R=100 ohm

Simulation:

Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

Transient Response:



Layout:

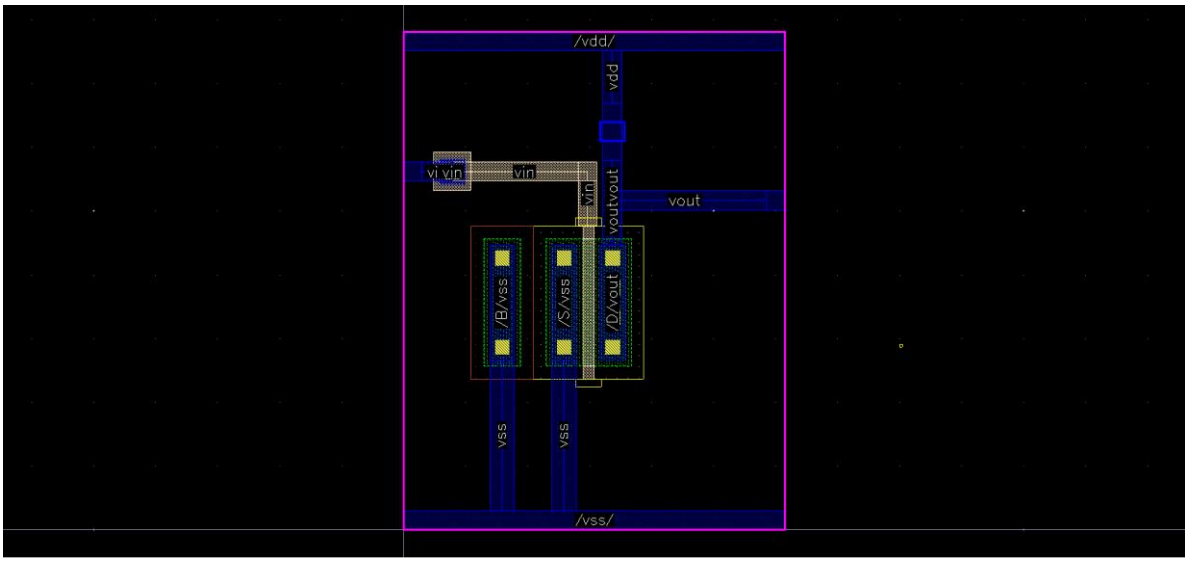


Fig: Common Source with Resistive Load Layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura - Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology - gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura - Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology - gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura - Quantus", select "Technology - gpdk180", "Output - Extracted View" from the "Setup" option, select "Extraction Type - RC" and "Ref Node - VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

Conclusion:

The Common Source amplifier with a resistive load successfully demonstrated voltage amplification with a clear 180° phase inversion between input and output. The circuit operated in the saturation region, and the small-signal gain depended primarily on the MOSFET transconductance and the load resistance. Overall, the experiment verified the fundamental behaviour of the CS configuration as a reliable voltage amplifier with high input impedance and moderate gain.