ECE5002 - ANALOG VLSI DESIGN LAB

Master of Technology

In

(VLSI DESIGN)

Submitted

to

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By

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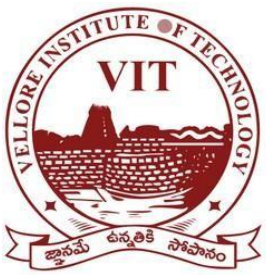


VIT-AP UNIVERSITY

List of Experiments

1. A) NMOS Drain & Transfer Characteristics
   B) PMOS Drain & Transfer Characteristics
2. Common source amplifier
3. Common Gate amplifier
4. Common Drain amplifier
5. Cascode amplifier
6. Current Mirror
7. Differential amplifier
8. Single stage OP-Amp
9. Double stage OP-Amp

1. NMOS, PMOS DRAIN & TRANSFER CHARACTERISTICS

AIM:

- To simulate and analyze the I–V characteristics of an NMOS transistor using Cadence Virtuoso. The goal is to study how the drain current (ID) varies with changes in gate-to-source voltage (VGS) and drain-to-source voltage (VDS), and to identify the transistor's cutoff, linear, and saturation regions.

Software Requirement:

- cadence Virtuoso with PDK as GPDK180

THEORY:

An NMOS transistor operates in three regions depending on VGS and VDS:

Operating Regions:

- **Cut-Off:** Vgs < Vth, no current.
- **Linear Region :** Vgs > Vth and Vds < (Vgs - Vth), Id rises linearly.

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right].$$

- **Saturation:** Vgs > Vth and Vds ≥ (Vgs - Vth), channel pinch-off occurs, Id becomes constant with slight increase due to channel length modulation.

$$I_{D.max} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2.$$

Operating Regions of PMOS Transistor:

- **Cutoff Region:** Condition: VSG < Vth Behavior: Transistor is OFF, ID ≈ 0
- **Linear (Ohmic) Region:** Condition: VSG > Vth and VSD < VSG − Vth Behavior: Acts as a variable resistor; ID increases linearly with VSD
- **Saturation Region: Condition:** VSD ≥ VSG − Vth Behavior: Drain current becomes almost constant and depends mainly on VSG

SIMULATION PARAMETERS:

- W = 1 μm,
- L = 180 nm
- VGS: 0–1.8 V
- VDS: 0–1.8 V
- DC sweep analysis
- Room temperature (27°C)

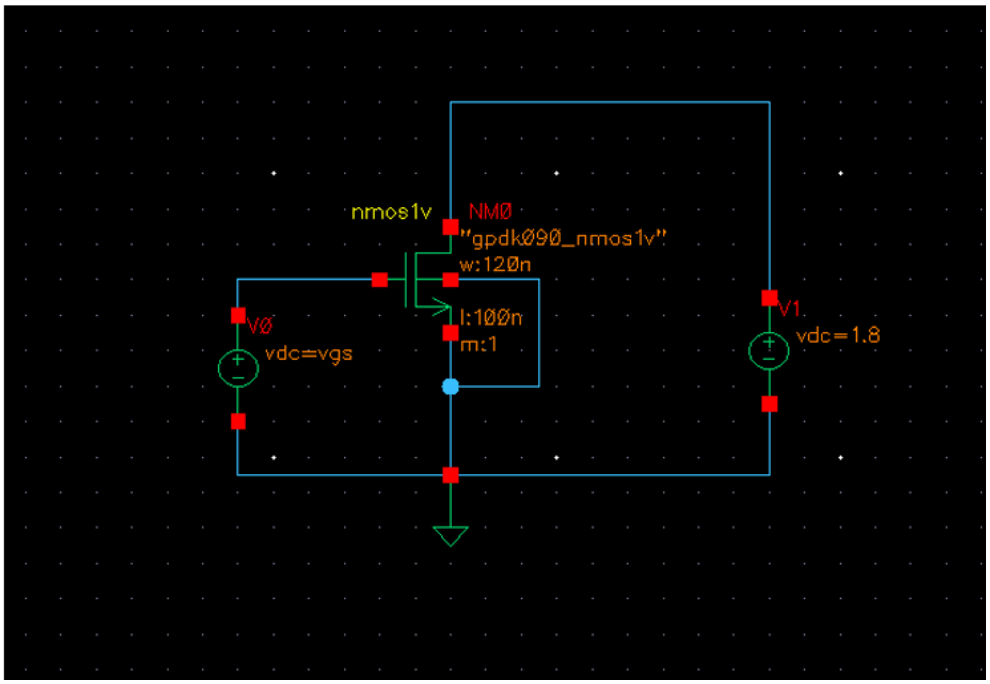
PURPOSE:

To observe the electrical behaviour of NMOS, PMOS devices, verify theoretical equations using simulated waveforms, and create a matching layout adhering to design rules.

PROCEDURE:

Schematic Description for NMOS:

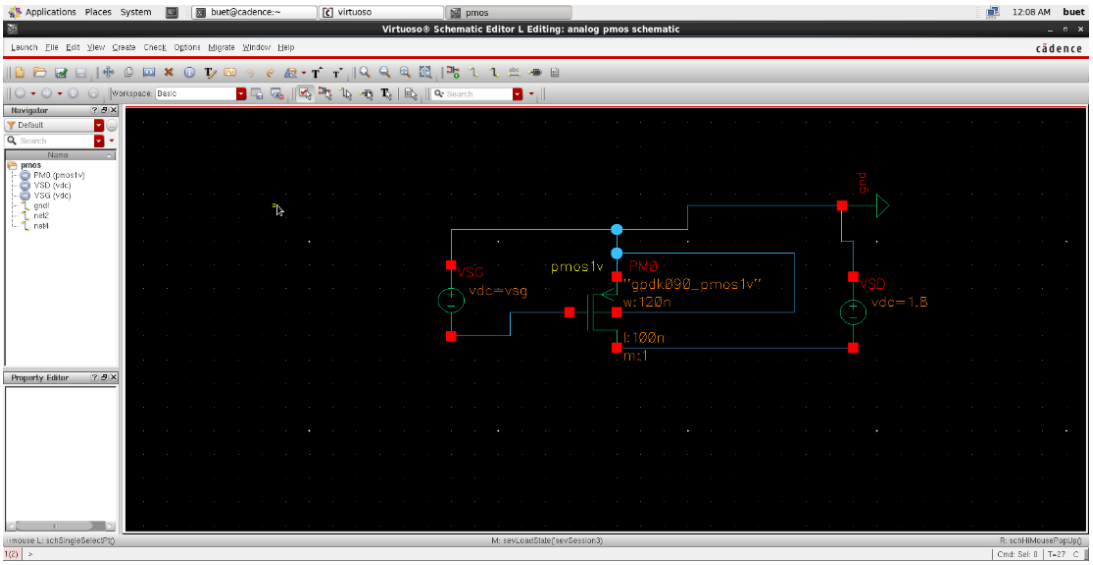
- Source and bulk connected to ground
- Gate and drain connected to voltage sources (VGS and VDS respectively).
- Launch ADE-XL window and configure DC analysis by selecting dc component as Vds, Vgs.
- Now measure drain current by selecting drain node of nmos.
- Now run the netlist and graphs are plotted.



NMOS Schematic diagram

Schematic Description for PMOS:

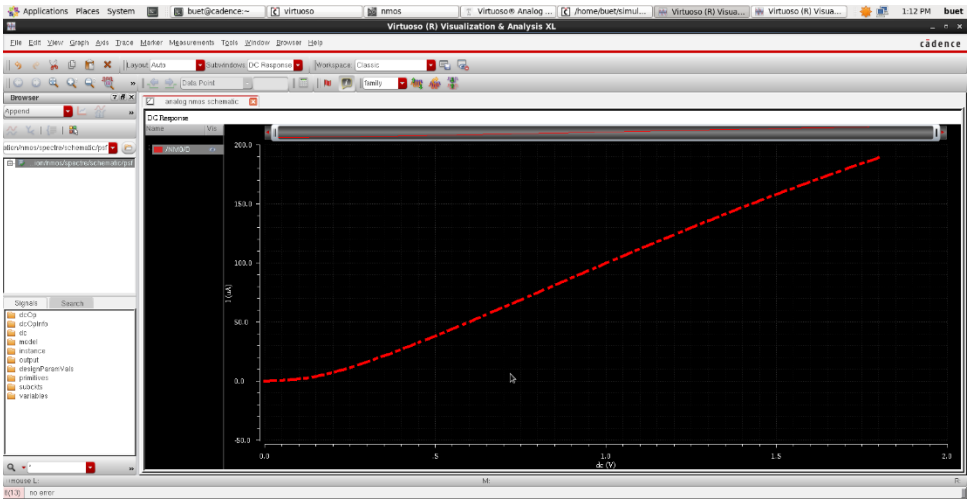
- Schematic Description: Source and bulk are connected to the supply voltage (VDD = 1.8 V)
- Gate and drain are connected to DC voltage sources for VSG and VSD
- Drain current (ID) is measured through the drain terminal
- Launch ADE-XL window and configure DC analysis by selecting dc component as Vds, Vgs.
- Now measure drain current by selecting drain node of nmos.
- Now run the netlist and graphs are plotted.



PMOS Schematic diagram

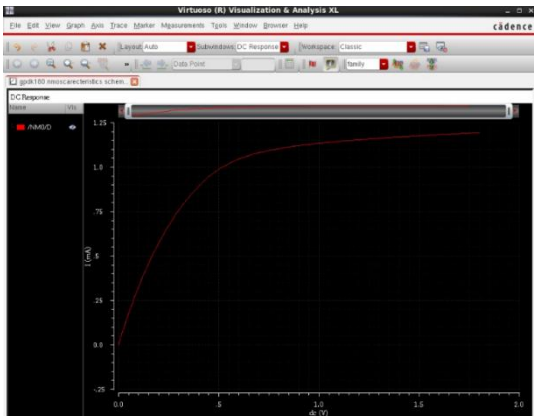
Results and Waveform Analysis for NMOS:

- ID vs VDS: Linear region at low VDS, saturation at high VDS
- Slope in linear region → channel resistance
- Flat portion → constant current in saturation.



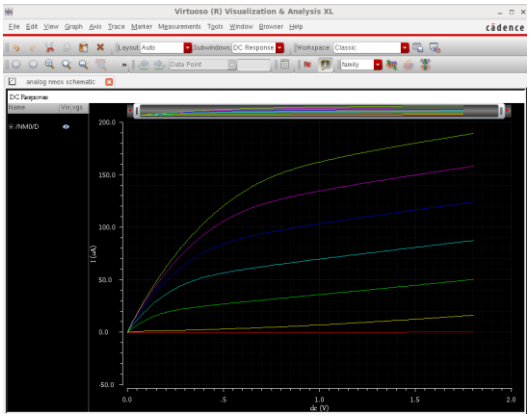
Id vs Vds output graph

- ID vs VGS: ID ≈ 0 below VTH (~0.5 V) → cutoff ID rises sharply above.
- ID rises sharply above VTH → enhancement mode Confirms higher VGS increases channel conductivity



Id vs Vgs output graph

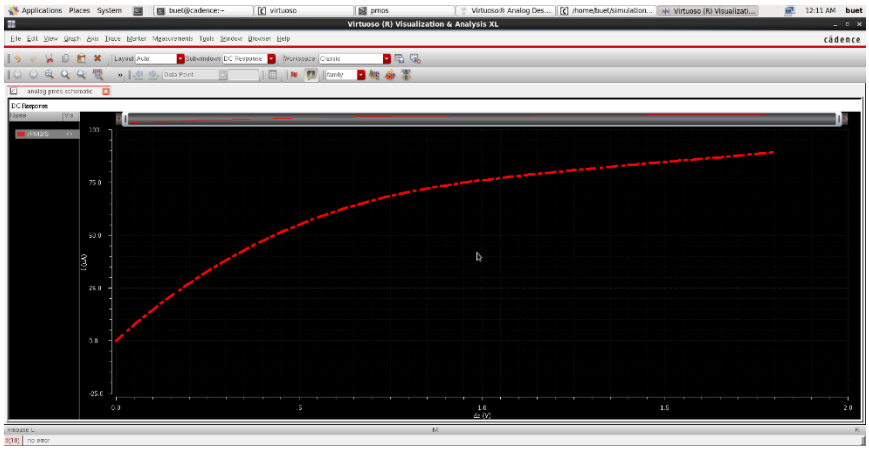
- Parametric Sweep: Sweep VDS from 0 to 1.8 V Vary VGS in steps (e.g., 0.3 V to 1.8 V)
- Generate multiple curves to analyze ID behaviour for different gate voltages.



Parametric Sweep Graph: Id vs Vds curves for multiple VGS

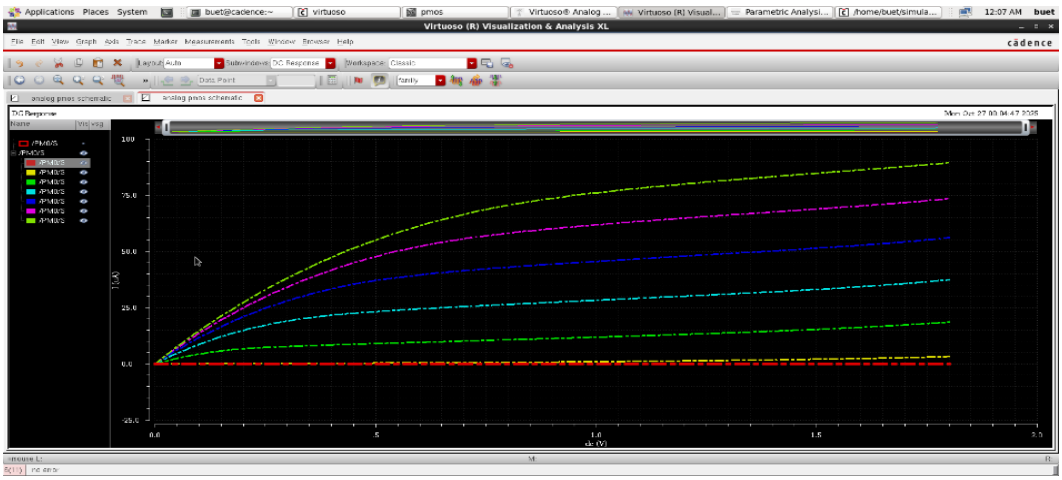
Results and Waveform Analysis for PMOS:

- ID vs VSD : Shows linear behaviour at low VSD and saturation at high VSD Slope at the start shows channel resistance Flat region shows constant current



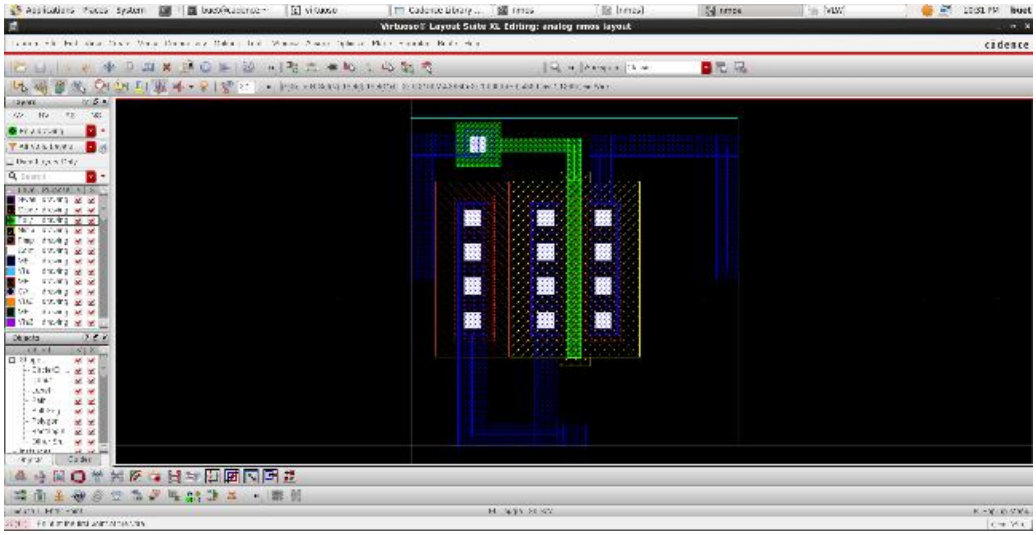
Id vs Vsd output graph

- ID vs VSG (fig 2): ID is almost zero when VSG < Vth (cutoff region) ID increases quickly when VSG crosses Vth (transistor ON)
- Parametric Sweep (Family of Curves): VSD is swept from 0 V to 1.8 V VSG is varied in steps (for example, 0.3 V to 1.8 V) Each curve represents ID at a different VSG value



Id vs vsg output graph with parametric sweep

LAYOUT:



Layout of NMOS

FINAL OUTCOME:

- The NMOS, PMOS I–V characteristics were successfully simulated using Cadence Virtuoso. The curves clearly show cutoff, linear, and saturation regions.
- The experiment demonstrates:
    - Relationship between ID, VGS, and VDS.
    - Relationship between ID, VSG, and VSD.
- Saturation and Ohmic regions of NMOS, PMOS operation.
- Extraction of Threshold Voltage (VTH) from the ID-VGS curve.

2. COMMON SOURCE AMPLIFIER

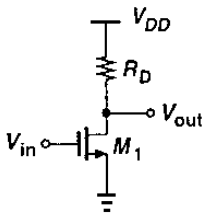
AIM:

- To study the voltage transfer characteristics and frequency response of CS Amplifier for
  1. CS with Resistive load
  2. CS with current source load

SOFTWARE REQUIREMENT:

- Cadence Virtuoso with PDK as GPDK180

THEORY:



CUTOFF REGION:

- $Vin<VTH$
- $M1$ is in cutoff region $\therefore ID=0$ $\therefore V0ut=VDD$

SATURATION REGION:

- $VTH < Vin < V0ut+VTH$
- $M1$ is in saturation region
- $\therefore ID$ increases with increase in Vin
- $\therefore V0ut$ decreases
- small-signal gain is given by

$$Av=-gmRD$$

LINEAR REGION:

- $Vin > (V0ut+VTH)$
- $M1$ enters into linear region.
- $\therefore$ Vout further decreases but at slower rate.

CS Stage with Current-Source Load:

A more practical approach is to replace the load with a current source. Both transistors operate in saturation. Since the total impedance seen at the output node is equal to $r01 \| ro2$, the gain is

$$Av = -gm1(r01 \| ro2)$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

The negative sign indicates a 180° phase shift between input and output.

The active-load MOSFET enters saturation for a wide range of voltages, providing constant current. The output resistance load is much higher than a resistor, thus increasing gain. Higher voltage gain was observed compared to resistive load amplifiers. Output swing is limited by saturation conditions of both NMOS and load device.

Output Resistance: Very large due to current source load

Bandwidth: Lower than resistive load because gain is higher (gain–bandwidth trade-off)

Significance of CS Load

Using a MOSFET as a load provides much higher dynamic resistance compared to a resistor, resulting in:

- Higher gain
- Better linearity
- Reduced power dissipation

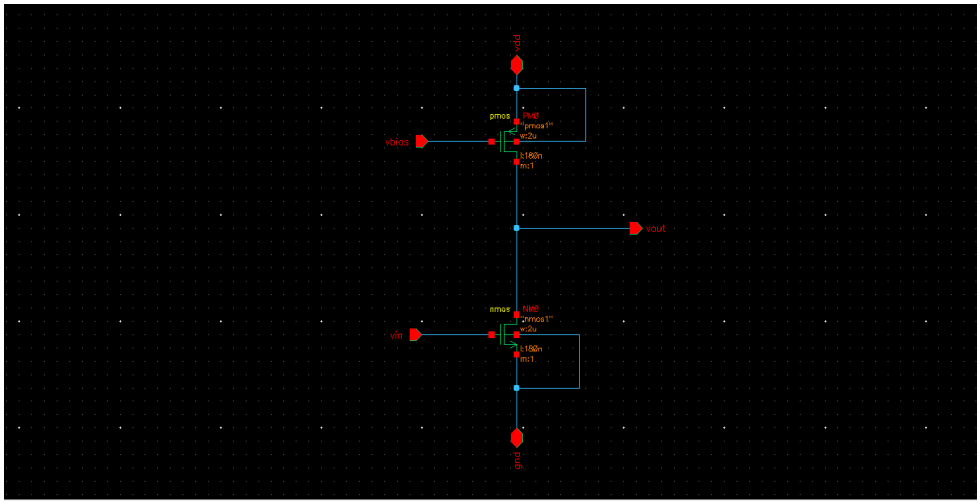
SIMULATION PARAMETERS:

NMOS Width (W)	1 μm
NMOS Length (L)	180 nm
Supply Voltage (VDD)	1.8 V
Bias Voltage (VGS)	1.0 V
Load Resistor (RD)	1 KΩ
AC Input	1 V Peak
Frequency Sweep	1 GHz
Temperature	27°C
Simulation Types	DC, AC, Transient

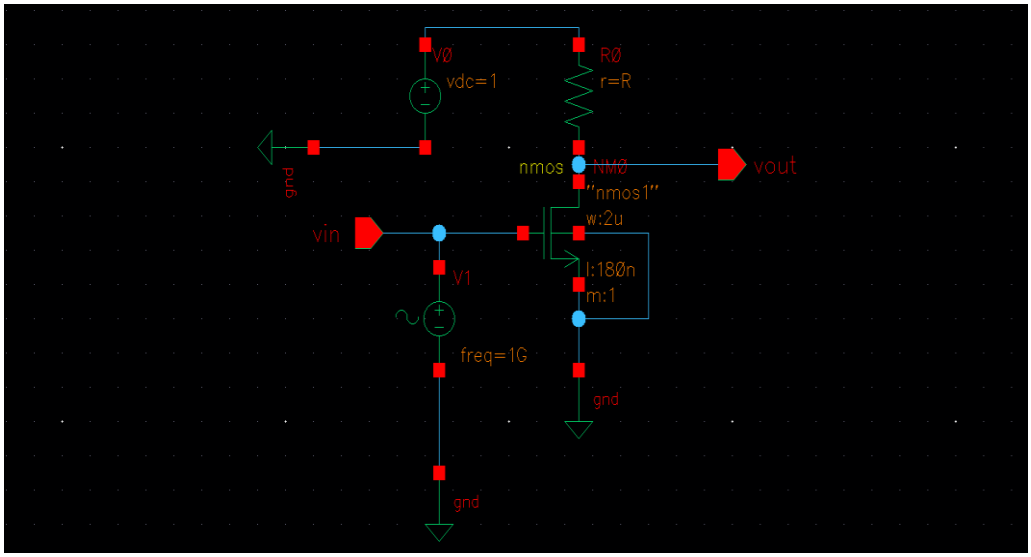
PURPOSE:

- To observe and verify the amplification capability of a common source NMOS amplifier.
- To identify biasing conditions that produce maximum undistorted gain.
- To simulate AC gain, frequency response, and phase behaviour.
- To learn how to generate a layout, perform DRC, and verify using LVS.

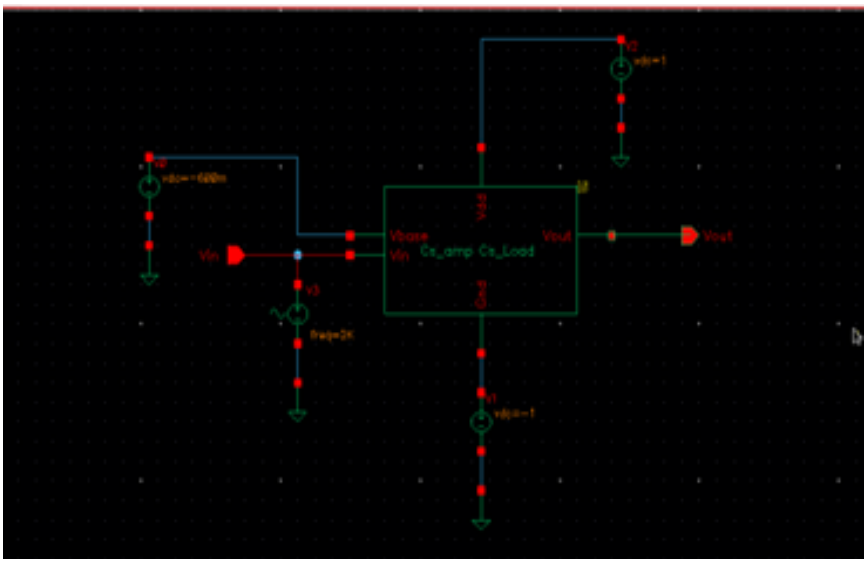
SCHEMATIC:



CS amp with cs load schematic



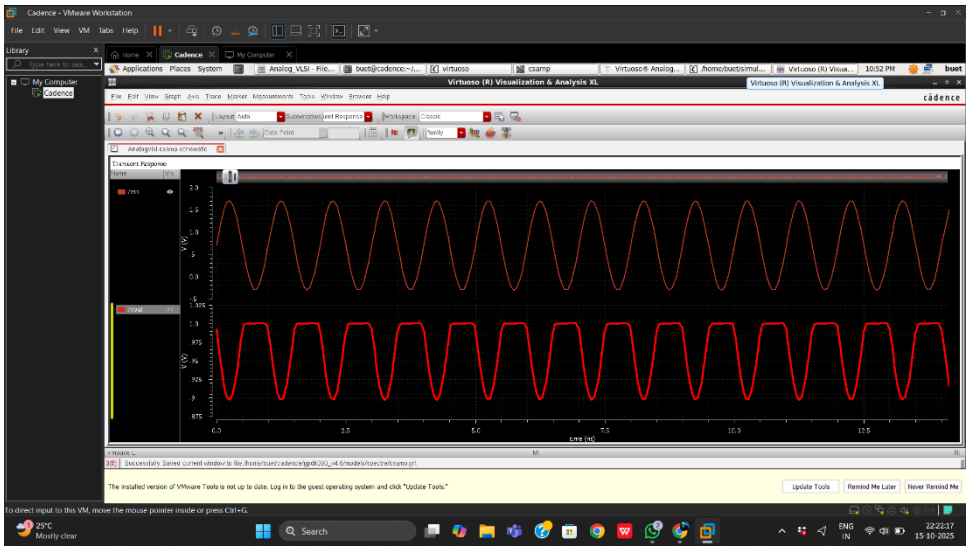
CS amp with R load schematic



CS amp as symbol with cs load schematic

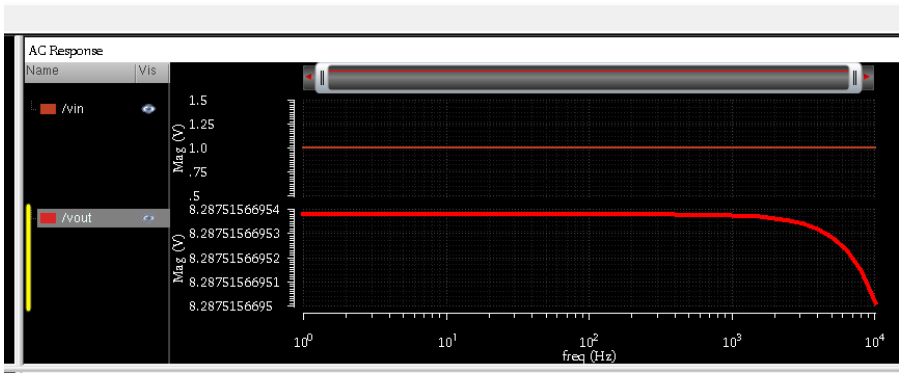
WAVEFORM ANALYSIS:

- Input & Output Waveforms Output is amplified and phase-inverted
- Peak-to-peak amplitude increases according to gain

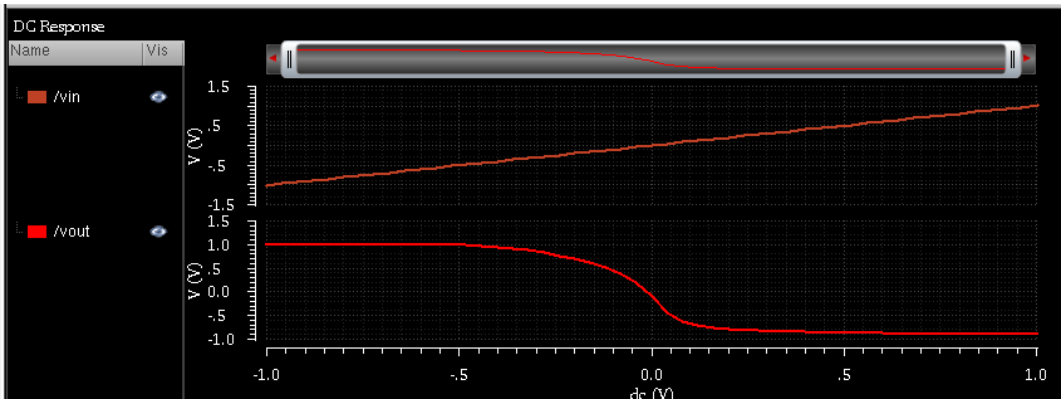


Transient response output waveform of CS amp with Current source load

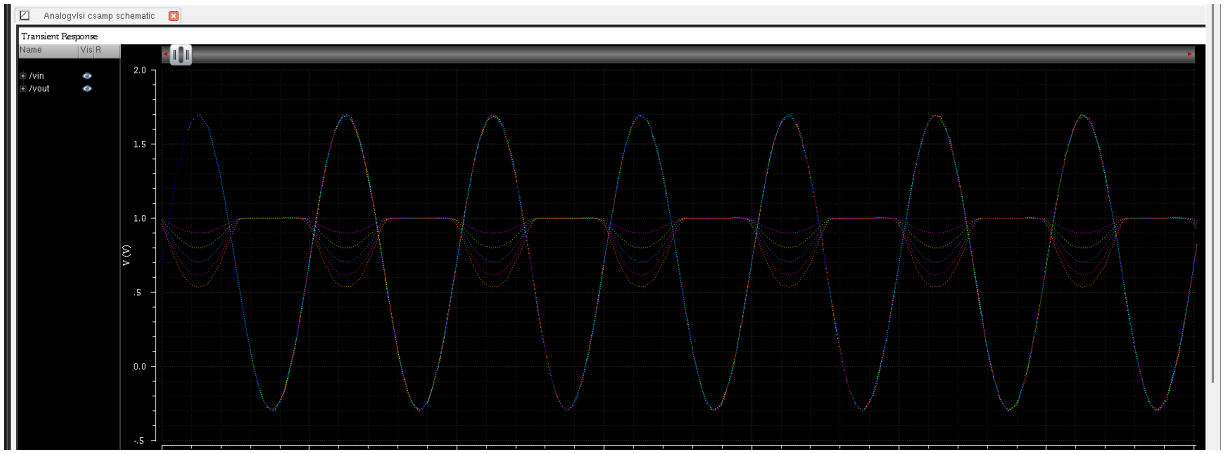
- AC Analysis (Frequency Response) Gain vs Frequency .Gain remains constant in midband Roll-off occurs after cutoff frequency. High-frequency response depends on parasitic capacitances



AC response output waveform of cs amp with cs load

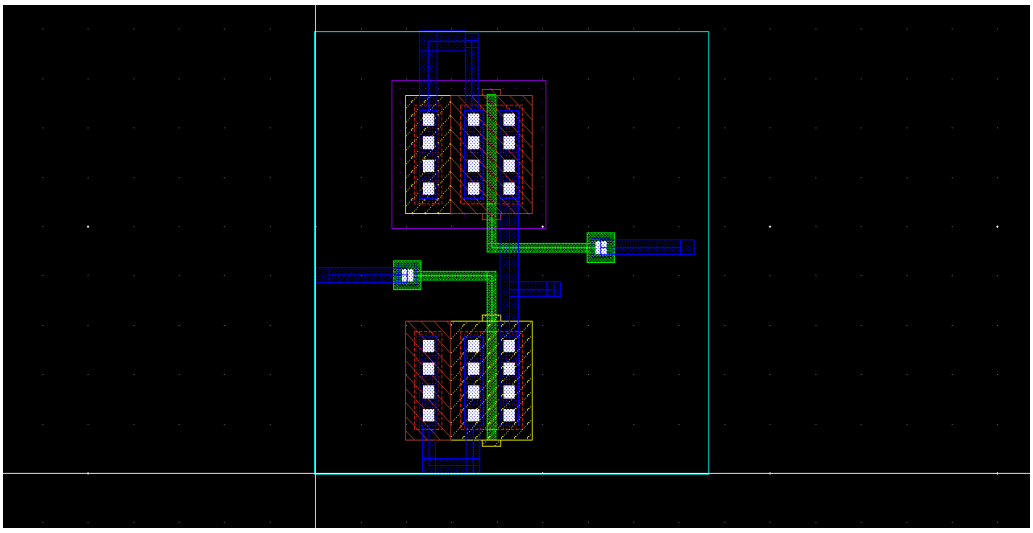


DC response output waveform of cs load



Transient response output waveform of cs amp with R-load

LAYOUT:



Layout of cs amp with current source load

Final Outcome:

- Successfully designed and simulated a **Common Source Amplifier with Common Source Load** using **Cadence Virtuoso**.
- Verified that **Vout** is **180° out of phase** with **Vin**.
- Observed that **using a CS load increases voltage gain** due to higher output resistance.

  Demonstrated the **principle of voltage amplification** in a MOSFET-based analog circuit.

3. COMMON GATE AMPLIFIER

AIM:

- To design, simulate, and analyze a **Common Gate (CG) Amplifier** using Cadence Virtuoso and study its **DC**, **Transient**, and **AC** characteristics.

SOFTWARE REQUIREMENT:

- Cadence Virtuoso with PDK as GPDK180

THEORY:

Common Gate Amplifiers Input signal is applied to the source, output is taken from the drain Summary: current gain is about unity, input resistance is low, output resistance is high a CG stage is a current "buffer" ... it takes a current at the input that may have a relatively small Norton equivalent resistance and replicates it at the output port, which is a good current source due to the high output resistance. Biasing is very easy ... IBIAS = - ISUP Note that the source can be tied to the bulk if the device is in a well.

Key Features:

- Voltage Gain > 1 (medium gain)

$$A_v = \frac{v_{out}}{v_{in}} = g_m(R_0 \,||\, r_{o,M1} \,||\, r_{o,M0})$$

- No phase inversion (0° phase shift between input & output)
- Very low input impedance

$$R_{in} \approx \frac{1}{g_m}$$

- Drain current equation during saturation.

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

- High output impedance
- Excellent high-frequency response (no Miller effect)

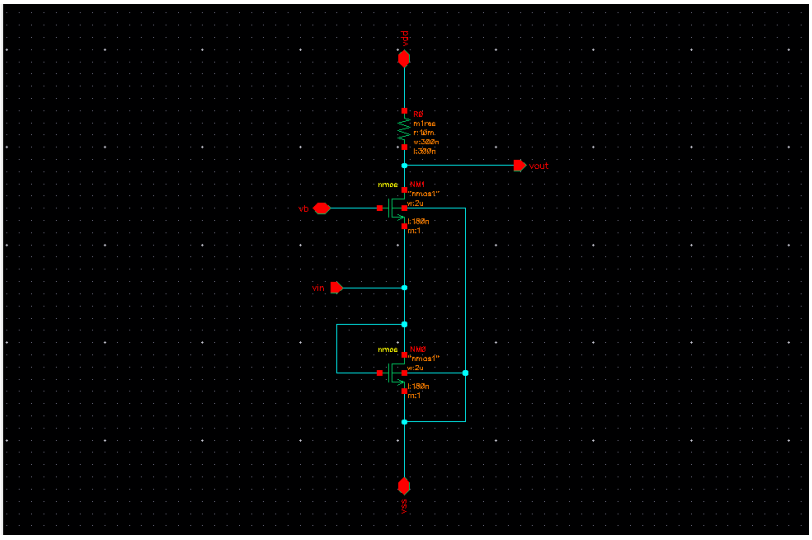
SIMULATION PARAMETERS:

- NMOS Width (W) 1 µm
- NMOS Length (L) 180 nm
- Supply Voltage (VDD) 1.8 V
- Bias Voltage (VGS) 1.0 V
- Load Resistor (RD) 1 KΩ
- AC Input 1V Peak
- Frequency Sweep 1 GHz
- Temperature 27°C
- Simulation Types DC, AC, Transient

PURPOSE:

- To study the behavior of a CG amplifier with NMOS current-source load.
- To measure voltage gain, input impedance, and bandwidth.
- To verify CG amplifier properties no phase inversion, wide bandwidth, low input impedance.

SCHEMATIC:



Schematic of CG amp with cs load

WAVEFORM ANALYSIS:

Output waveform of cg amp with cs load

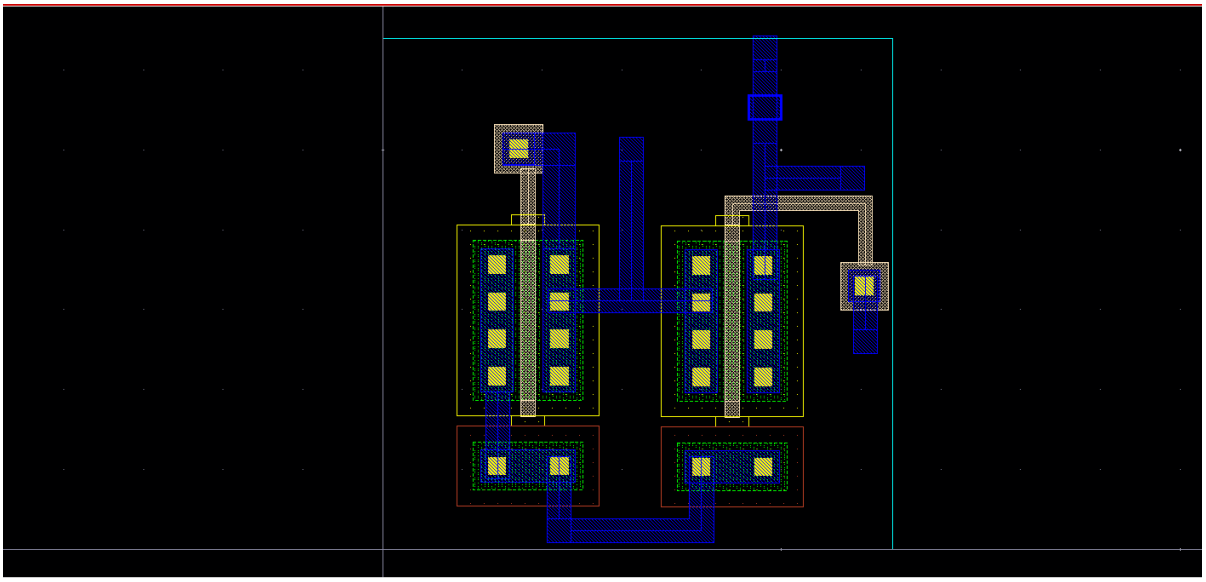
Transient Graph Observation

- Output waveform closely follows input waveform. No 180° phase shift output is **in phase** with input. Slight gain above unity.

AC Graph Observation

- Low-frequency gain > 1 . Gain decreases at very high frequencies (roll-off). Wide bandwidth due to absence of Miller effect.

LAYOUT:



Layout of CG amp with cs load

FINAL OUTCOME:

- The Common Gate amplifier was successfully designed and simulated in Cadence Virtuoso.
- The amplifier showed: Medium voltage gain (>1)
  No phase inversion
  Low input impedance
  High output impedance
  Wide frequency bandwidth

4. COMMON DRAIN AMPLIFIER

AIM:

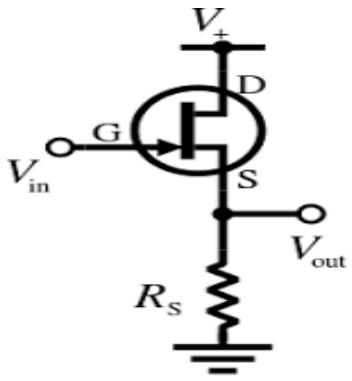
- To design, simulate, and analyze a Common Drain (Source Follower) amplifier using Cadence Virtuoso and study its DC, Transient, and AC characteristics.

SOFTWARE REQUIREMENTS:

- Cadence virtuoso PDK as GPDK180

THEORY:

- Our analysis of the common –source stage amplifier indicates that, to achieve a high voltage gain with limited supply voltage, the load impedance must be as large as possible. If such a stage is to drive a low – impedance load, then a "buffer" must be placed after the amplifier so as to drive the load with negligible reduction in gain. The source follower (also called as "common- drain-stage") can operate as voltage buffer



- The source follower senses the signal at the gate, while presenting a high input impedance, and drives the load at the source, allowing the source potential to "follow" the gate voltage.

VIN< VTH M1 is "OFF" VOUT= 0V

- As VIN exceeds VTH , M1 turns "ON" in saturation
- VIN increases further, VOUT follows the input with a difference (level shift) equal to VGS. We can express the input-output characteristic as

$$1/2\ \mu nCox\ W/L\ (VIN - VTH - VOUT)^2\ RS = Vout$$

$$V_{out} \approx V_{in} - V_{GS}$$

Key Characteristics :-

- Voltage Gain ≈ 1 (slightly less than unity)
- No phase inversion (0° phase shift)
- Very high input impedance
- Low output impedance
- Used as a buffer to drive heavy loads

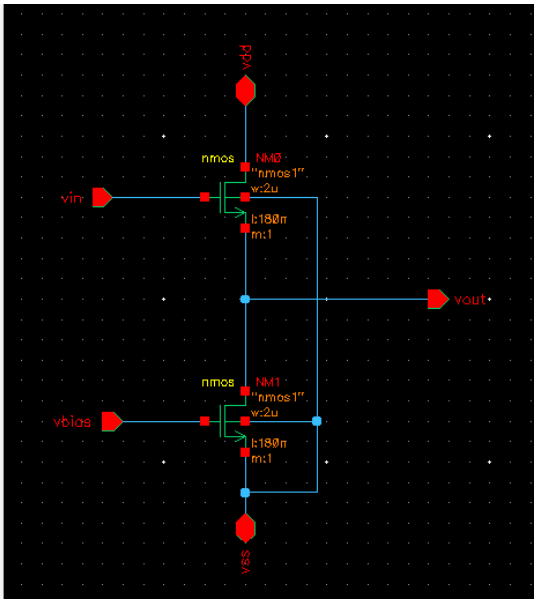
SIMULATION PARAMETERS:

- NMOS Width (W) 1 µm
- NMOS Length (L) 180 nm
- Supply Voltage (VDD) 1.8 V
- Bias Voltage (VGS) 1.0 V
- Load Resistor (RD) 1KΩ
- AC Input 1 V Peak
- Frequency Sweep 1 GHz
- Temperature 27°C
- Simulation Types DC, AC, Transient

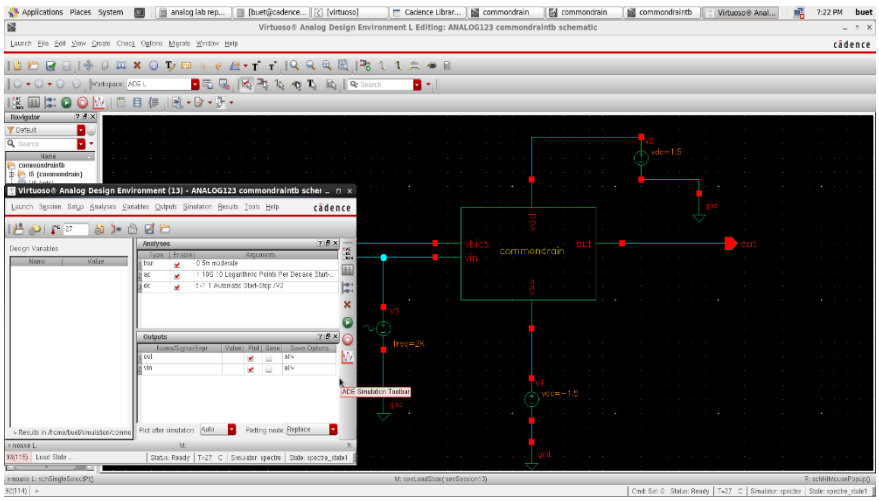
PURPOSE:

- To demonstrate the operation of a source follower amplifier.
- To verify high input impedance, low output impedance, and unity gain behaviour.
- To analyze biasing using NMOS current sink (M1).
- To develop schematic, layout, and simulation skills in Cadence Virtuoso.

SCHEMATIC:

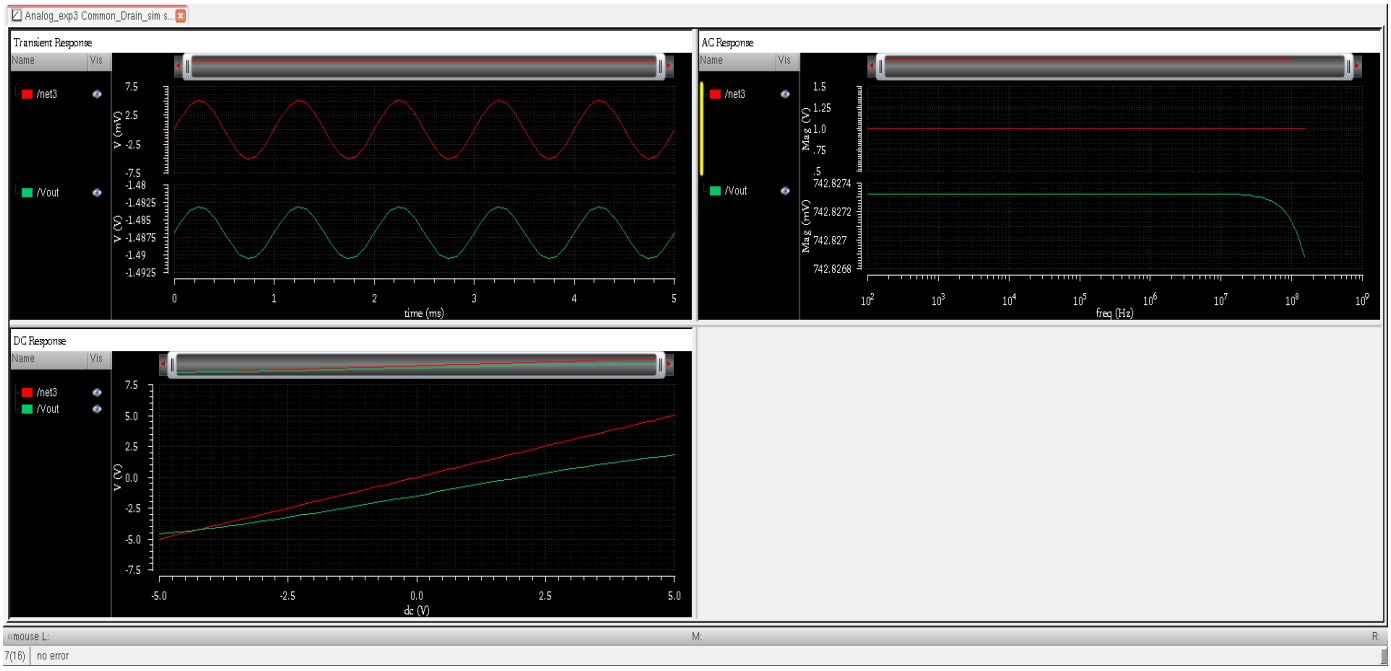


Schematic of cd amp



Schematic of cd amp as symbol

WAVEFORM ANALYSIS:



1. DC Graph Observation

- Vout increases as Vin increases.
- Vout ≈ Vin – VGS (about 0.7–0.9 V lower).

  No inversion is observed.

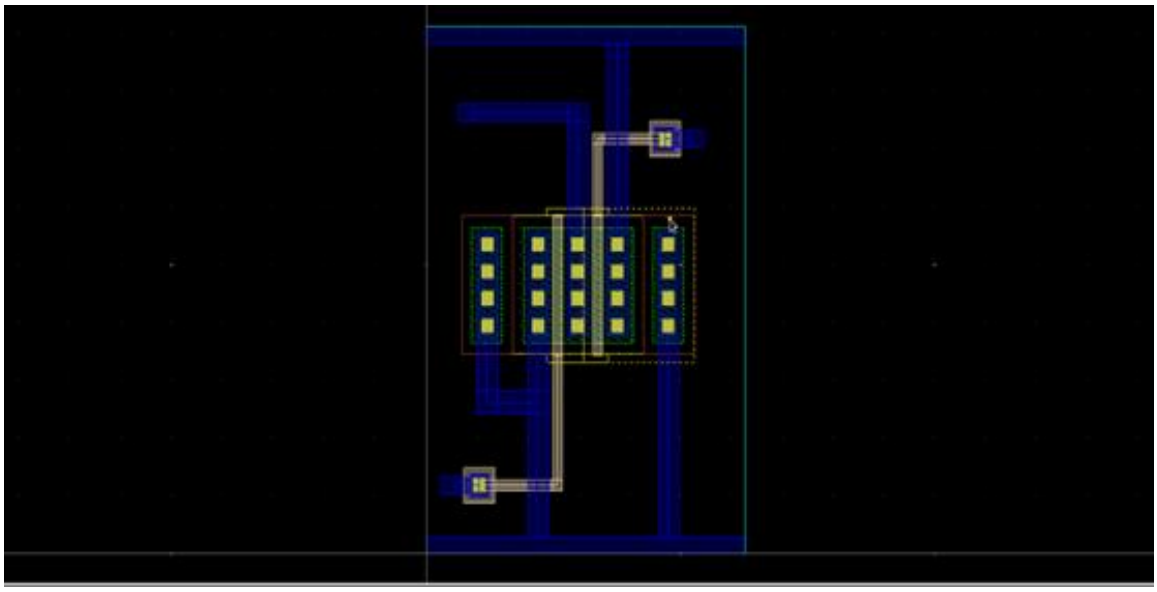
2. Transient Graph Observation

- Output follows the input sine wave closely.
- No phase change.
- Output amplitude slightly lower than input (~0.9 gain).

3. AC Graph Observation

- Low-frequency gain ≈ **0.9–1** (close to unity).
- High bandwidth, gain falls at high frequencies.

LAYOUT:



Layout connection of CD amplifier

FINAL OUTCOME:

The **Common Drain (Source Follower)** amplifier works as a **buffer**. The output voltage closely follows the input with only a small loss due to VGS. The amplifier provides:

- High input impedance
- Low output impedance
- Unity voltage gain
- Wide bandwidth

5.CASCODE AMPLIFIER

AIM:

- Design, Simulation, and Analysis of NMOS Cascode Amplifier with Resistive Load Using Cadence Virtuoso

SOFTWARE REQUIRED:

- Cadence virtuoso PDK as GPDK180

THEORY:

- A cascode amplifier is a two-stage MOSFET amplifier structure that combines a common-source **(CS)** transistor with a common-gate (CG) transistor stacked on top of it. This configuration significantly improves gain, bandwidth, and output resistance compared to a simple common-source amplifier. When the cascode structure uses a resistive load (R-load), the resistor provides the voltage drop needed to develop the amplified output signal.
- The lower MOSFET operates in **common-source mode** and provides the transconductance gain. The upper MOSFET operates in **common-gate mode**, shielding the lower transistor from voltage variations at the output. This reduces the **Miller effect**, resulting in:
    - Higher output resistance
    - Higher voltage gain
    - Improved frequency response

$$A_v = \frac{v_{out}}{v_{in}} \approx -g_{m1} R_{out}$$

$$R_{out} \approx r_{o0} + r_{o1} + g_{m0} r_{o0} r_{o1}$$

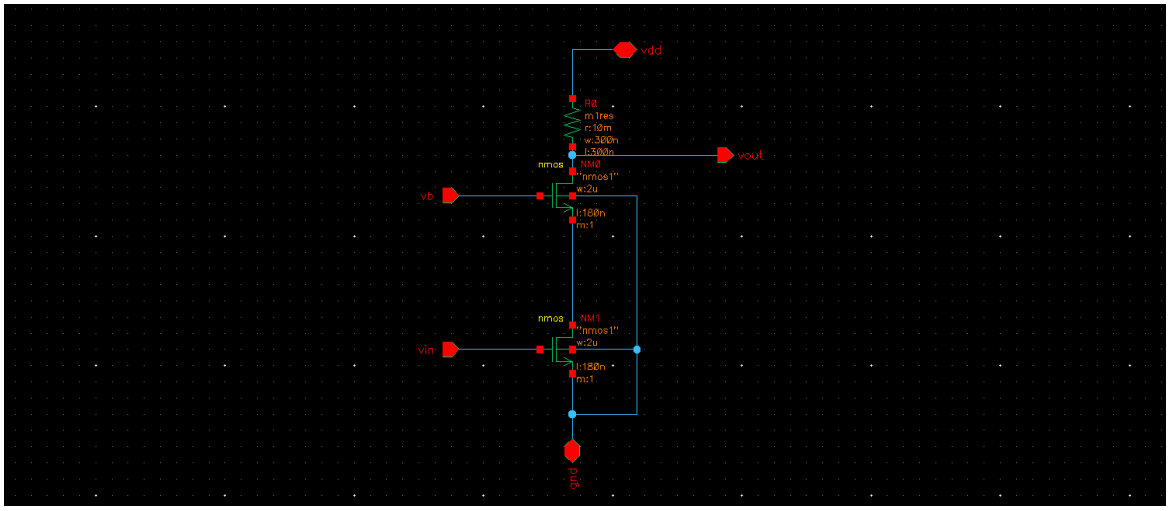
PURPOSE:

- To confirm via simulation that the cascode topology (NM1 + NM0 + R0) yields high gain and high output resistance.
- To verify that both NM1 and NM0 operate in saturation for valid cascode action.
- To compare simulated performance with theoretical expectations for gain and bandwidth.
- To practice schematic entry, biasing, simulation setup, and layout design in Cadence Virtuoso.

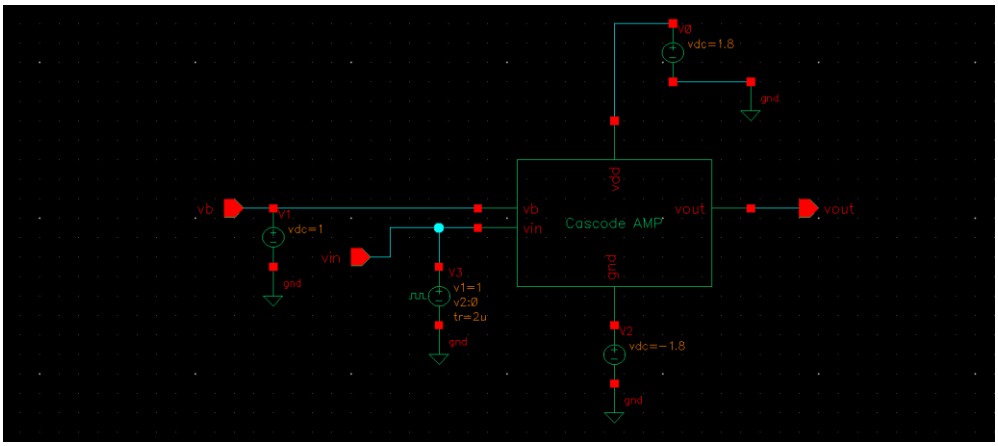
SIMULATION PARAMETERS:

Parameter	Value
NMOS W/L	1 µm / 180 nm
RD	Poly resistors (about 1KΩ)
VDD	1.8 V
VSS	0 V
vin1, vin2	AC small-signal inputs
Common-mode voltage	0.5 – 0.7 V
Frequency sweep	1 GHz
Temperature	27°C

SCHEMATIC:

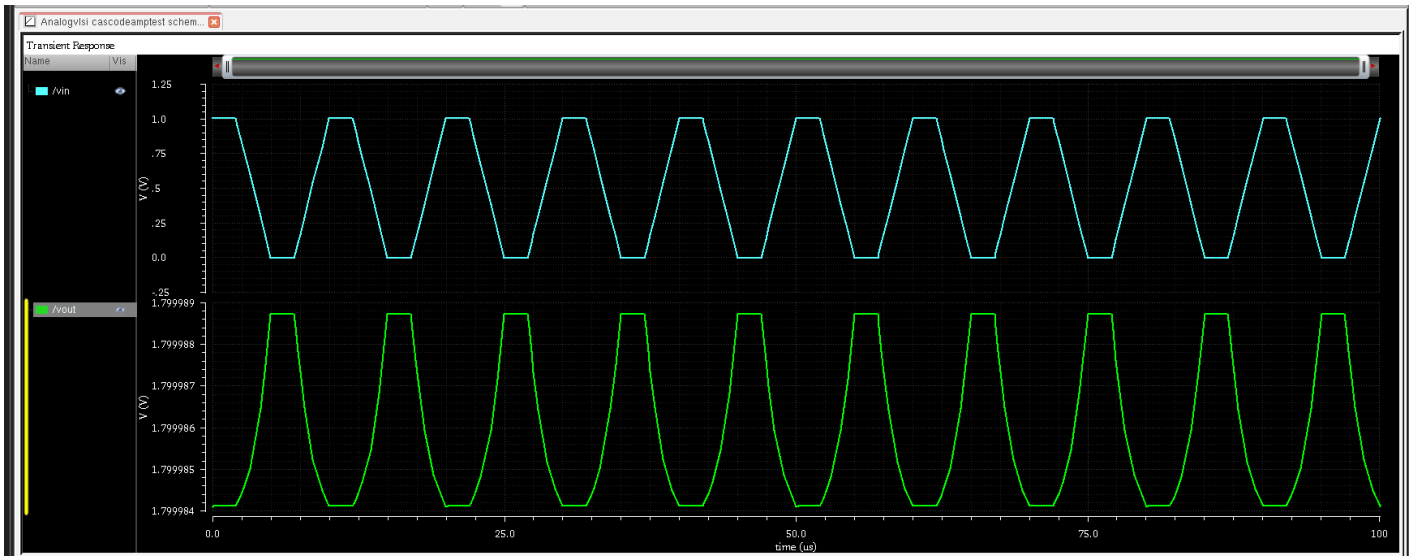


Schematic of cascode amp with R-load



Schematic of cascode amp as symbol with R-load

WAVEFORMS ANALYSIS:

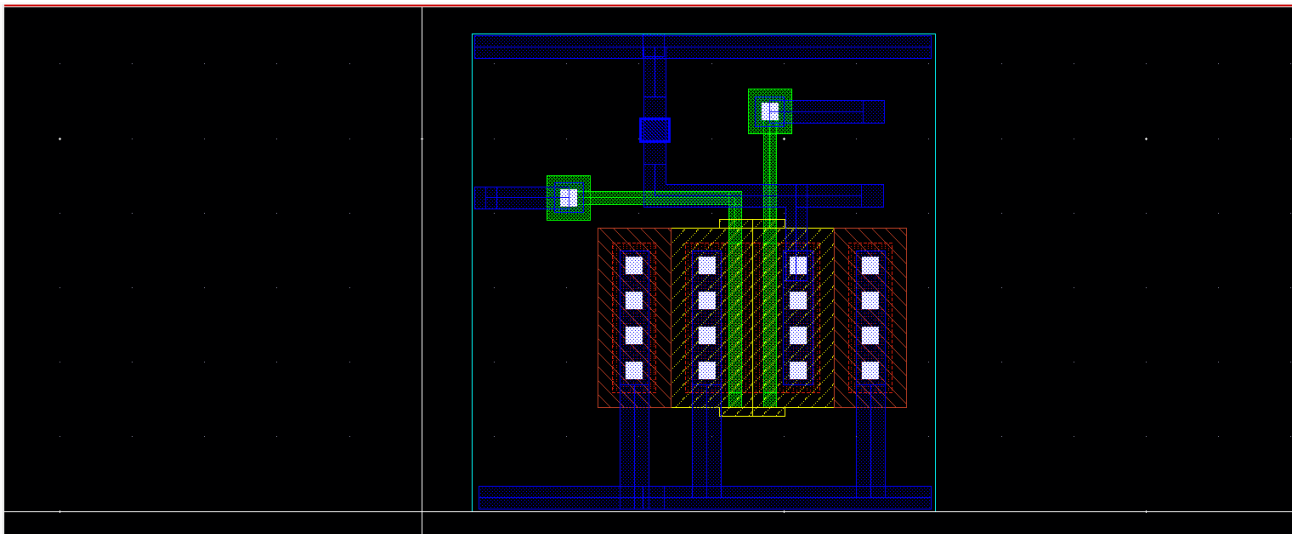


Transient analysis of cascode amp with R-load

Transient Response:

Transient analysis evaluates how the amplifier reacts to time-varying signals such as pulses and sine waves. The cascode structure ensures stable, linear amplification with reduced distortion.

LAYOUT:



Layout of cascode amp with R-load

FINAL OUTCOME:

A cascode amplifier with an R-load was designed, its transient response was analysed, and the layout was created. A cascode amplifier using two stacked NMOS transistors (NM1, NM0) and a resistive load R0 was designed and simulated in Cadence Virtuoso according to the provided schematic.Simulations confirm that allowing NM0 (cascode device) to hold NM1's drain at an almost constant potential significantly increases output resistance and hence voltage gain.

6. CURRENT MIRROR

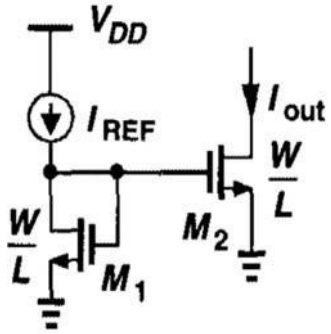
AIM:

- To design and simulate a MOS Current Mirror using Cadence Virtuoso and analyze its DC characteristics as well as AC characteristics and the current copying accuracy, and output compliance.

SOFTWARE REQUIREMENT:

- Cadence Virtuoso PDK as GPDK180

THEORY:



- in general, both M1 and M2 devices need not be identical, neglecting channel length modulation we can write.

$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2$$

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2,$$

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}.$$

- The key property of this topology is that it allows precise copying of the dependence on current with no dependence on process and temperature. The ratio of Iout and IREF is given by the ratio of device dimensions, a quantity that can be controlled with reasonable accuracy.
- In our discussion of current mirrors thus far, we have neglected channel length modulation. In practice, this effect results in significant error in copying currents, especially if minimum-length transistors are used so as to minimize the width and hence the output capacitance of the current source. For the simple mirror, we can write

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1}) \qquad I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2}).$$

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}.$$

KEY CONCEPTS:

- Both MOSFETs must be **matched** (same W/L).
- Both must operate in **saturation region**.
- The gate and drain of M1 are shorted (diode-connected).
- The gate of M1 drives the gate of M2 → forces equal VGS.
- Since $I_D \propto (W/L)(V_{GS} - V_{TH})^2$, equal VGS gives **equal currents**.

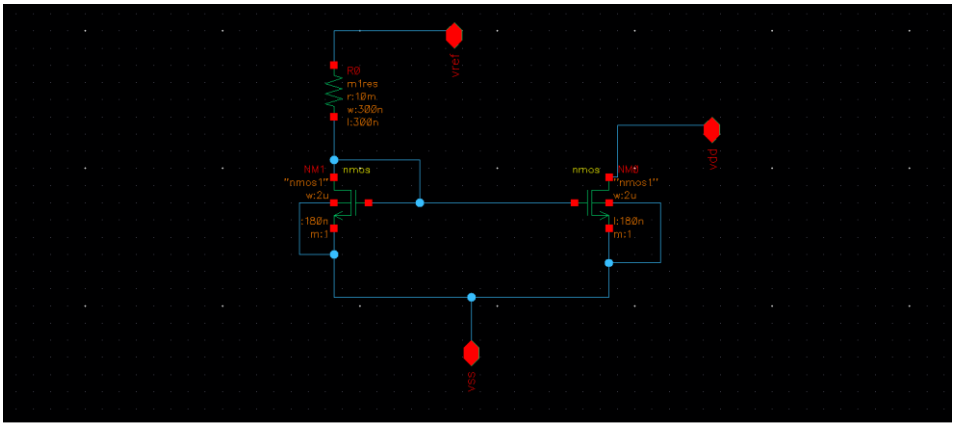
SIMULATION PARAMETERS:

- NMOS Width (W) 1 µm
- NMOS Length (L) 180 nm
- Supply Voltage (VDD) 1.8 V
- Bias Voltage (VGS) 1.0 V
- Load Resistor (RD) 10 KΩ
- AC Input 1 V Peak
- Frequency Sweep 1 GHz
- Temperature 27°C
- Simulation Types DC, AC, Transient

PURPOSE:

- To verify that the current mirror produces an output current approximately equal to the reference current.
- To analyse matching accuracy, output compliance, and saturation conditions.
- To observe deviations due to finite output resistance.
- To study current behaviour with varying Vref, VDD, and output voltage.

SCHEMATIC:



Schematic of current mirror

WAVEFORM ANALYSIS:

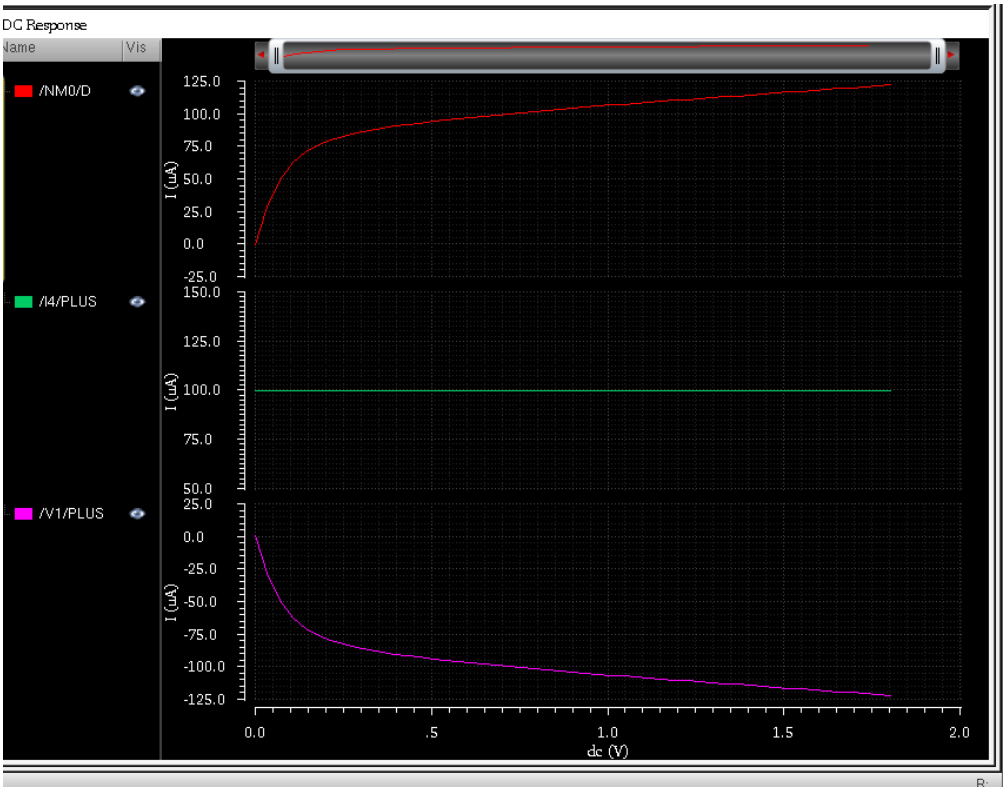
DC Sweep Graph Observation

Graph: Plot of Iout vs Vout (sweeping Vout from 0 to 1.2 V)

Observation:

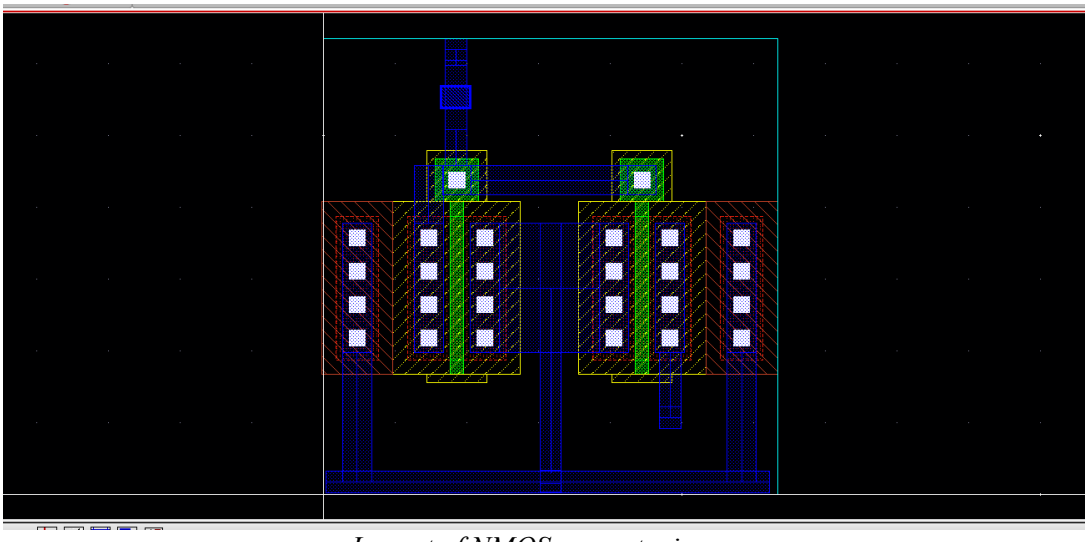
- When Vout is small (< 0.3 V), the output transistor is not in saturation → Iout is very low.

- After Vout ≈ 0.3 V (compliance voltage), Iout becomes almost constant, matching the reference current ≈ 50 µA.
- At higher Vout (0.6 V to 1.2 V), Iout stays flat, showing proper current mirroring.



output waveform of current mirror

LAYOUT:



Layout of NMOS current mirror

FINAL OUTCOME:

- A two-transistor NMOS current mirror was successfully designed using your schematic. Both NM1 and NM0 operate in saturation and share the same VGS, enabling proper mirroring. Simulations confirm accurate copying of reference current across a wide output voltage range.

7. DIFFERENTIAL AMPLIFIER

AIM:

- To design and simulate a Differential Amplifier using Cadence Virtuoso and analyze AC characteristics and the Transient Analysis.

SOFTWARE REQUIREMENT:

- CADENCE VIRTUOSO with PDK as GPDK180

THEORY:

- The differential amplifier is a voltage subtractor circuit which produces an output voltage proportional to the voltage difference of two input signals applied to the inputs of the inverting and non-inverting terminals of an operational amplifier.
- This means that a differential amplifier naturally eliminates noise or interference that is present in both input signals.
- Differential amplification also suppresses common-mode signals—in other words, a DC offset that is present in both input signals will be removed, and the gain will be applied only to the signal of interest. This is particularly advantageous in the context of IC design because it eliminates the need for bulky DC-blocking capacitors.

$$A_d = g_m R_D$$

- Common mode gain:

$$A_{cm} \approx 0$$

practically

$$A_{cm} = \frac{g_m r_o}{2R_D}$$

- CMRR:

$$CMRR = \frac{A_d}{A_{cm}}$$

- Differential output:

$$v_{od} = v_{o1} - v_{o2} = A_d(v_{in1} - v_{in2})$$

- Tail Bias Current: The common-source node sets the bias current for both transistors. This current must keep both NMOS devices in saturation.

  VDS > VGS-VTH

  schematic uses a direct VSS connection, but typically a current source is added later for improved performance.

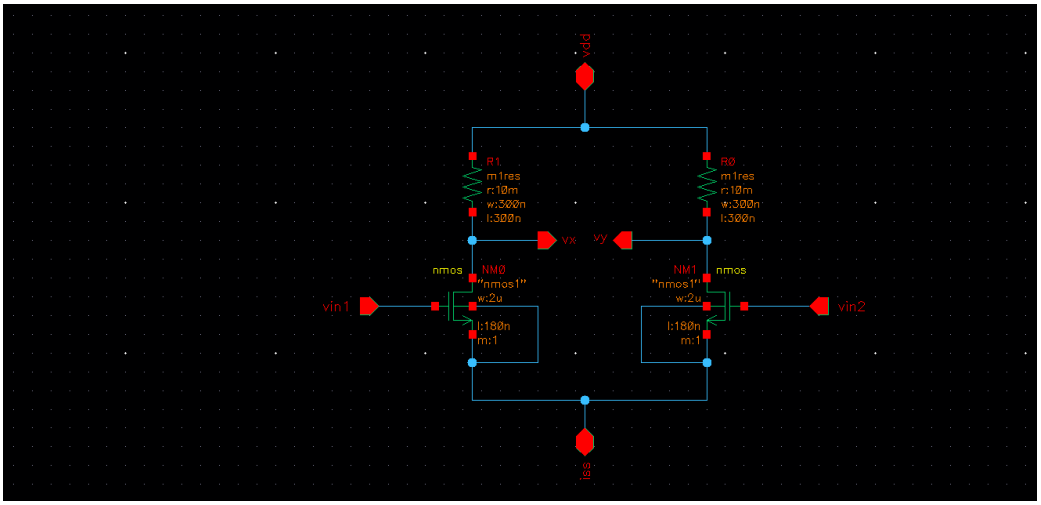
PURPOSE:

- To evaluate the behaviour of the differential pair when two inputs vary independently.
- To observe gain matching, symmetry, and signal steering between branches.
- To verify that the circuit rejects common-mode signals.
- To prepare the design for the next stages.

SIMULATION PARAMETERS:

Parameter	Value
NMOS W/L	1 µm / 180 nm
R1, R0	Poly resistors (about 1 KΩ)
VDD	1.8 V
VSS	0 V
vin1, vin2	AC small-signal inputs
Common-mode voltage	0.5 – 0.7 V
Frequency sweep	1 GHz
Temperature	27°C

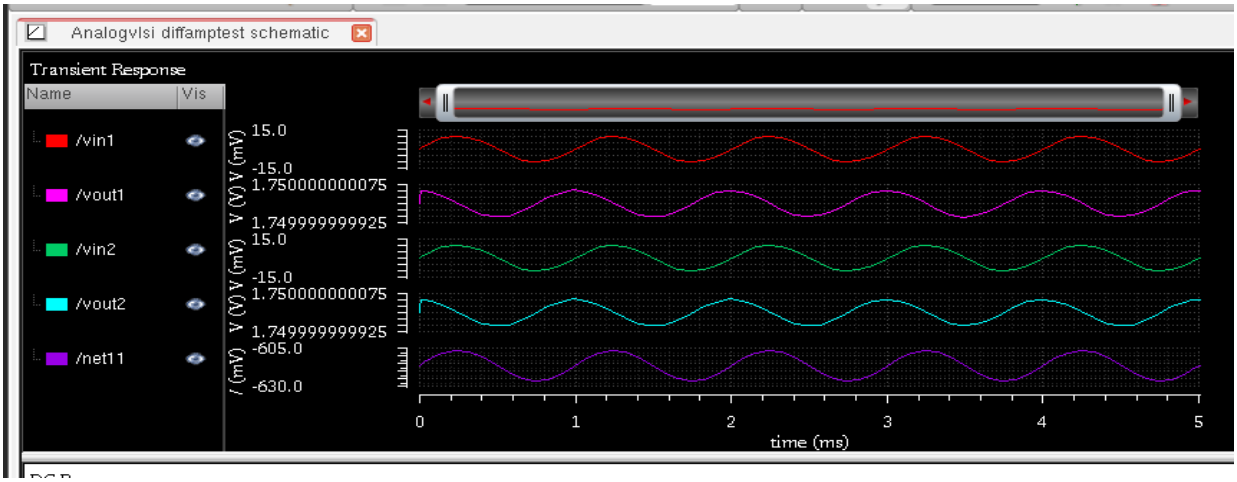
SCHEMATIC:



Schematic of differential of amplifier

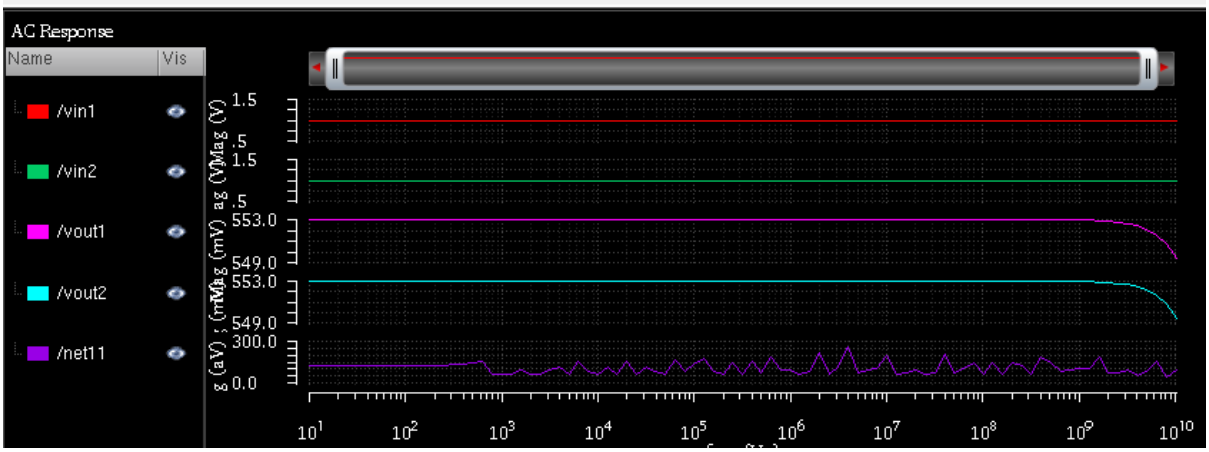
WAVEFORM ANALYSIS:

- **Transient Analysis** computes the circuit's response over a specific time interval.
  For a differential amplifier, this analysis helps determine:
  Linearity and Swing, Gain Calculation,
  Phase Relationship: Whether the output is inverted or non-inverted relative to the input. Common Mode Rejection: How well the amplifier ignores signals that are identical on both inputs.



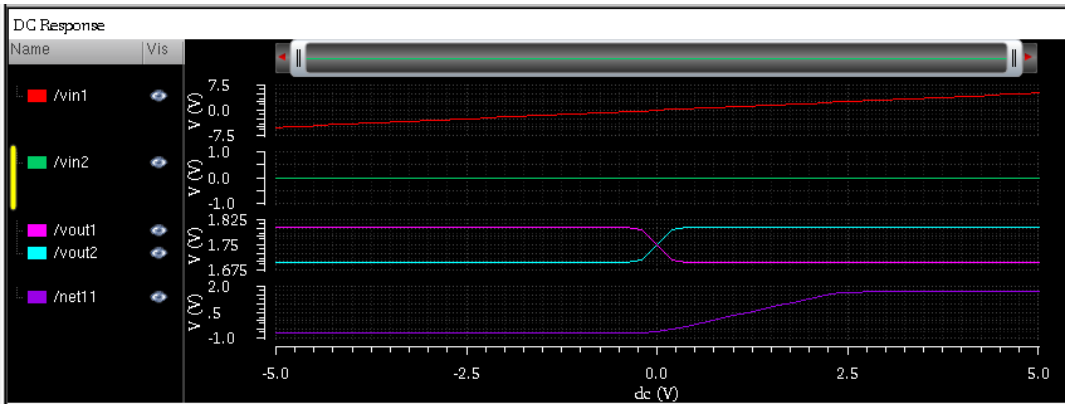
Transient response of differential amplifier

- AC analysis evaluates the small-signal behaviour, including differential gain, common-mode gain, and frequency response.



AC response of differential of amplifier

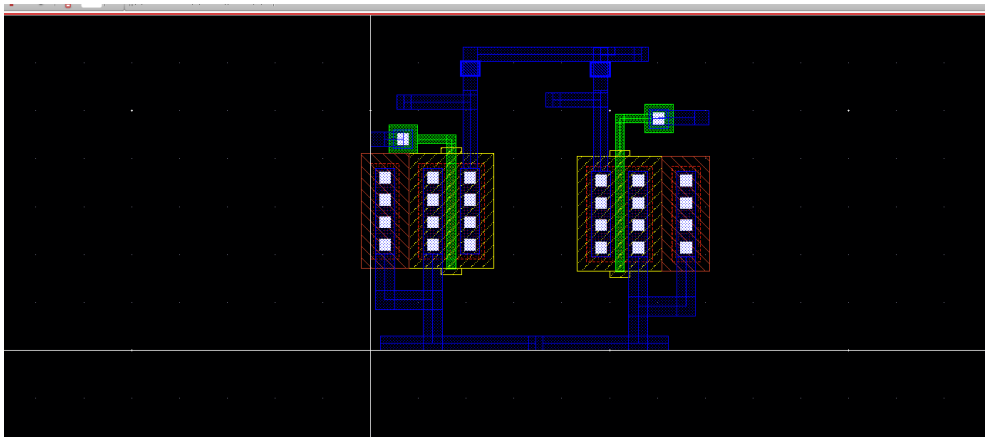
- DC analysis examines the static operating point (Q-point) of the differential amplifier. It determines the bias currents, node voltages, and transistor regions of operation



`*DC response of differential amplifier*

- As we can see the V_{out1}, V_{out2} vs $(V_{in1} — V_{in2})$ graph from the waveform.

LAYOUT:



LAYOUT OF DIFFERENTIAL AMPLIFIER

FINAL OUTCOME:

Differential amplifier is designed using cadence and designed layout according to schematic. Simulated Transfer characteristics of differential amplifier.

8. SINGLE STAGE OPAMP

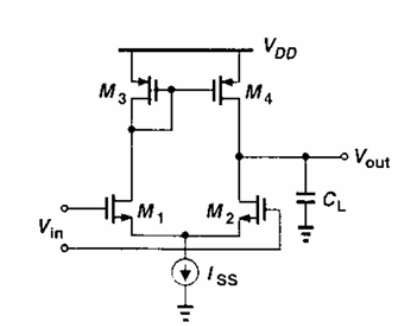
AIM:

- To design and simulate a single stage Op-Amp using Cadence Virtuoso and analyze AC characteristics and the Transient Analysis.

SOFTWARE USED:

- CADENCE VIRTUOSO with PDK as GPDK180

THEORY:



- An operational amplifier is a high-gain voltage amplifier used in analog integrated circuits.
- A single-stage operational amplifier usually consists of a differential input stage with an active load, providing voltage amplification with simple architecture and low power consumption.
- The small-signal low frequency gain of a single-stage op-amp is given by:

$$Av = gm(r_{ON}||r_{OP})$$

- The performance of the op-amp is affected by device dimensions, biasing, and parasitic capacitances introduced during layout.

PURPOSE:

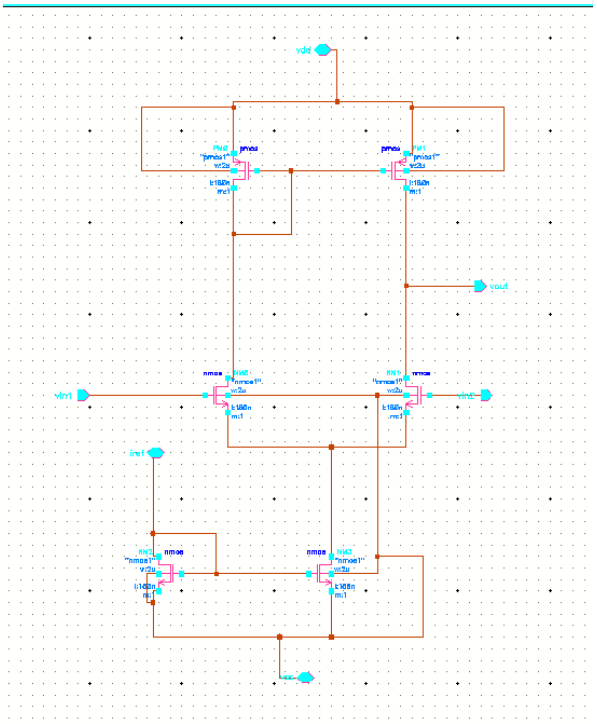
- The purpose of this experiment is to understand:
- Layout design techniques for analog circuits
- Effects of parasitic capacitances on amplifier performance
- Bandwidth (BW): Frequency range over which gain is stable
- Slew Rate (SR): Maximum rate of change of output voltage
- CMRR: Ability to reject common-mode noise

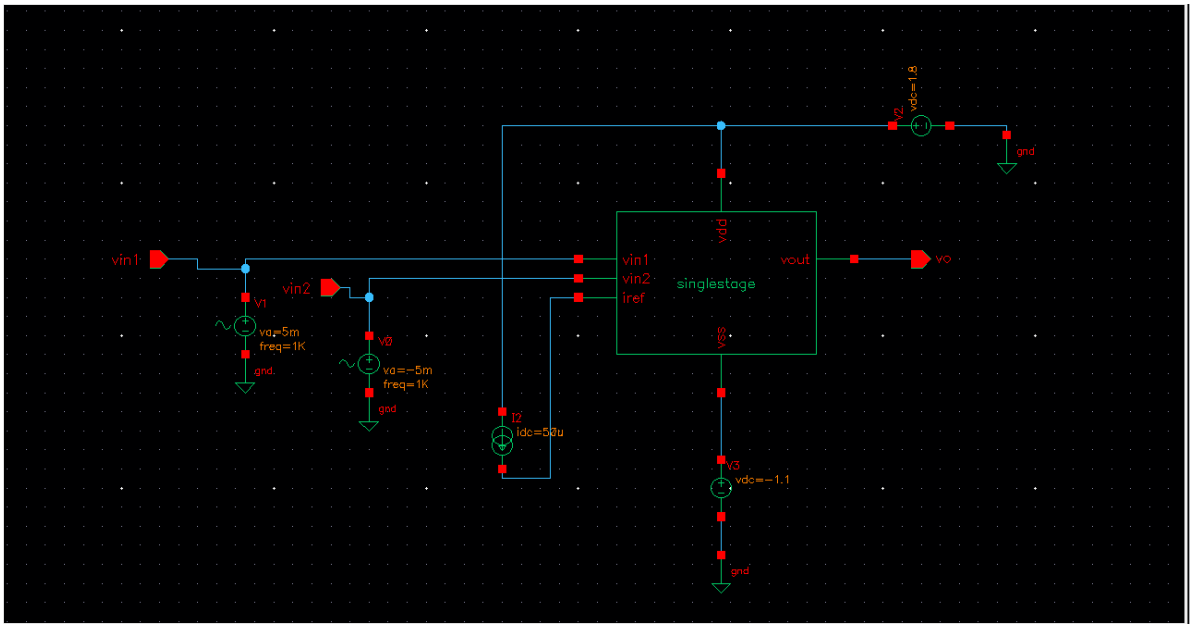
SIMULATION PARAMETERS:

Parameter	Value
NMOS W/L	1 µm / 180 nm
VDD	1.8 V
VSS	0 V
vin1	5mV & 1KHz
vin2	-5mV & 1KHz

- Common-mode voltage 0.5 – 0.7 V
- Frequency sweep 1 GHz
- Temperature 27°C

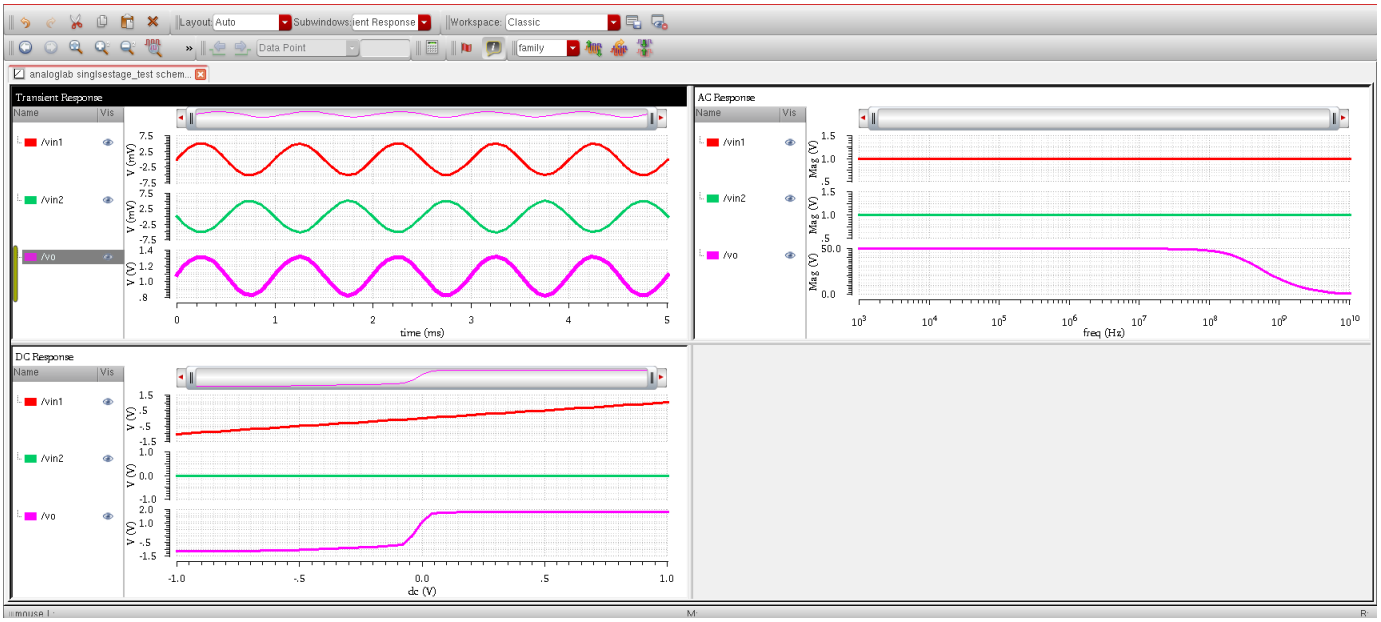
SCHEMATIC:





Test schematic

WAVEFORM ANALYSIS:



1. **DC**

Analysis Steps:

1. ADE L → Analyses → Choose
2. Select:
    - *dc*
    - Sweep variable: **Component Parameter**
    - Choose the **V3 Component**
    - Set the sweep range from Start = **-5 V**, Stop = **5 V**

2. AC

Analysis Steps:

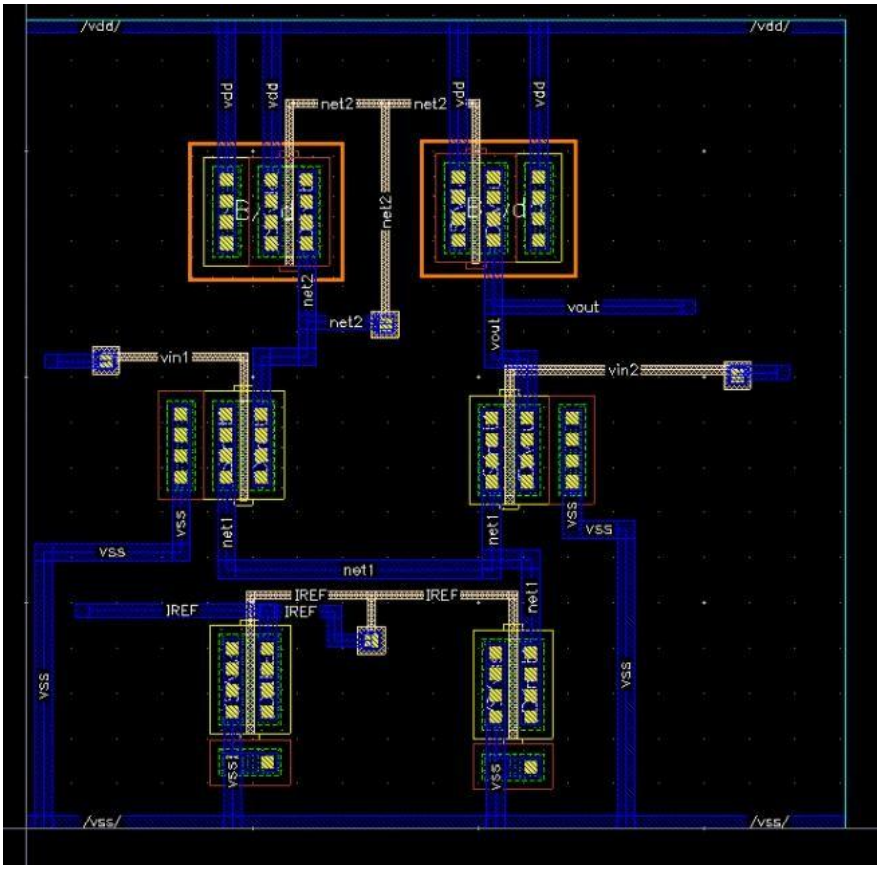
1. ADE L → Analyses → Choose
2. Select:
    - *AC*
    - Sweep variable: **Frequency**
    - Set the sweep range from Start = **1 V**, Stop = **10G**
    - Set Sweep type as Logarithmic

3. **Transient Analysis: -**

- ADE L → Analyses → trans
- Stop Time: **5 m**

Accuracy: Moderate

LAYOUT:



FINAL OUTCOME:

- An Single Stage Operational Amplifier was designed and simulated using Cadence Virtuoso with gpdk90/gpdk180 CMOS technology.
- The full design flow included schematic creation, symbol generation, and circuit connection.
- DC, AC, and Transient simulations were executed using the ADE environment.
- DC analysis confirmed correct transistor biasing and input-output characteristics.

9. DOUBLE STAGE OPAMP

AIM:

- To design and simulate a **Two Stage Operational Amplifier** using Cadence Virtuoso and analyze its **DC characteristics**, AC Characteristics as well as Transient Analysis.

SOFTWARE USED:

- CADENCE VIRTUOSO with PDK as GPDK180

THEORY:

An Operational Amplifier (Op-Amp) is a high-gain, direct-coupled amplifier widely used in analog electronic circuits for signal conditioning, filtering, and performing mathematical operations such as addition, subtraction, integration, and differentiation. It is typically designed using differential amplifiers, gain stages, and an output buffer to provide high input impedance and low output impedance.

Basic Structure

An Op-Amp generally consists of three main stages:

Input Differential Stage

- Compares two input signals (inverting and non-inverting)
- Provides high input impedance
- Ensures excellent Common-Mode Rejection Ratio (CMRR)

Gain stage:

- Provides very high open-loop voltage gain
- Amplifies the differential signal from the input stage
- Includes internal compensation for stability

Output Stage

- Delivers high current drive capability.
- Maintains low output impedance for maximum signal transfer Ideal

Although practical Op-Amps cannot fully achieve these ideal parameters, modern CMOS-based designs closely approach them for accurate and stable amplification.

Modes of operation:

Although practical Op-Amps cannot fully achieve these ideal parameters, modern CMOS-based designs closely approach them for accurate and stable amplification.

Open-Loop Mode

- Very high gain, used for comparators
- Not suitable for linear amplification due to instability

Closed-Loop Mode

- Uses feedback (negative feedback is most common)
- Controls gain, improves stability, bandwidth, linearity, and reduces distortion Key

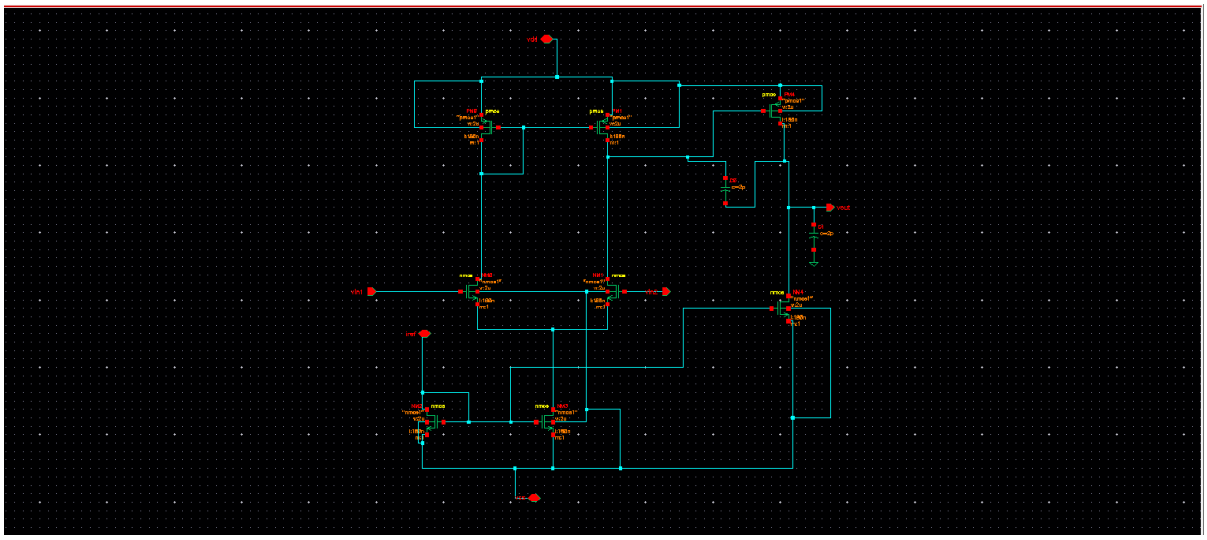
PURPOSE:

- The purpose of this experiment is to understand:
- Layout design techniques for analog circuits
- Effects of parasitic capacitances on amplifier performance
- Bandwidth (BW): Frequency range over which gain is stable
- Slew Rate (SR): Maximum rate of change of output voltage
- CMRR: Ability to reject common-mode noise

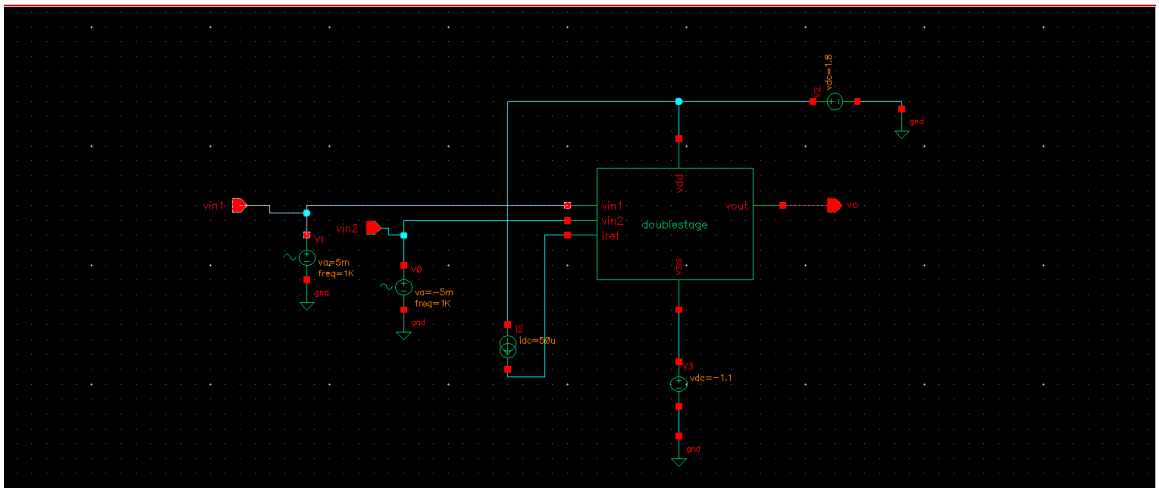
SIMULATION PARAMETERS:

Parameter	Value
NMOS W/L	1 µm / 180 nm
R1, R0	Poly resistors (about 1 KΩ)
VDD	1.8 V
VSS	0 V
vin1	5mV & 1KHz
vin2	-5mV & 1KHz
Common-mode voltage	0.5 – 0.7 V
Frequency sweep	1 GHz
Temperature	27°C

SCHEMATIC:

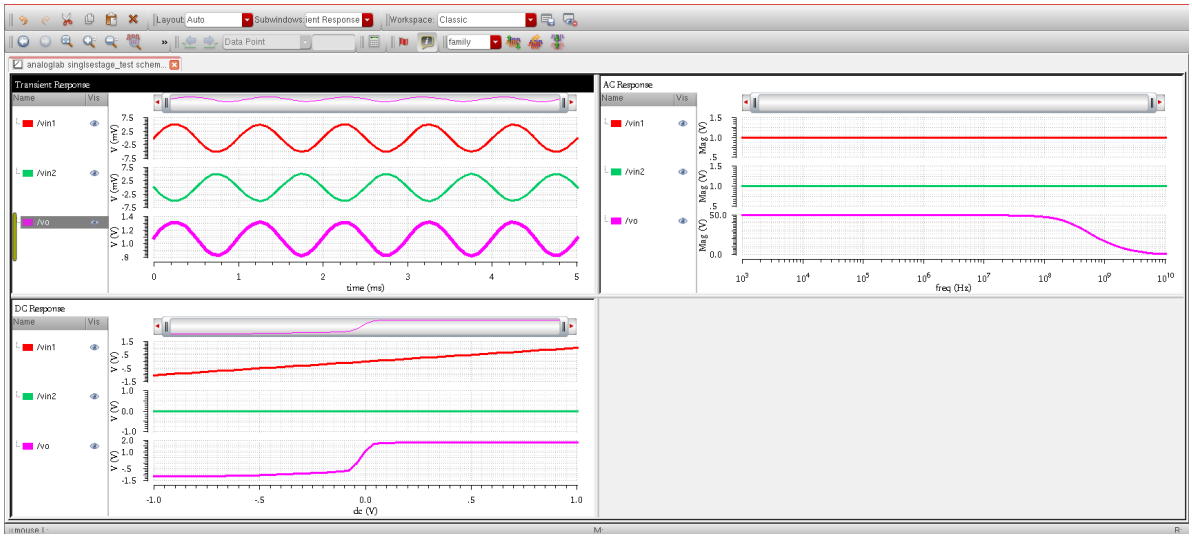


Schmeatic of doublestage op-amp



Schematic testbench of double stage 0p-amp

WAVEFORM ANALYSIS:



AC, DC, Tran analysis waveform

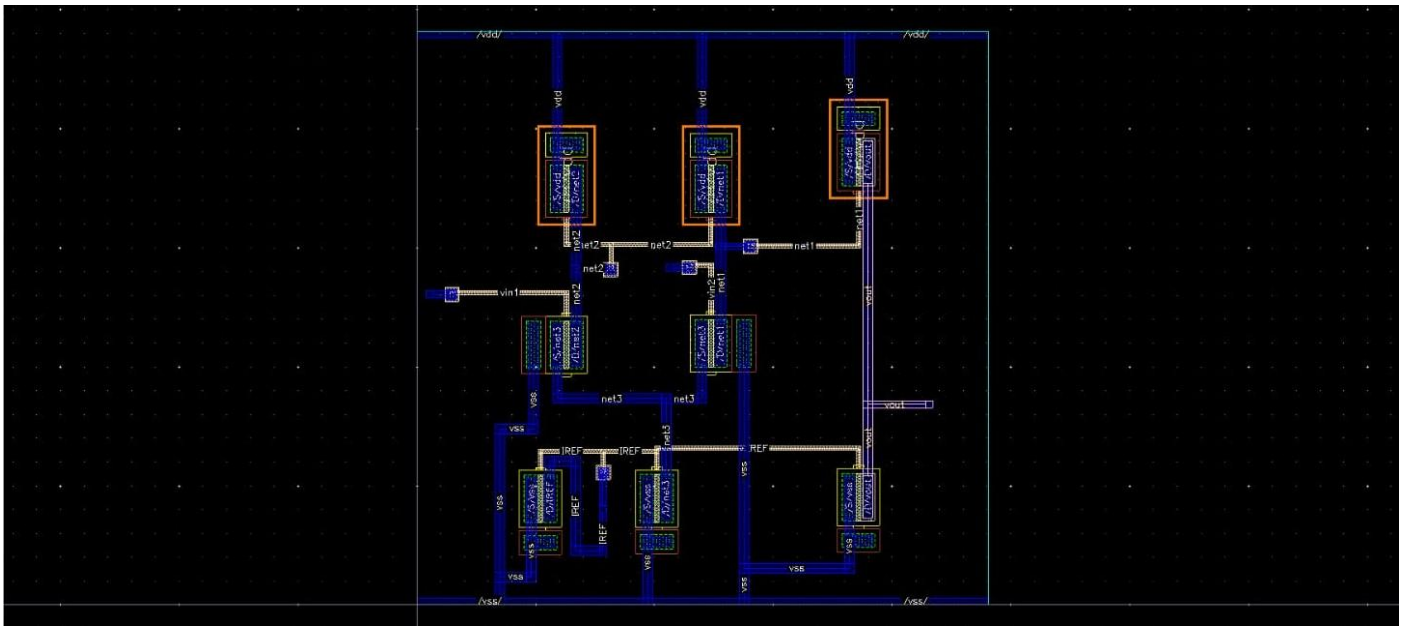
Set AC Analysis Parameters

- **Sweep Variable** → Frequency (default)
- **Sweep Type** → Linear / Logarithmic

  (Commonly **Logarithmic** for wide range frequency response)

- **Start Frequency** → 1K Hz
  Stop Frequency → e.g., 100 M Hz or 1G Hz *(for Op-Amp up to high frequency limits)*
- *Choose Automatic Sweep Type and apply.*
- **Run the values** Then press **OK**.
- Here our Aim is to check the "Gain vs Frequency and Phase vs Frequency characteristics of the Op-Amp" .
- For that step go to Results -> Choose the Direct Plot -> AC Gain Phase, To check the output we have to run the AC Analysis and choose the Vin 1 and V-out as well as Vin2 and V-out.
- To check Vin1 Vs Vout and Vin2 Vs Vout Gain vs Frequency and Phase vs Frequency characteristics.

LAYOUT:



Final Outcome:

- A Two Stage Operational Amplifier was designed and simulated using Cadence Virtuoso with gpdk90/gpdk180 CMOS technology.
- The full design flow included schematic creation, symbol generation, and circuit connection.
- AC analysis was executed using the ADE environment.
- The **Gain vs Frequency** and **Phase vs Frequency** characteristics of the Op-Amp
- A layout was designed to ensure physical implementation while satisfying design rules.
- The experiment provided improved understanding of analog IC design techniques and Two Stage Op-Amp performance analysis in Cadence.