## EXPERIMENT - 10

## TWO STAGE OPERATIONAL AMPLIFIER

**Aim:** To design, simulate, and implement the schematic and physical layout of a MOSFET two stage operational amplifier using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

**Software & Technology Used:** CADENCE VIRTUOSO, 180nm.

**Theory:** A two-stage CMOS operational amplifier combines high DC gain with adequate output swing and drive capability. It consists of:

1. Input differential gain stage, which converts differential input voltage into a high-gain single-ended signal.
2. Second gain/output stage, typically a common-source amplifier, which boosts gain and provides sufficient output drive.

This topology is widely used because it achieves high open-loop gain, supports moderate-to-large output swing, and can be compensated for stable operation in closed-loop configurations. In this lab, the op-amp is designed and simulated using Cadence Virtuoso.

Small-signal gain of stage 1:

$$A_1 \approx g_{m1}(r_{o1} \parallel r_{o,load})$$

Small-signal gain of stage 2:

$$A_2 \approx g_{m2}(r_{o2} \parallel r_{o,load2})$$

Overall DC Gain

$$A_v = A_1 \cdot A_2$$

Pole Expressions

$$p_1 \approx \frac{1}{(r_{o1} \parallel r_{o,load})C_1}$$

$$p_2 \approx \frac{1}{(r_{o2} \parallel r_{o,load2})C_L}$$

**Procedure**

Follow the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

**Schematic Diagram:**

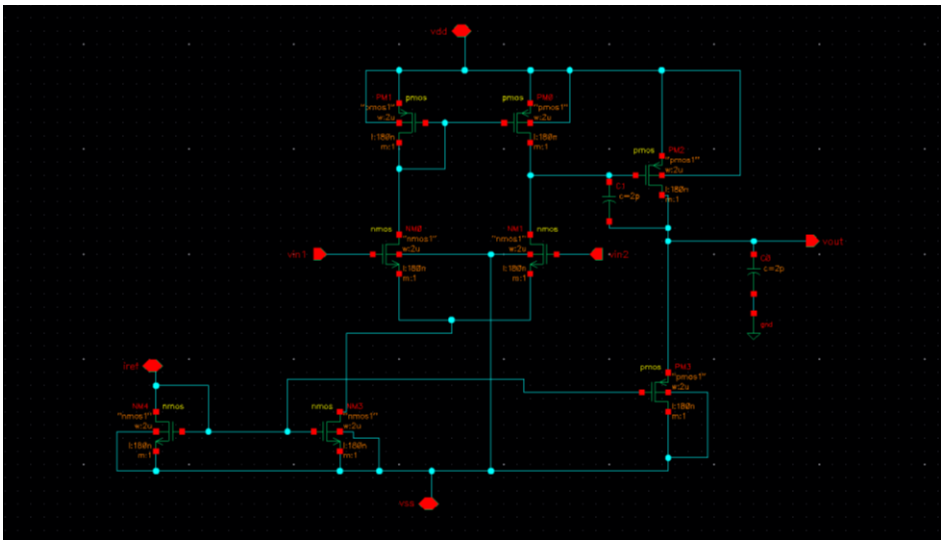


Fig: Schematic of two Stage Operational Amplifier

**Functional Stimulation:**

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of two stage operational amplifier, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

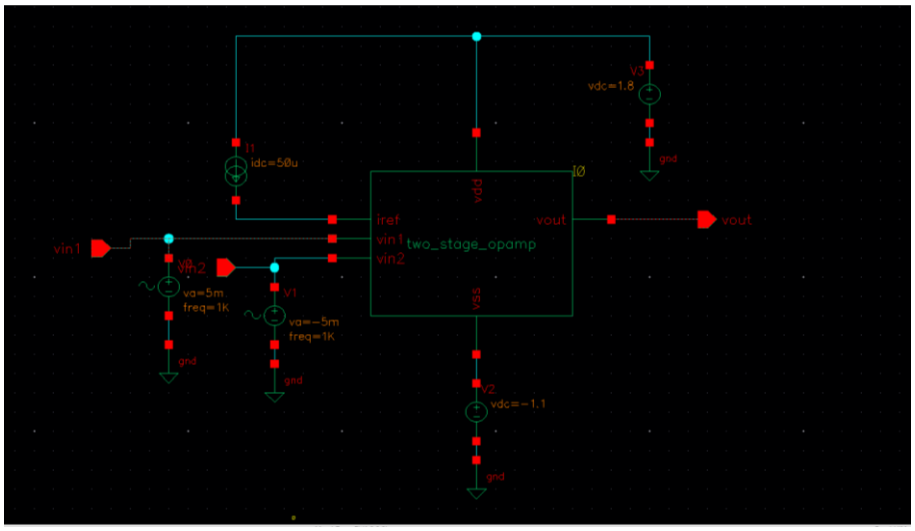


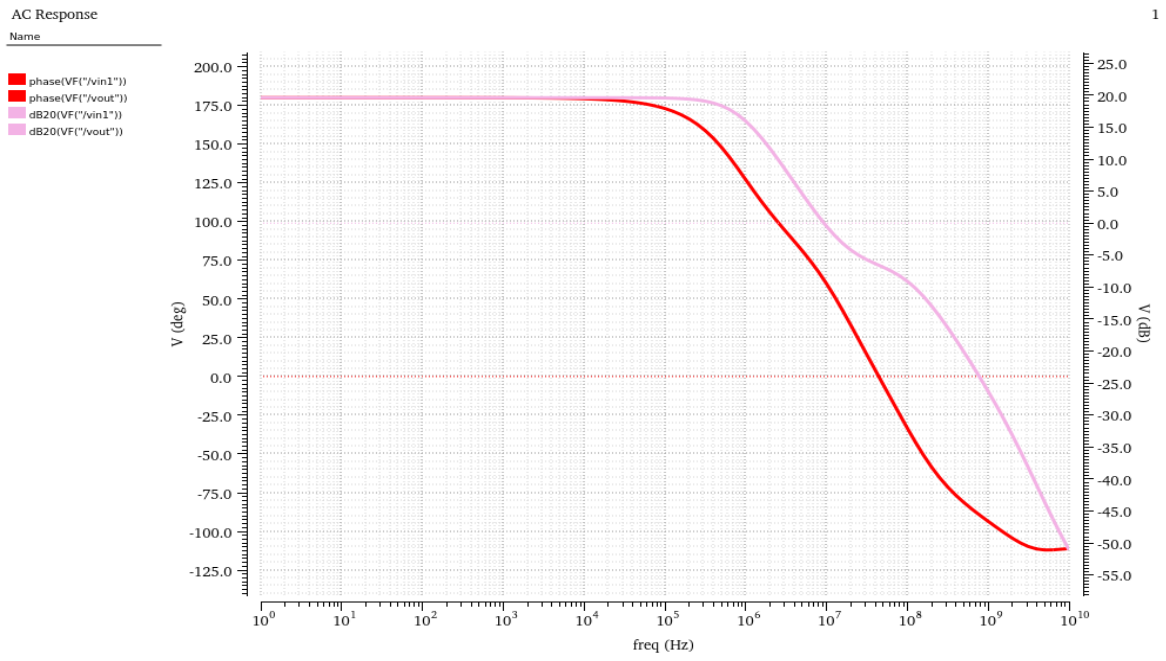

Fig: Test bench schematic of two Stage Operational Amplifier

**Properties of vdc and vsin:**

| Library Name | Cell Name | Properties |
|---|---|---|
| AnalogLib | vdc | DC voltage = 1.8V |
| AnalogLib | vdc | DC voltage = -1.1V |
| AnalogLib | vsin | AC magnitude = 1V<br>Amplitude = 5m<br>Frequency = 1KHz |
| AnalogLib | vsin | AC magnitude = 1V<br>AC Phase = 180<br>Amplitude = -5m<br>Frequency = 1KHz |
| AnalogLib | idc | DC current = 50u |

**Simulation:**

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "1" and "Stop" value as "10G", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".



**Layout:**

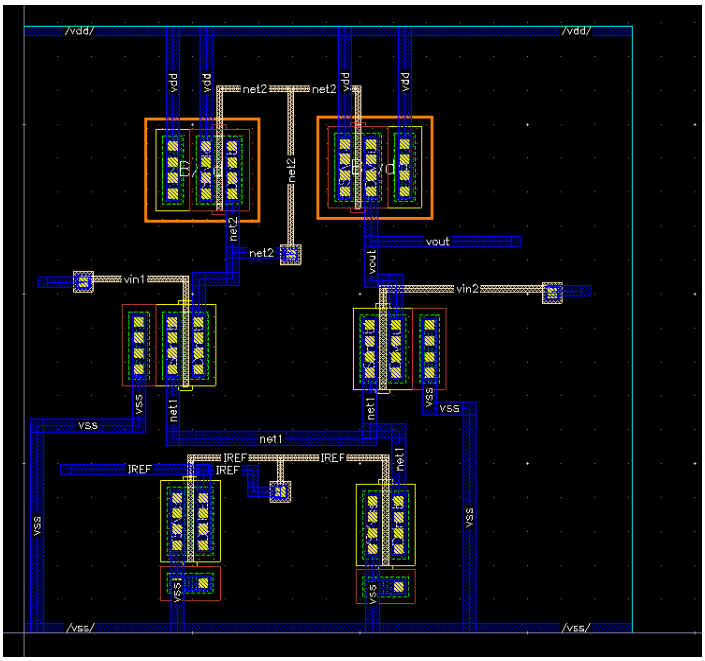



Fig: Two Stage Operational Amplifier layout

**DRC:**

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

**LVS:**

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

**QRC:**

To extract the Parasitics, select "Assura → Quantus", select "Technology →gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type →RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

**Conclusion:**

The Two Stage Operational Amplifier was successfully designed and implemented using Cadence Virtuoso. Pre- layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.