EXPERIMENT - 06

CASCODE AMPLIFIER

Aim: - To design, simulate, and implement the schematic and physical layout of a MOSFET cascode amplifier using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm

Theory: A cascode amplifier is a two-transistor configuration that combines a common-source (CS) or common-emitter stage with a common-gate (CG) or common-base stage. It is widely used in analog integrated circuit design due to its ability to achieve high gain, improved bandwidth, and enhanced output impedance. In CMOS design, the cascode topology is implemented using MOSFETs and is an essential building block in operational amplifiers, current mirrors, low-noise amplifiers, and RF circuits.

The total small-signal voltage gain of the cascode amplifier is approximately:

$$A_v \approx g_{m1} \times (r_{o1} \parallel g_{m0} r_{o0} r_{o1})$$

Because the cascode device significantly boosts output resistance, the overall gain becomes:

$$A_v \approx g_{m1} \cdot r_{o1} \cdot g_{m0} \cdot r_{o0}$$

This is much larger than that of a single common-source amplifier.

Procedure

Following the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:

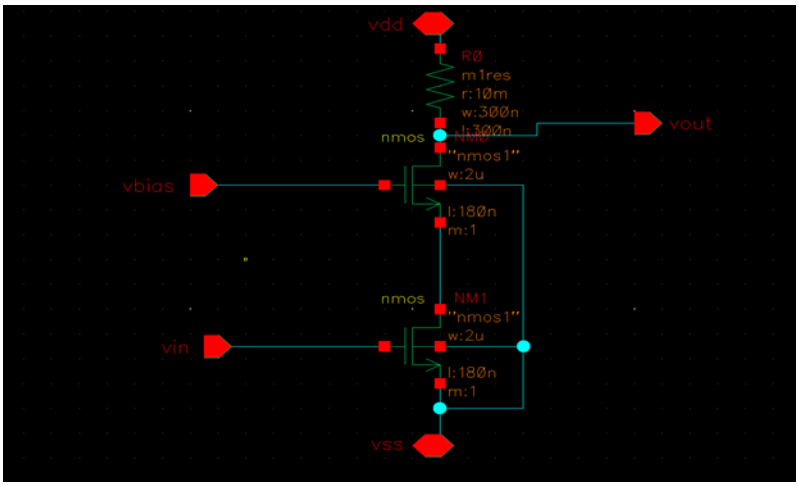

Fig: Schematic of Cascode Amplifier

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Cascode amplifier, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

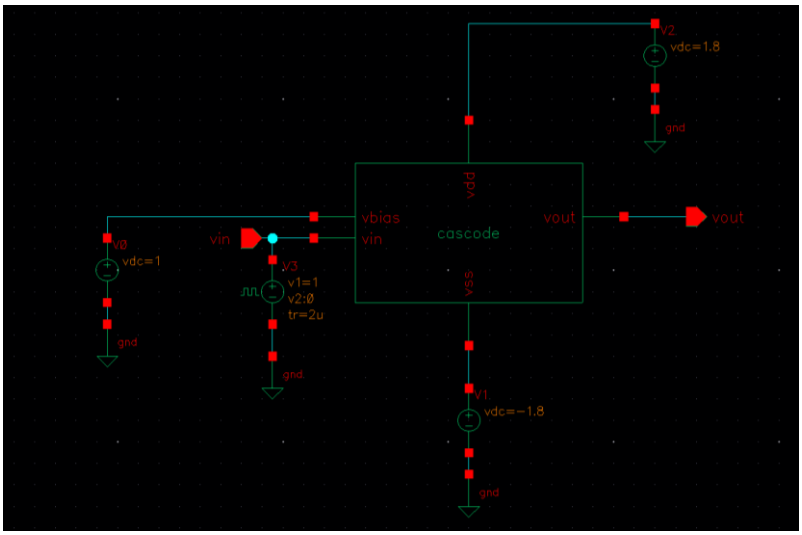

Fig: Test bench schematic of Cascode Amplifier

Properties of vdc and vpulse

Library Name	Cell Name	Properties
AnalogLib	Vdc	Vbias: DC voltage = 1V Vss: DC voltage = -1.8V Vdd: DC voltage = 1.8V
AnalogLib	Vpulse	V1 = 1V V2 = 0V Delay time = 0ns Rise time = 2ns Fall time = 2ns Pulse width = 5ns

Simulation:

Launch ADE L, import the design variables, mention the values and select the Transient Analysis, and mention the parameters and choose the signals to be plotted as shown in Figure.

To set up a "**Transient Analysis**", select "tran", mention the **Stop Time – 2m** select **Accuracy Defaults - moderate**, click on "Apply" and click on "OK".

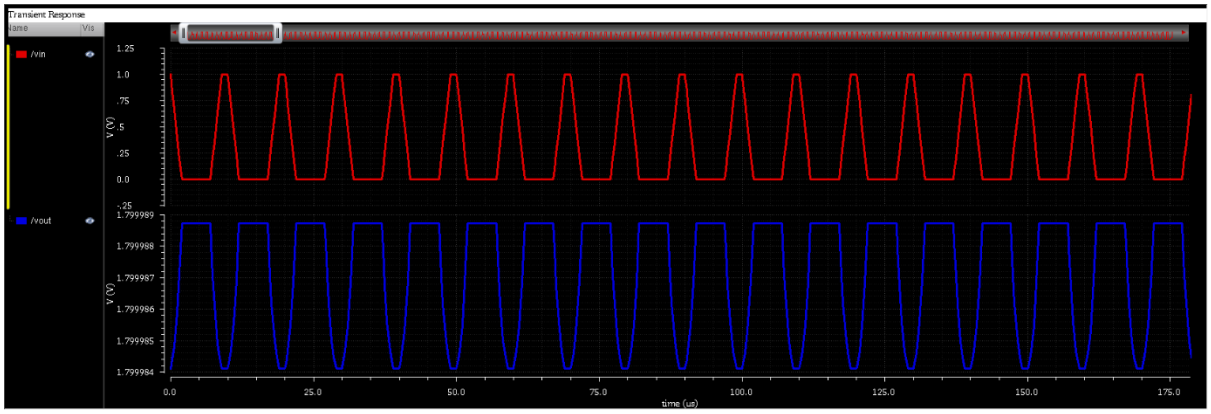

Fig: Pre-layout stimulation of Cascode Amplifer

Layout:

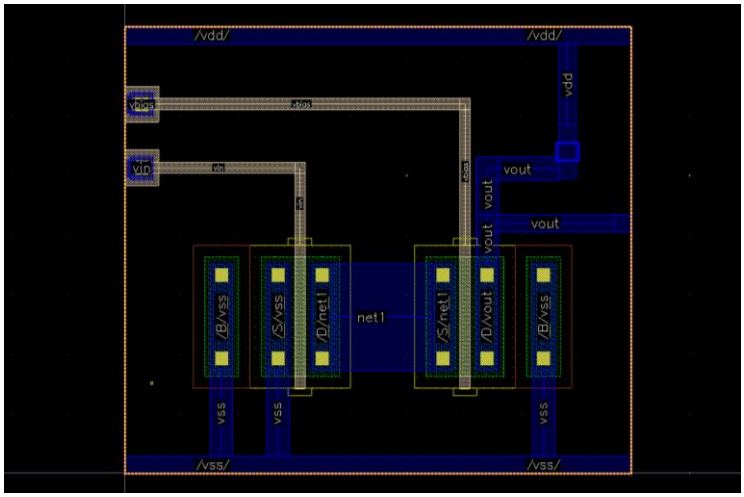

Fig: Cascode amplifier layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura → Quantus", select "Technology →gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type → RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

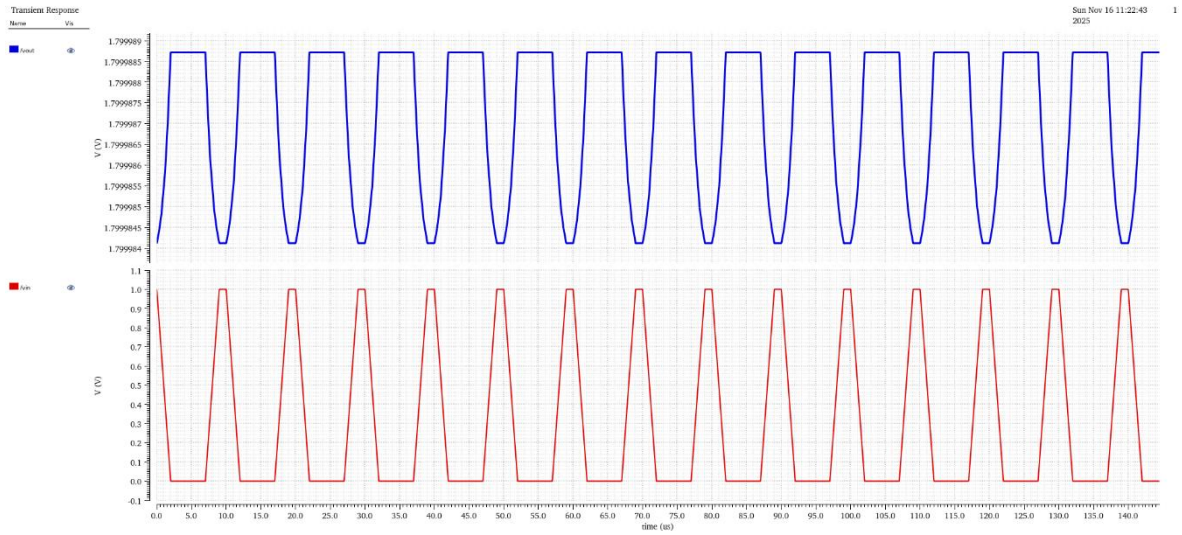

Fig: Post-layout stimulation of Cascode Amplifer

Conclusion:

The cascode amplifier was successfully designed and implemented using Cadence Virtuoso. Pre-layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.