EXPERIMENT - 03

COMMON SOURCE WITH CURRENT SOURCE LOAD

Aim: To design, simulate, and implement the schematic and physical layout of a MOSFET common source with current source load using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm.

Theory: The common-source (CS) amplifier with a current source load is a high-gain MOSFET amplifier in which the input signal is applied to the gate of an NMOS transistor, and the load at the drain is provided by an active PMOS current source rather than a passive resistor. Replacing the resistor with an active load significantly increases the small-signal voltage gain, improves output swing, and enhances linearity. This configuration is widely used in analog IC design and is fundamental to differential pairs, operational amplifiers, and gain stages.

The NMOS transistor operates in saturation, where the small-signal drain current is controlled by:

$$i_d = g_m v_{gs} + \frac{v_{ds}}{r_{oN}}.$$

The PMOS transistor functions as a current source load, biased to remain in saturation and supply a nearly constant drain current I_D. Its small-signal resistance contributes to the overall load resistance.

Since both transistors are in saturation, the small-signal output node experiences the combined output resistances of the NMOS and PMOS:

$$r_o = r_{oN} \parallel r_{oP}.$$

Applying an AC input signal $v_{in}$to the gate modulates the NMOS drain current, producing a small-signal change in the output voltage at the drain:

$$v_o = -i_d(r_{oN} \parallel r_{oP})$$

The small-signal voltage gain of the common-source stage with a current source load is:

$$A_v = -g_m(r_{oN} \parallel r_{oP}).$$

In contrast, a resistor-loaded CS amplifier has:

$$A_v \approx -g_m R_D,$$

The input is applied to the MOS gate, so the input impedance is extremely high:

$$R_{in} \approx \text{gate resistance} \gg 1\ \text{M}\Omega.$$

The output impedance is the parallel combination of the two devices' output resistances:

$$R_{out} = r_{oN} \parallel r_{oP}.$$

Procedure

Follow the techniques, create a New Library using the option "File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:

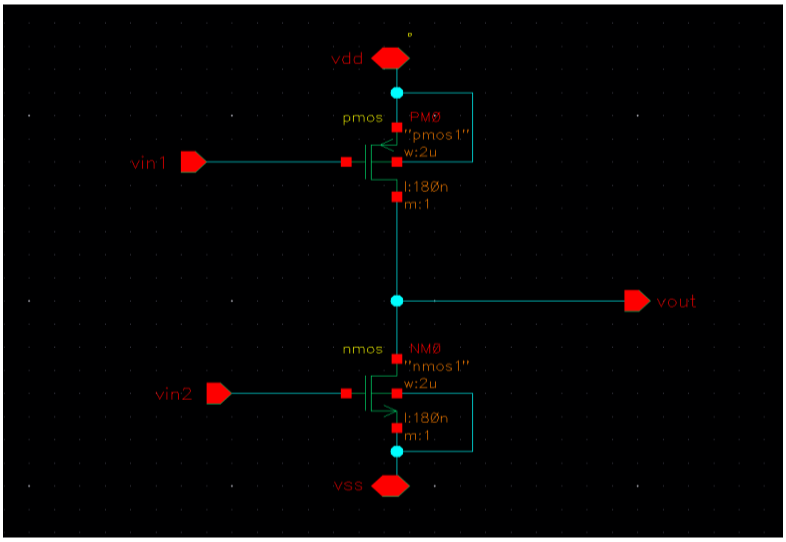


Fig: Schematic of Common Source with current source load

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Common source with current source load, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

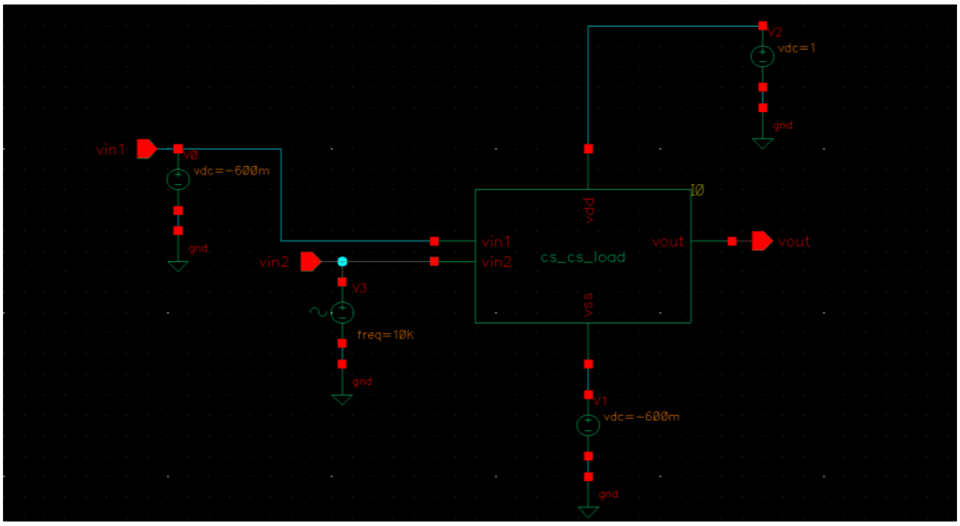


Fig: Test bench schematic of Common Source with current source load

Properties of vdc and vsin:

Library Name	Cell Name	Properties
AnalogLib	vdc	Vin1: DC voltage = -600mV
AnalogLib	vdc	Vss: DC voltage = -600mV
AnalogLib	vsin	AC magnitude = 1V Frequency = 1KHz
AnalogLib	vdc	Vdd: DC voltage = 1V

Simulation:

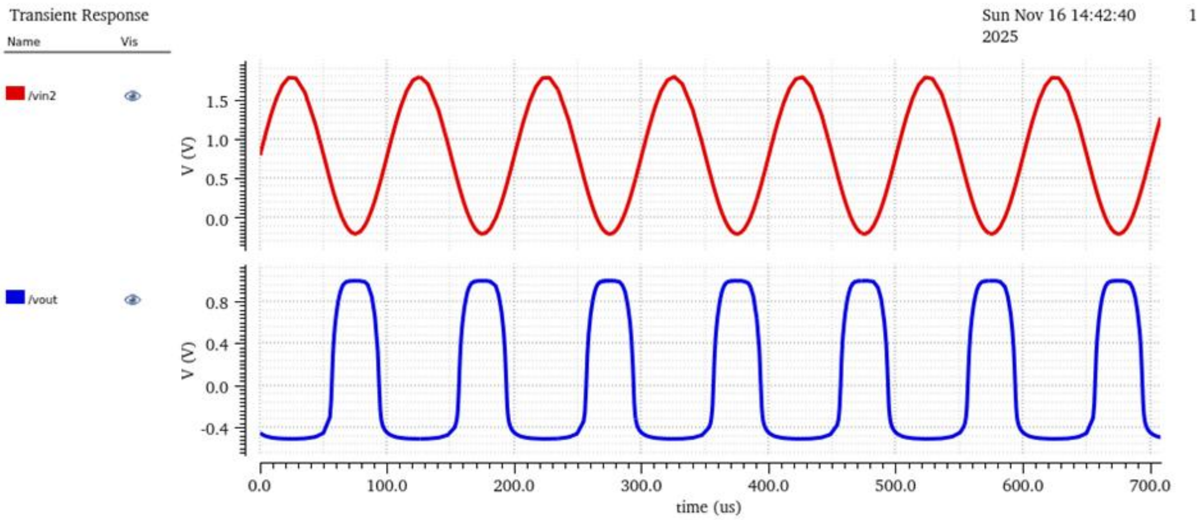
Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

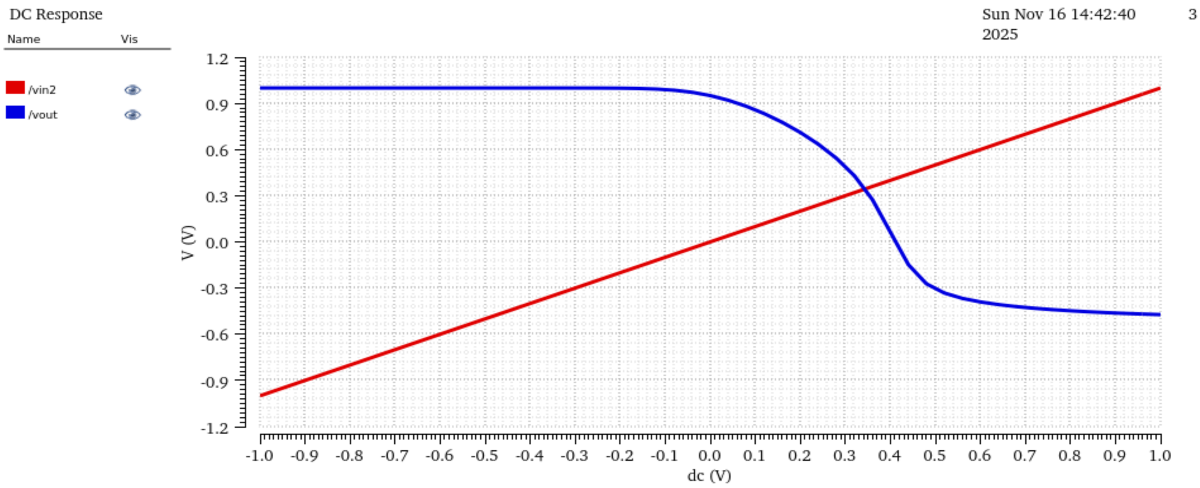
To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "-1" and "Stop" value as "1", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "0" and "Stop" value as "1M", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".

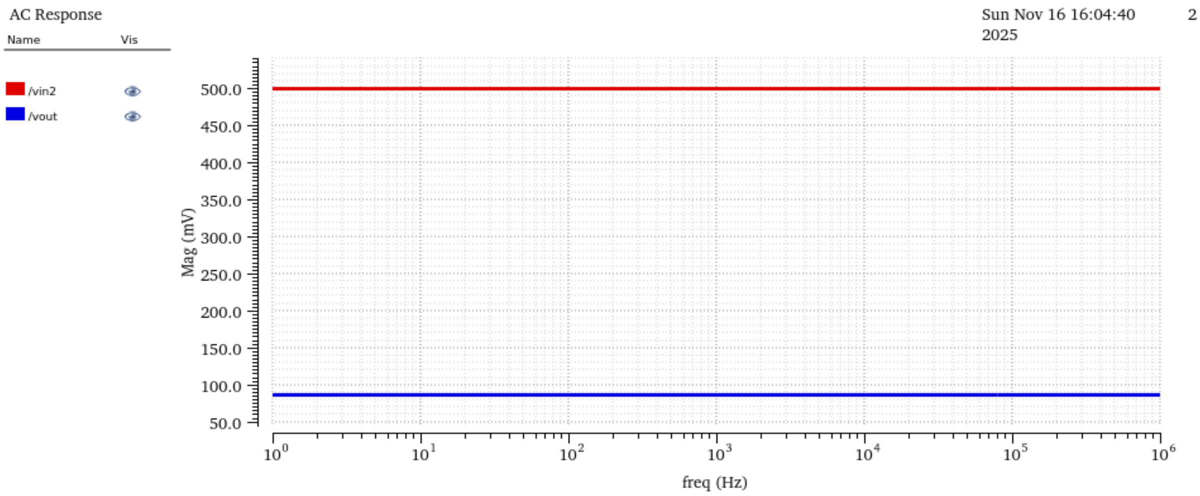
Transient Response:



DC Response :



AC Response :



Layout:

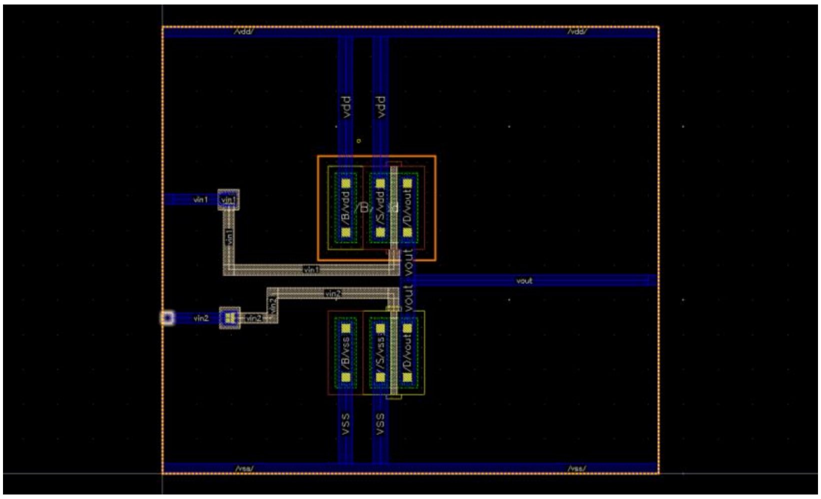


Fig: Common source with current source load layout

DRC:

To check for the DRC violations, browse the “assura_tech.lib” file, select “Assura → Run DRC”, verify the Layout Design Source, mention a “Run Name”, select “Technology → gpdk180” and click on “OK”.

LVS:

To check for the LVS violations, select “Assura → Run LVS”, verify the Schematic Design Source and the Layout Design Source, mention a “Run Name”, select “Technology → gpdk180” and click on “OK”.

QRC:

To extract the Parasitics, select “Assura → Quantus”, select “Technology →gpdk180”, “Output → Extracted View” from the “Setup” option, select “Extraction Type →RC” and “Ref Node → VSS” from the “Extraction”, Disable HRCX and click on “OK”.

The result can be checked from the Library Manager.

Conclusion:

The common source with current source load was successfully designed and implemented using Cadence Virtuoso. Pre- layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.