ECE 5002 – ANALOG VLSI DESIGN

Fall Semester 2025-26

M. Tech VLSI DESIGN

School of Electronics Engineering Lab report

Submitted to

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EXPERIMENT – 01

NMOS AND PMOS

Aim: To design, simulate, and implement the schematic and physical layout of MOSFETs nMOS and pMOS using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology used: CADENCE VIRTUOSO, 180nm

Theory: An **nMOS (n-channel MOSFET)** uses electrons as majority carriers. When a positive gate voltage is applied relative to the source, an electron inversion layer forms beneath the oxide, creating a conductive channel between drain and source. nMOS devices offer higher mobility, faster switching, and lower on-resistance, making them widely used in digital logic and high-speed circuits.

A **pMOS (p-channel MOSFET)** uses holes as majority carriers. When a negative gate voltage is applied relative to the source, a hole inversion layer forms, allowing current to flow from source to drain. pMOS devices typically have lower mobility but are essential in forming CMOS technology, where nMOS and pMOS pairs provide low static power, high noise margins, and full logic swing.

Procedure:

Create a New Library using the option File ⟶New ⟶ Library", create a New Cell View upon selecting the newly created library using the option "File⟶New Cell View" and instantiate the required devices using the "Create⟶Instance" option.

Schematic Diagram:

nMOS:

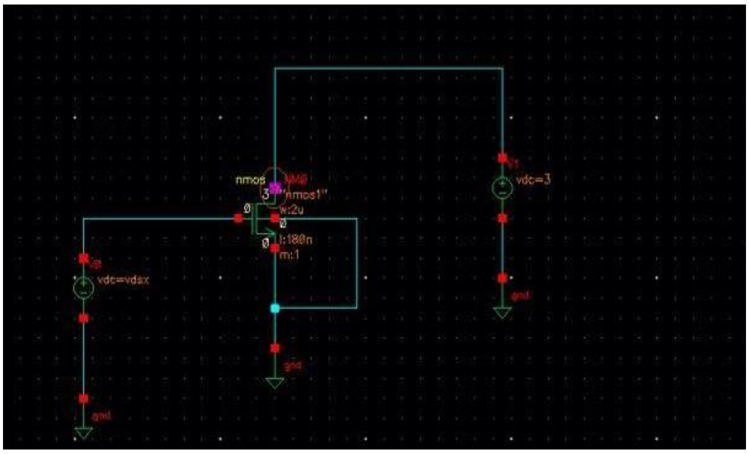


Fig: Schematic of nmos

pMOS:

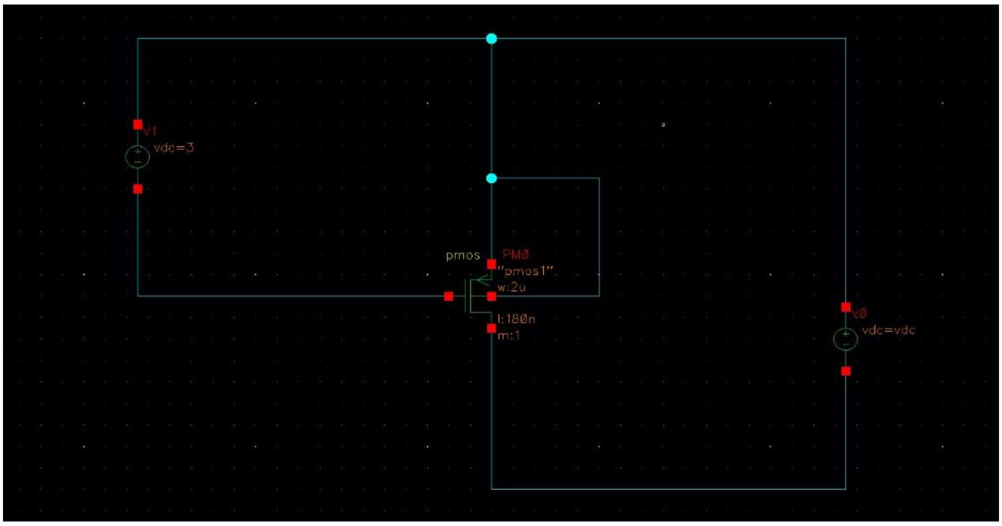


Fig: Schematic of pmos

Analysis: -

1. Transfer Characteristics (ID vs VGS)

Objective: Observe how ID changes with VGS (VDS fixed).

Steps:

1. Set VDS = 1.8 V (constant).
2. Open ADE_L → Analysis → DC.
3. Select Sweep Variable = VGS (e.g., 0 V to 1.8 V).
4. Go to Outputs → Select on Schematic → choose ID.
5. Run the simulation to get ID vs VGS plot.
6. From the graph, note:
   - Threshold Voltage (VTH)
   - Current rising region (saturation region)

2. Output Characteristics (ID vs VDS)

Objective: Observe how ID changes with VDS for different VGS.

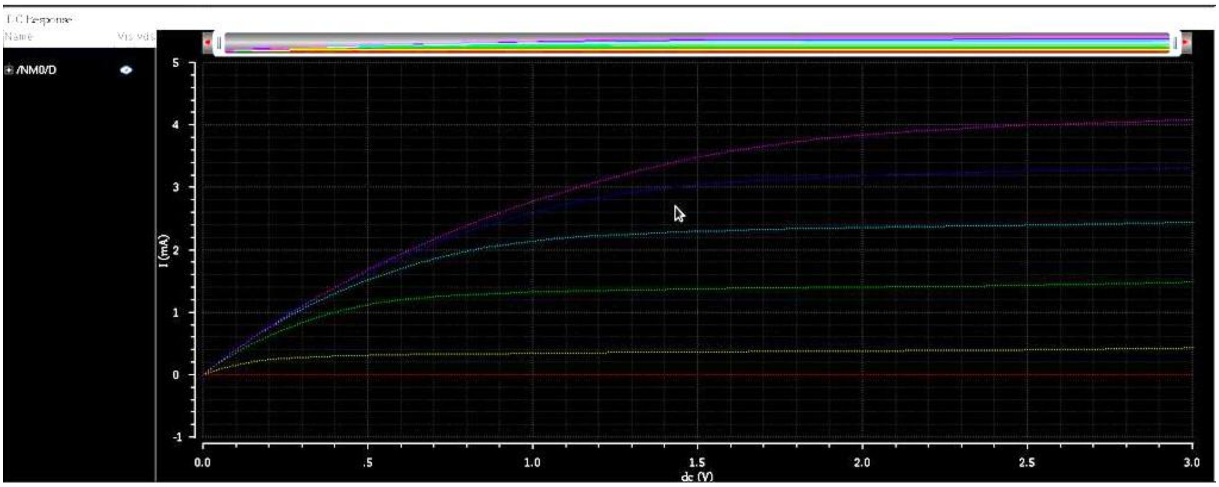
Steps:

1. Set VGS = constant values (e.g., 0.9 V, 1.2 V, 1.5 V).
2. Open ADE_L → Analysis → DC.
3. Select Sweep Variable = VDS (e.g., 0–1.8 V).

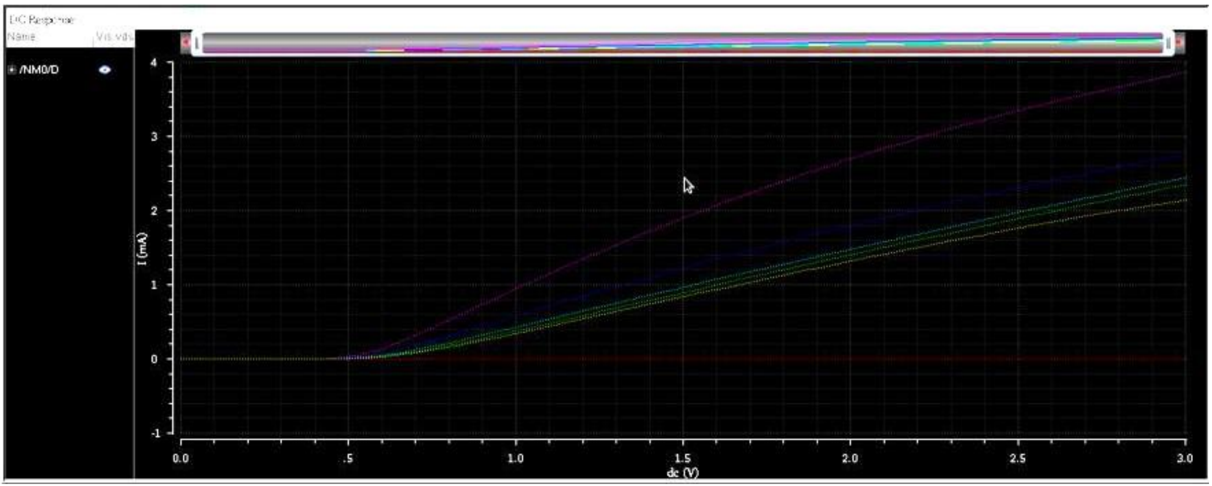
4. Go to Outputs → Select on Schematic → choose ID.
5. Run the simulation to get ID vs VDS graph.
6. Observe:
    - Linear region (small VDS)
    - Saturation region (VDS > VGS − VTH)

<u>Graphs and Observations</u>:

nMOS:

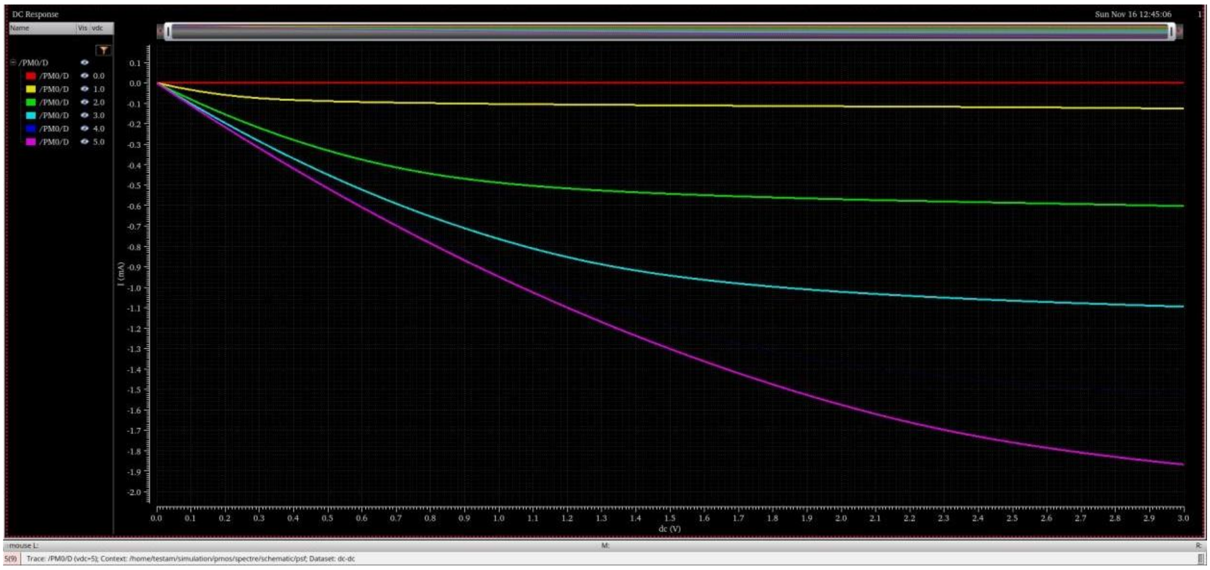


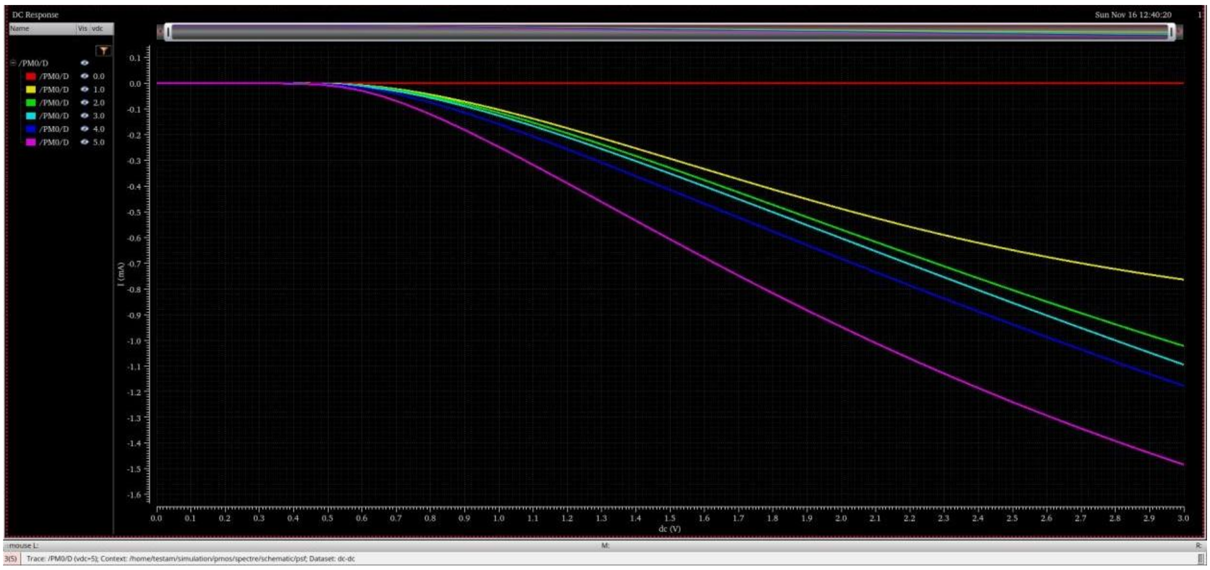
ID vs VGS (Transfer): current ≈ 0 until VGS ≈ VTH; beyond VTH, ID rises (nearly quadratic in ideal model) — use intercept to estimate VTH.



- In the **ID vs VDS** graph, observe the **linear region** and **saturation region** of the NMOS transistor.
- The **ID vs VGS** curve shows the **threshold voltage (VTH)** where conduction starts.
- Drain current increases with higher VGS due to stronger channel formation.

pMOS:





Layout:

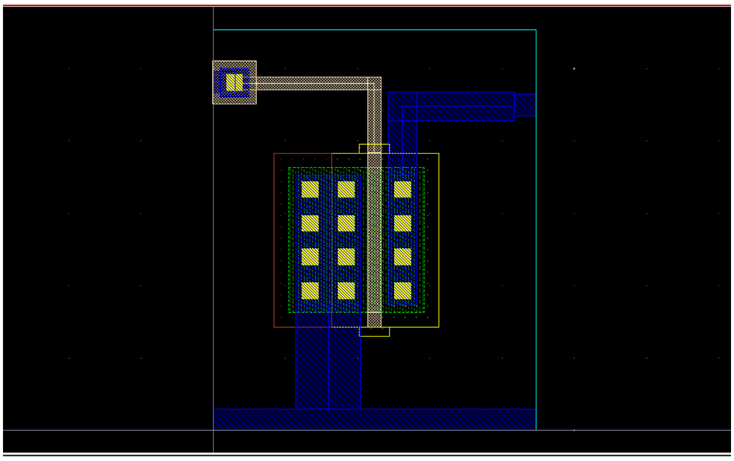


Fig: nmos Layout

Outcome:

- The **Transfer** and **Drain** characteristics of NMOS were successfully simulated using **Cadence Virtuoso**.
- The experiment demonstrates:
  - Relationship between **ID**, **VGS**, and **VDS**.
  - **Saturation** and **Ohmic regions** of NMOS operation.
  - Extraction of **Threshold Voltage (VTH)** from the ID-VGS curve.