

ECE 5003 – CMOS DIGITAL IC DESIGN



VIT-AP

UNIVERSITY

Fall Semester 2025-26

M. Tech VLSI DESIGN

School of Electronics Engineering (SENSE)

Engineering Lab report

Submitted to

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Submitted By

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Registration Number - 25MVD7036

TABLE OF CONTENTS

S. No.	Name of the Experiment	Date of Experiment	Page No
1.	Design and Implementation of a CMOS Inverter	27/09/2025	3-5
2.	Design and Implementation of a CMOS NAND GATE	04/10/2025	6-9
3.	Design and Implementation of a CMOS NOR Gate	11/10/2025	10-13
4.	Design and Implementation of a FULL Adder	25/10/2025	14-16
5.	Design and Implementation of a D-Flip Flop	15/11/2025	17-18
6.	Design and Implementation of a 6T-SRAM	06/12/2025	19-20

Experiment No.1

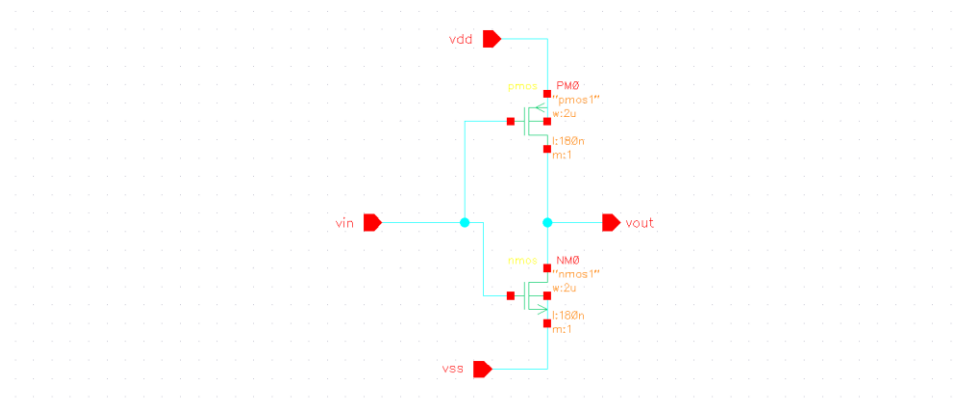
Design and Implementation of a CMOS Inverter

Aim: To design, simulate, layout, and verify a CMOS inverter using Cadence Virtuoso.

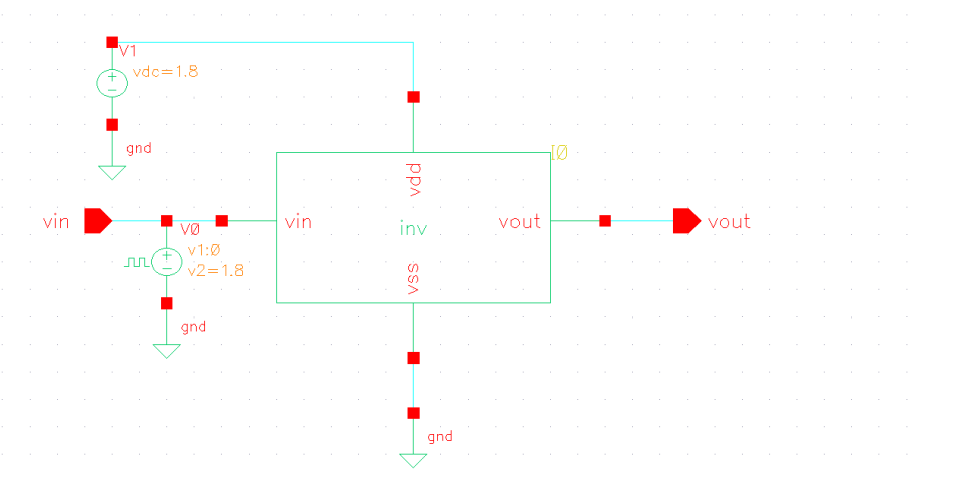
Tools Used: Cadence Virtuoso

- Cadence Virtuoso Schematic Editor – Schematic design
- Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations
- Cadence Spectre Simulator – Circuit simulation engine
- Cadence Virtuoso Layout Editor – Layout creation
- Cadence PVS / Assura – DRC and LVS verification
- Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

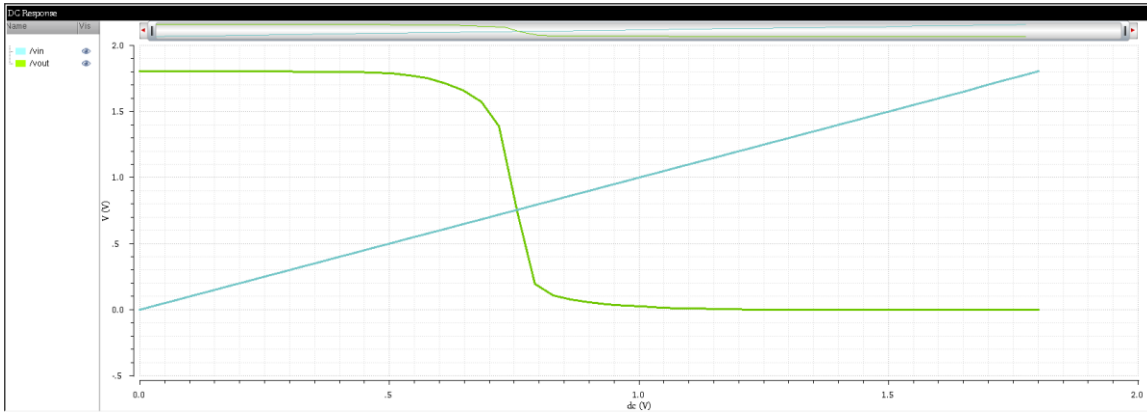
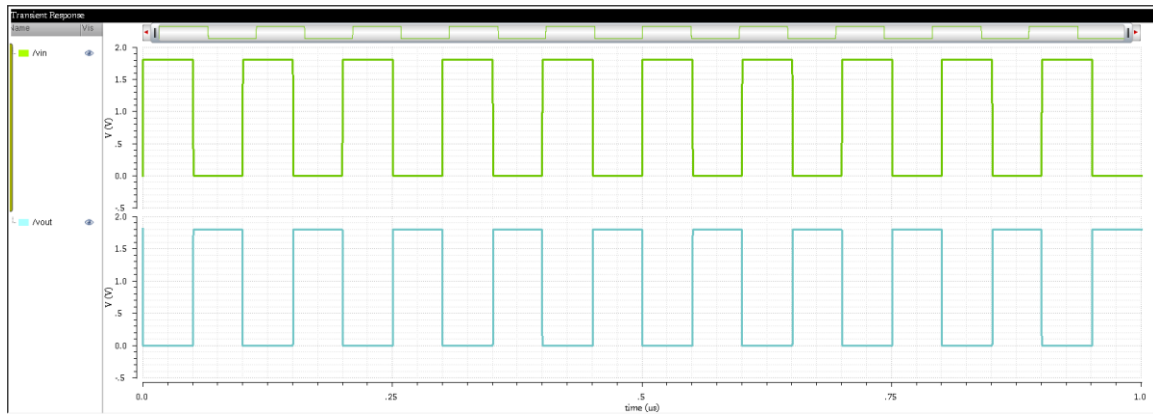
Schematic Diagram:



Test Schematic:



Simulation Waveforms (Pre-Layout):



ADE L Window:

Virtuoso® Analog Design Environment (1) - lab1 inv_tb schematic

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help

Design Variables

Name	Value

Analyses

Type	Enable	Arguments
1 dc	<input checked="" type="checkbox"/>	t 0 1.8 Automatic Start-Stop /V0
2 tran	<input checked="" type="checkbox"/>	0 1u moderate

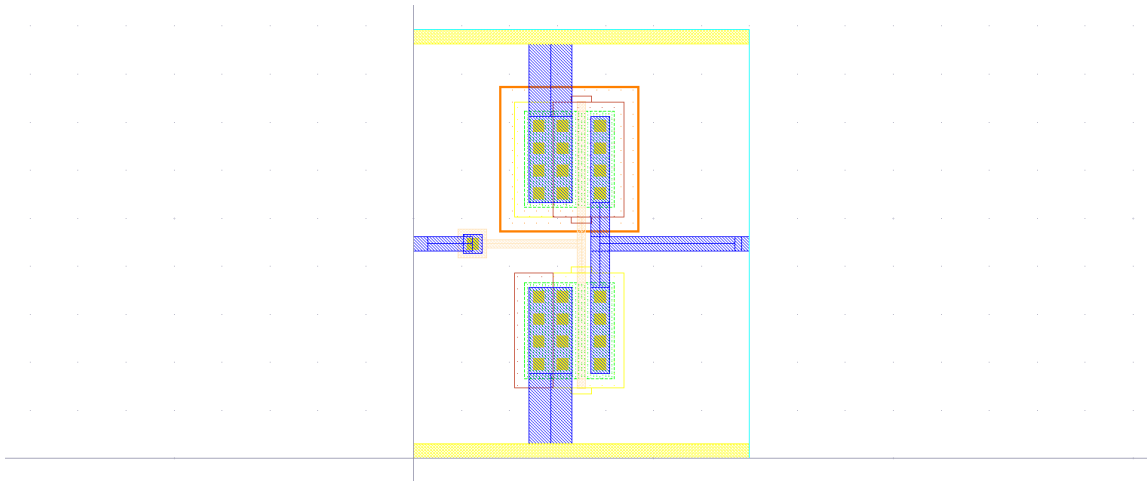
Outputs

Name/Signal/Expr	Value	Plot	Save	Save Options
1 vin		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
2 vout		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
3 tphi	85.2064p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
4 tphi	50.5n	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
5 rise time	35.5667p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
6 fall time	18.4294p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	

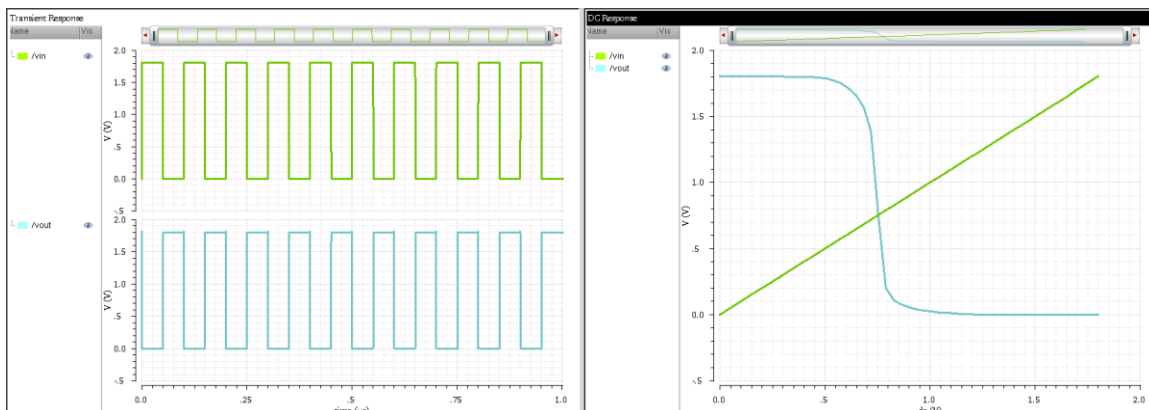
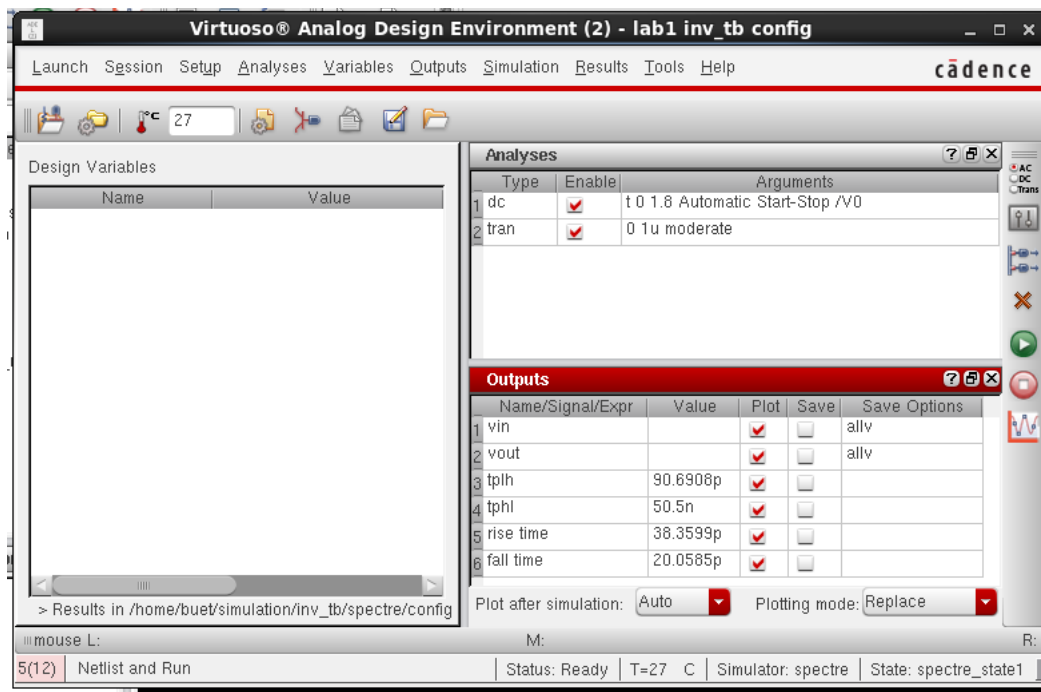
Plot after simulation: Auto Plotting mode: Replace

1(3) Stop Status: Ready T=27 C Simulator: spectre State: spectre_state1

Layout:



Post-Layout Simulation Results:



Experiment No.2

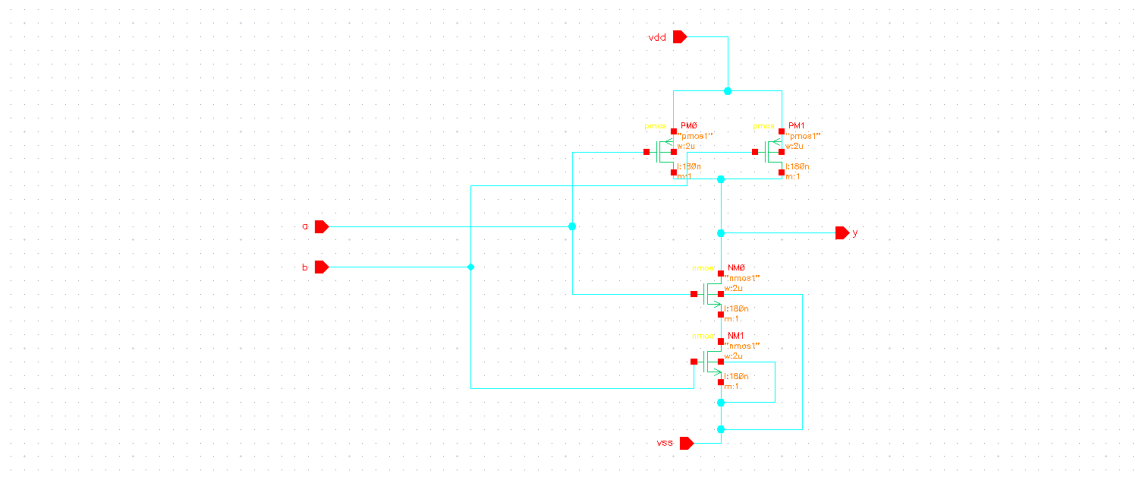
Design and Implementation of a CMOS NAND GATE

Aim: To design, simulate, layout, and verify a CMOS NAND Gate using Cadence Virtuoso.

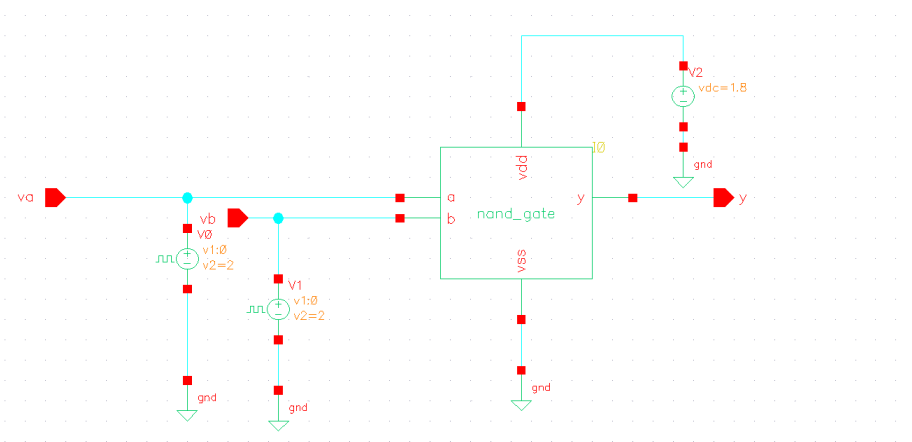
Tools Used: Cadence Virtuoso

- Cadence Virtuoso Schematic Editor – Schematic design
- Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations
- Cadence Spectre Simulator – Circuit simulation engine
- Cadence Virtuoso Layout Editor – Layout creation
- Cadence PVS / Assura – DRC and LVS verification
- Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

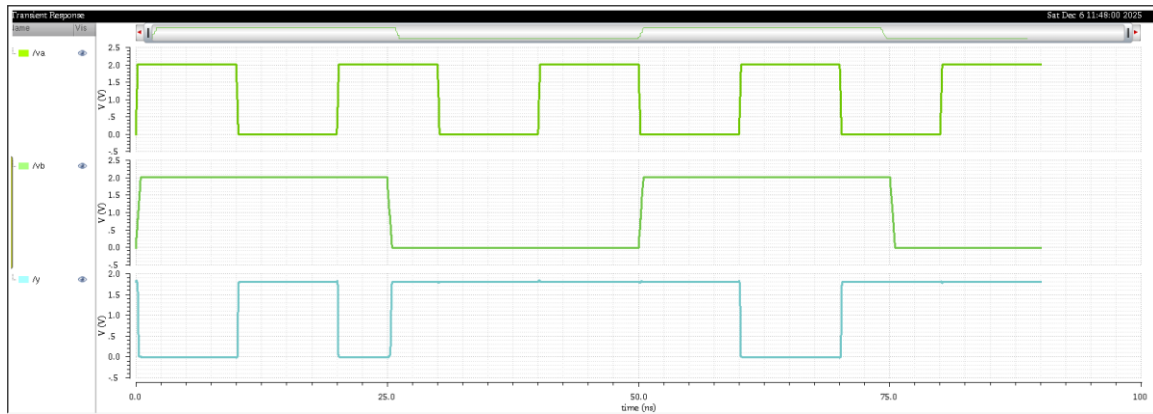
Schematic Diagram:



Test Schematic:



Simulation Waveforms (Pre-Layout):



ADE L Window:

Virtuoso® Analog Design Environment (5) - lab1 NAND_gate_test schematic

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Help

Design Variables

Name	Value
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Analyses

Type	Enable	Arguments
1 tran	<input checked="" type="checkbox"/>	0 90n moderate

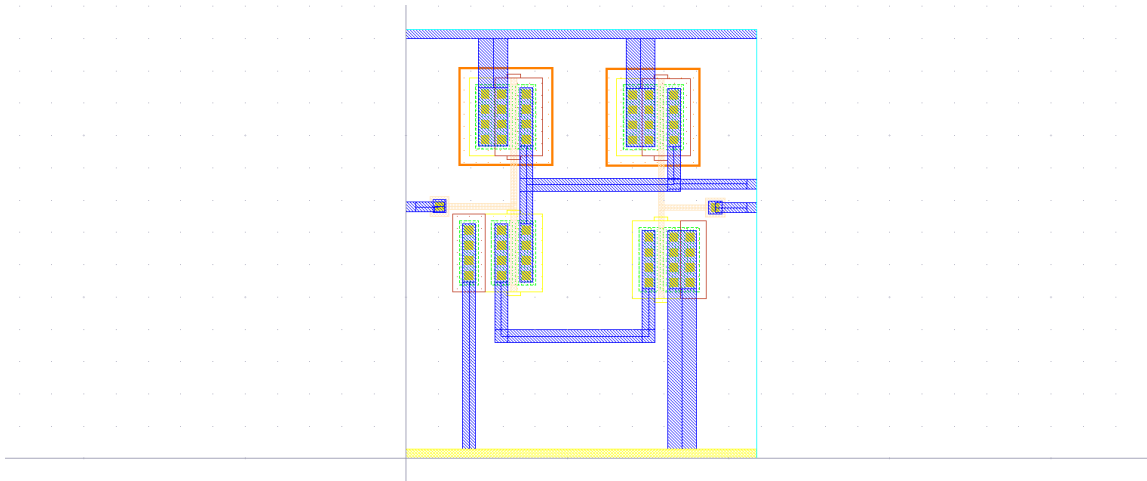
Outputs

Name/Signal/Expr	Value	Plot	Save	Save Options
1 fall time	33.1224p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
2 rise time	25.4203p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
3 tphi	26.6896p	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
4 tphi	-4.71439n	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
5 va		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
6 vb		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
7 y		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv

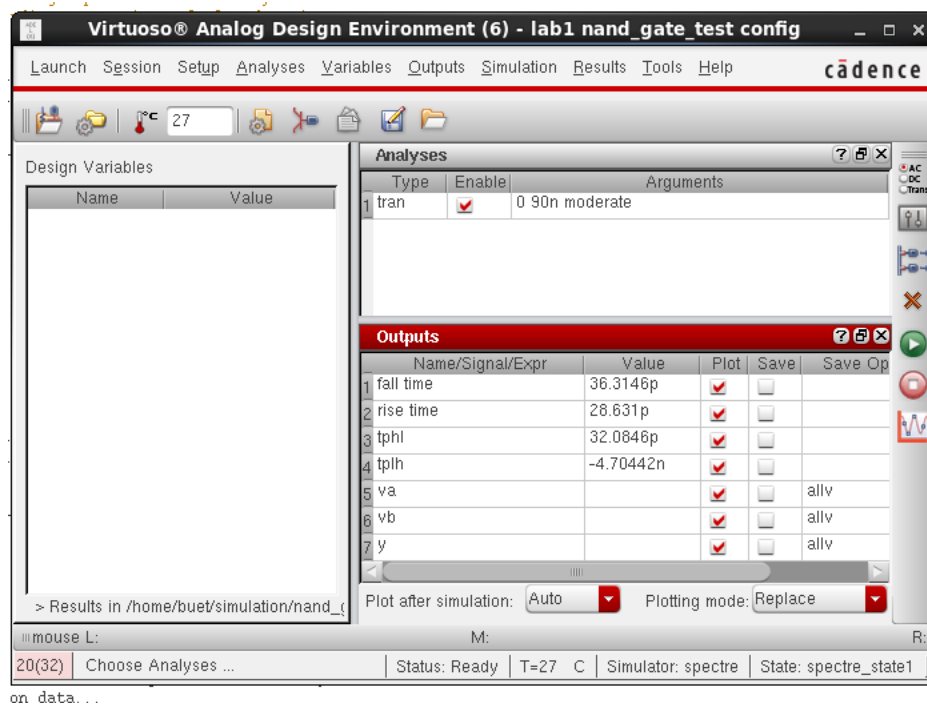
Plot after simulation: Auto Plotting mode: Replace

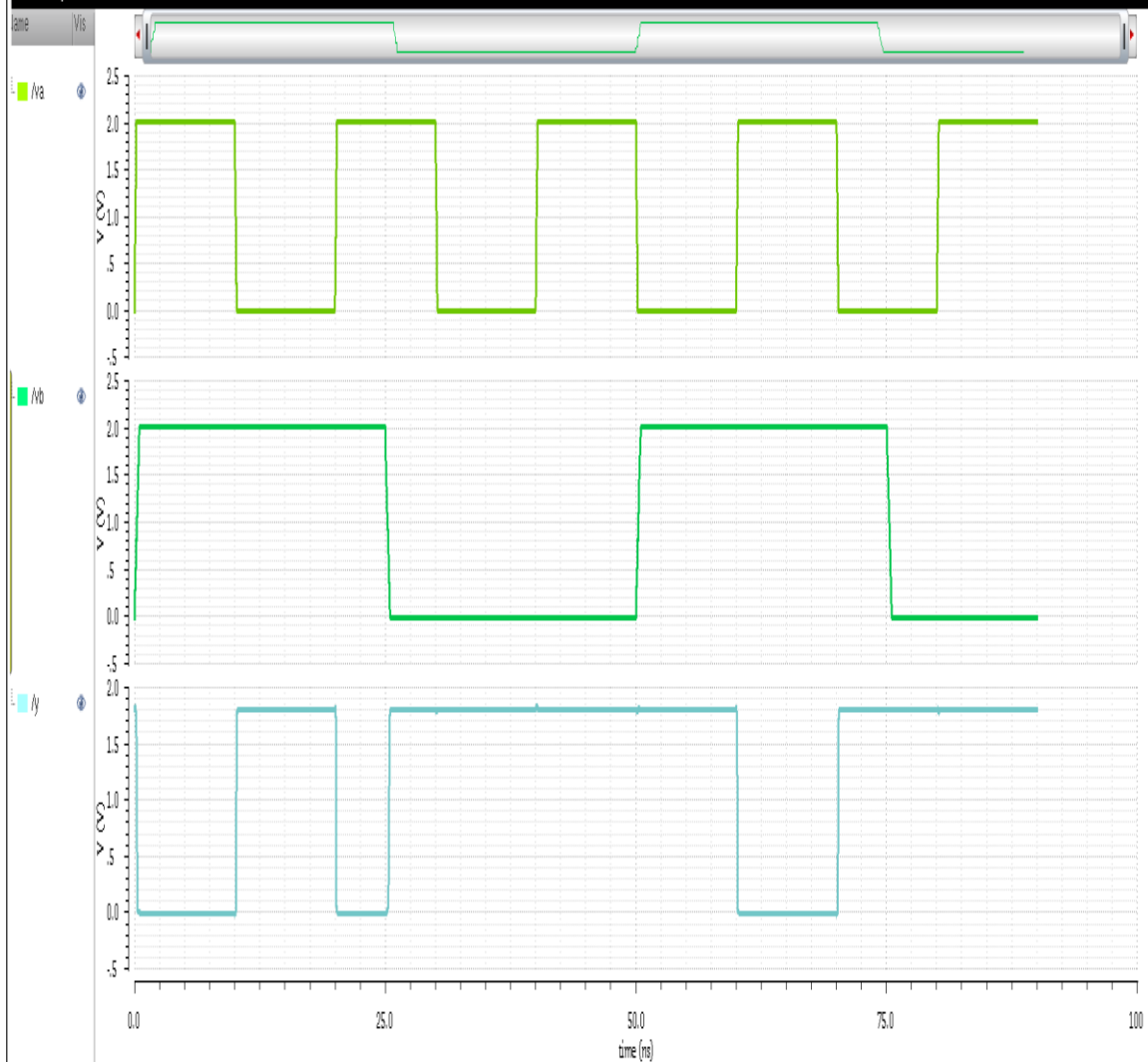
17(26) Plot Outputs Status: Ready T=27 C Simulator: spectre State: spectre_state1

Layout:



Post-Layout Simulation Results:





Experiment No.3

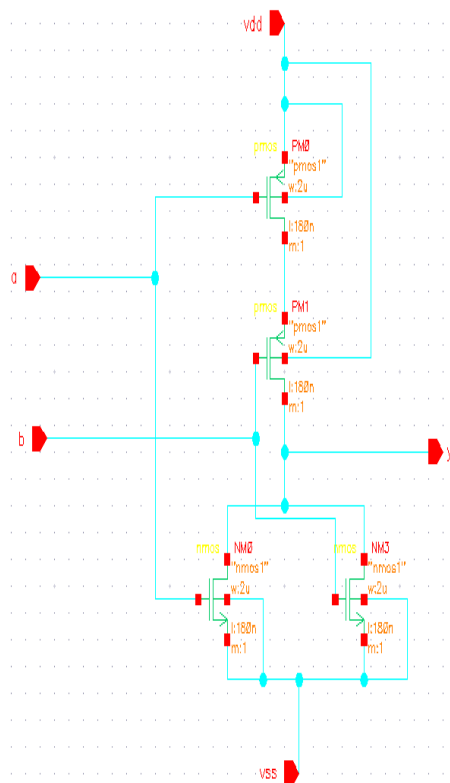
Design and Implementation of a CMOS NOR Gate

Aim: To design, simulate, layout, and verify a CMOS NOR Gate using Cadence Virtuoso.

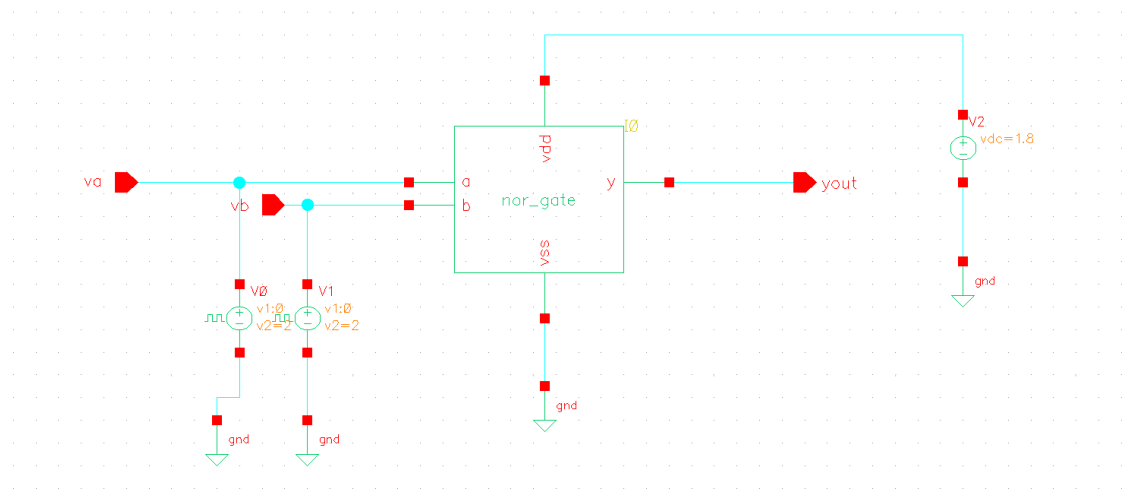
Tools Used: Cadence Virtuoso

- Cadence Virtuoso Schematic Editor – Schematic design
- Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations
- Cadence Spectre Simulator – Circuit simulation engine
- Cadence Virtuoso Layout Editor – Layout creation
- Cadence PVS / Assura – DRC and LVS verification
- Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

Schematic Diagram:



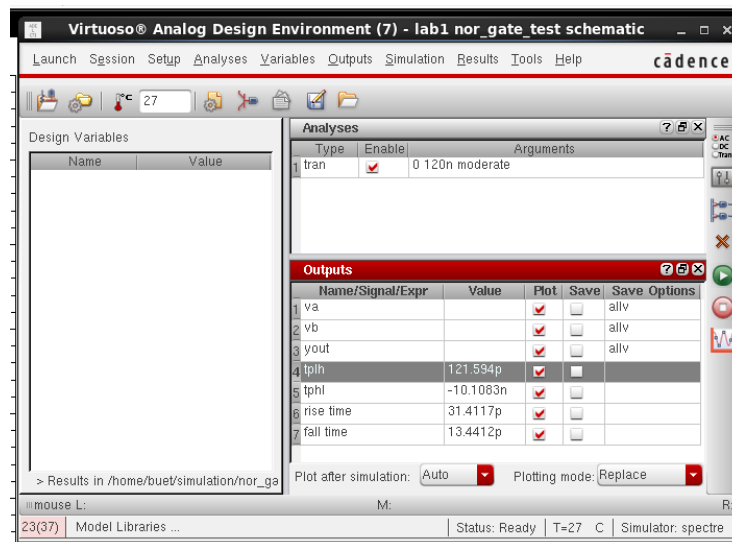
Test Schematic:



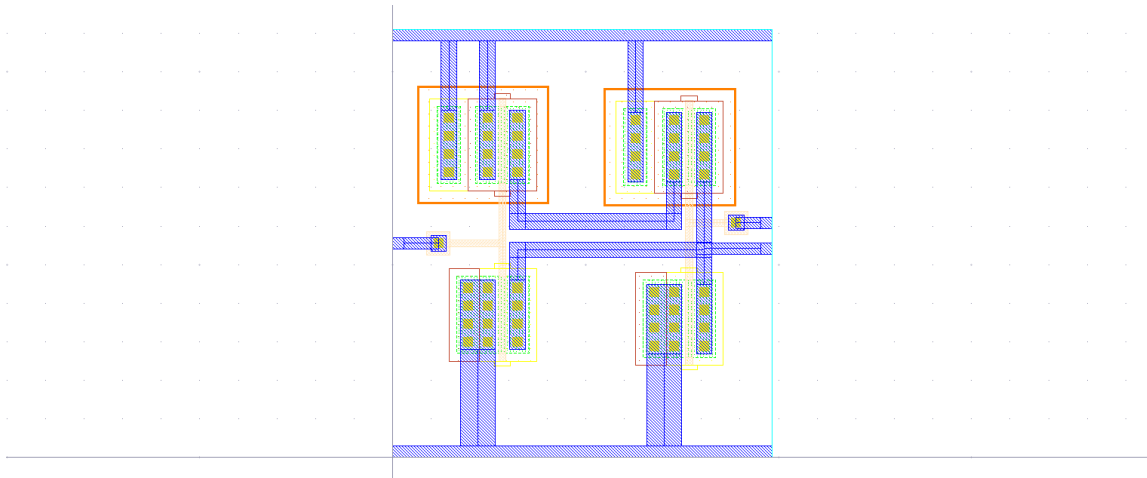
Simulation Waveforms (Pre-Layout):



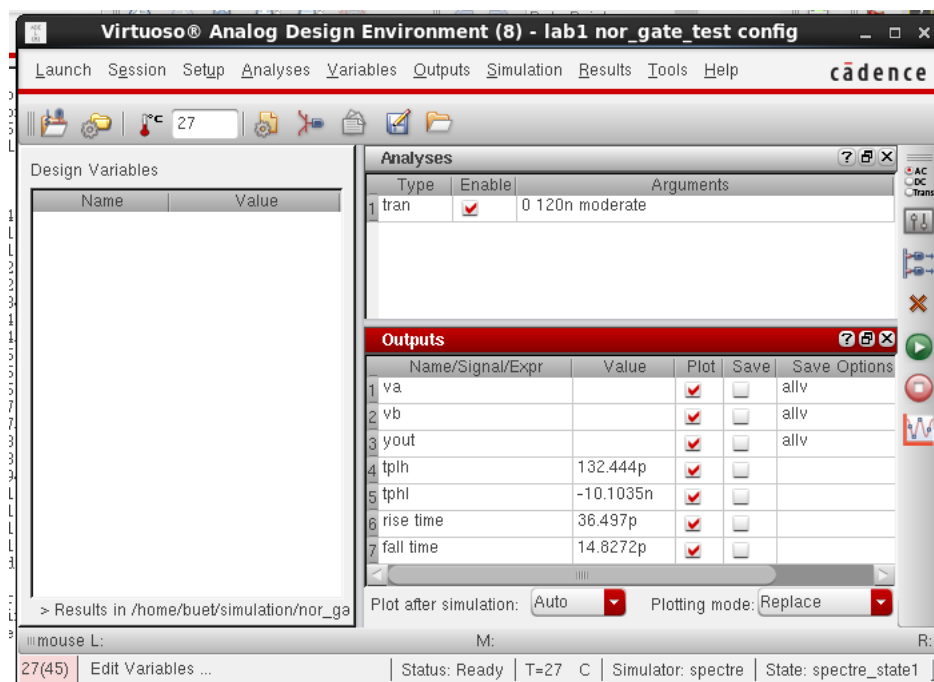
ADE L Window:

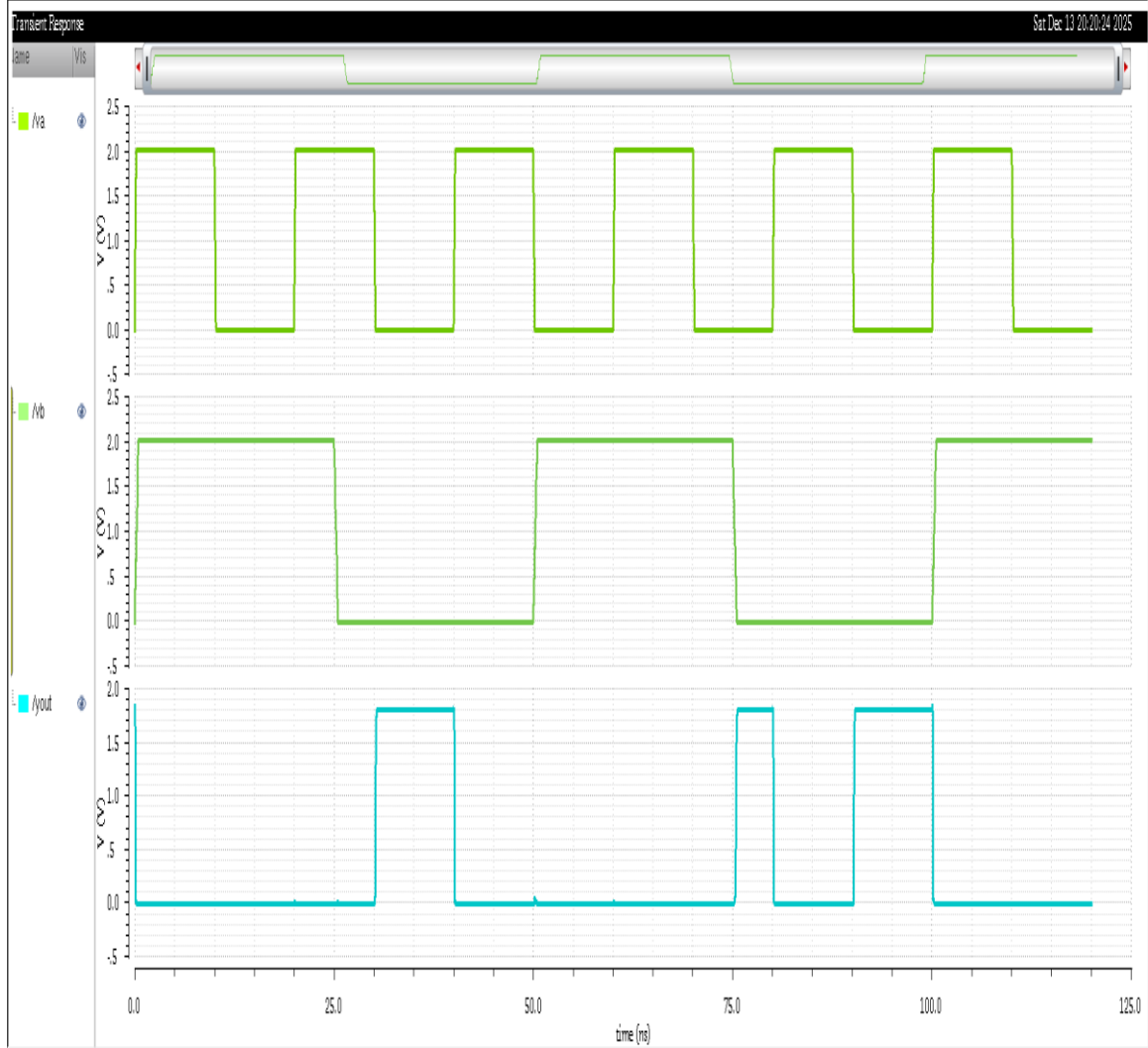


Layout:



Post-Layout Simulation Results:





Experiment No.4

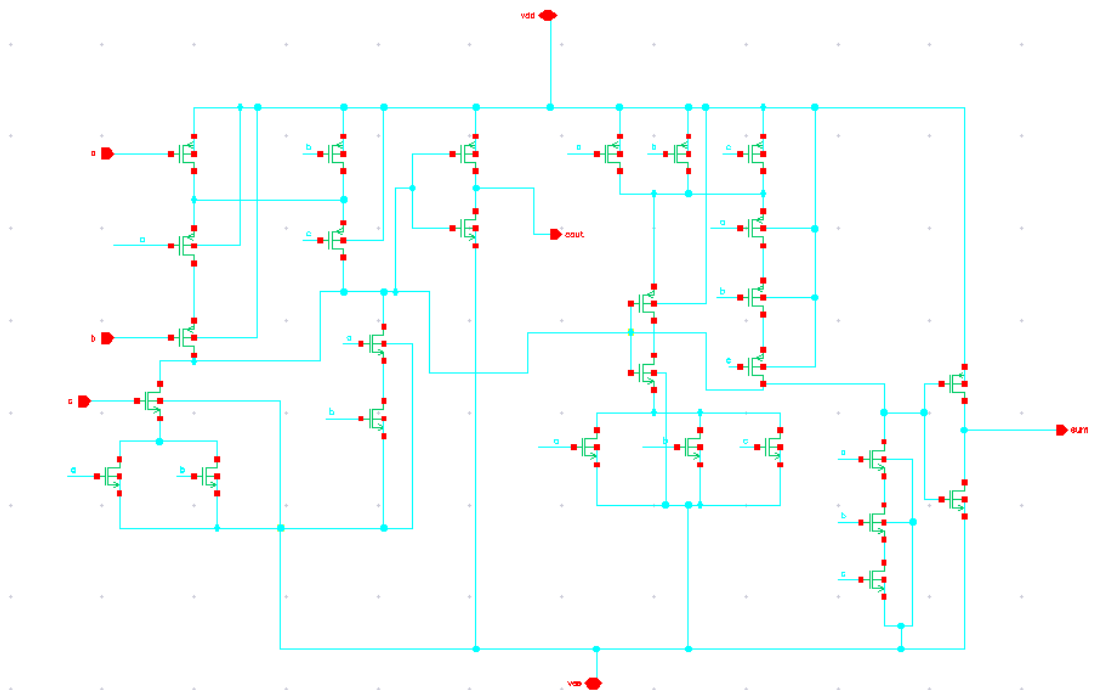
Design and Implementation of a FULL Adder

Aim: To design, simulate, layout, and verify a CMOS FULL Adder using Cadence Virtuoso.

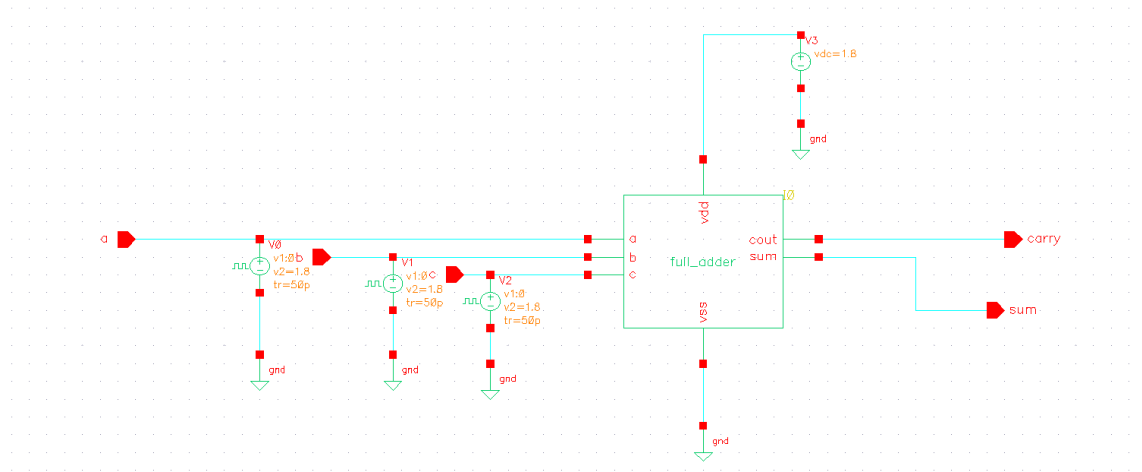
Tools Used: Cadence Virtuoso

- Cadence Virtuoso Schematic Editor – Schematic design
- Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations
- Cadence Spectre Simulator – Circuit simulation engine
- Cadence Virtuoso Layout Editor – Layout creation
- Cadence PVS / Assura – DRC and LVS verification
- Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

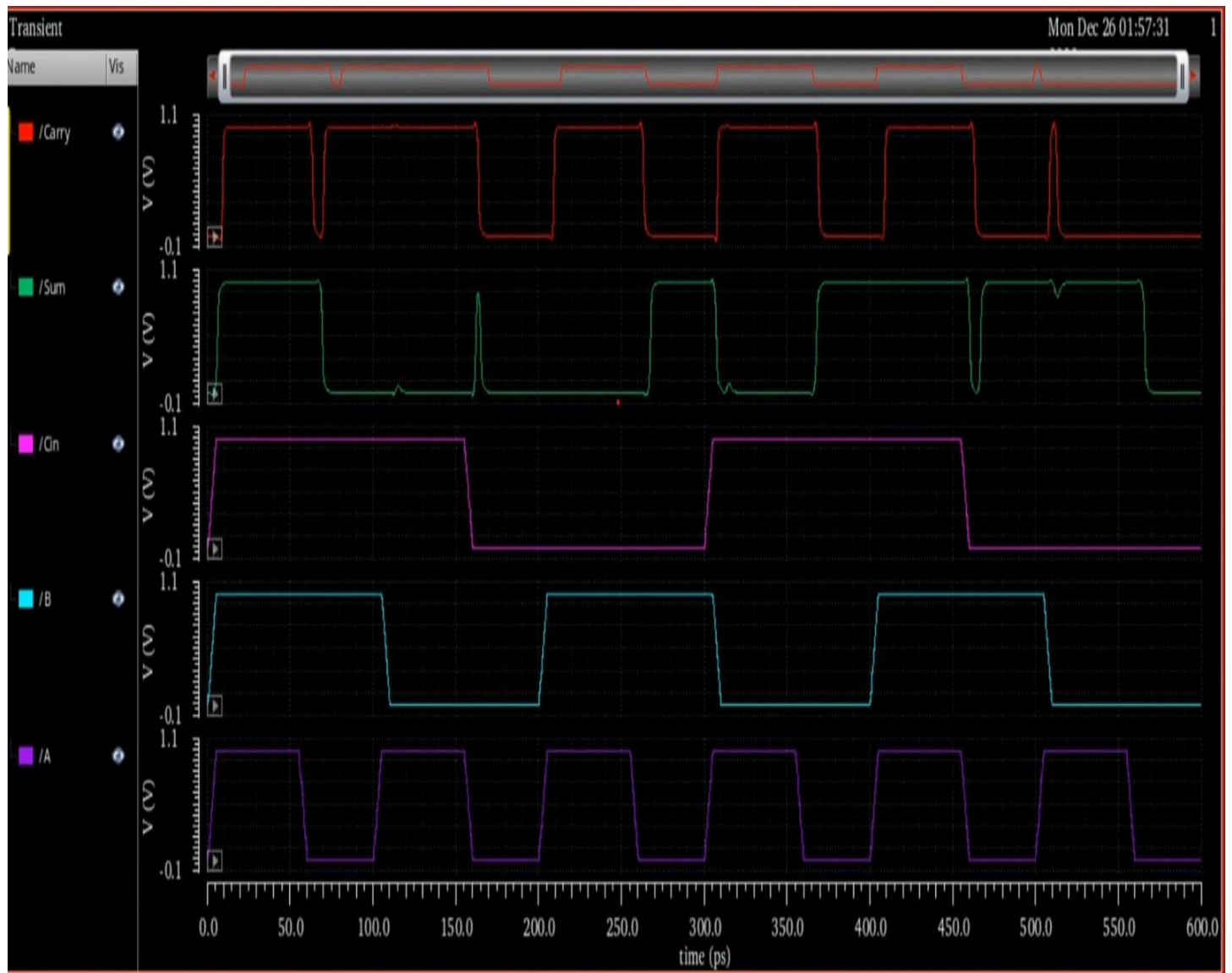
Schematic Diagram:



Test Schematic:



Simulation Waveforms (Pre-Layout):



ADE L Window:

ADE L (3) - TEST FA schematic

Launch Session Setup Analyses Variables Outputs Simulation Results Tools Calibre Help

27

Design Variables

Name	Value
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Analyses

Type	Enable	Arguments
1 tran	<input checked="" type="checkbox"/>	0 600p moderate

Outputs

Name/Signal/Expr	Value	Plot	Save	Save Options
1 A		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
2 B		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
3 Cin		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
4 Sum		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv
5 Carry		<input checked="" type="checkbox"/>	<input type="checkbox"/>	allv

> Select on Schematic Outputs to Be Plotted

Plot after simulation: Auto Plotting mode: Replace

7(27) | Status: Selecting outputs to be plotted... | T=27 C | Simulator: spectre

Experiment No.5

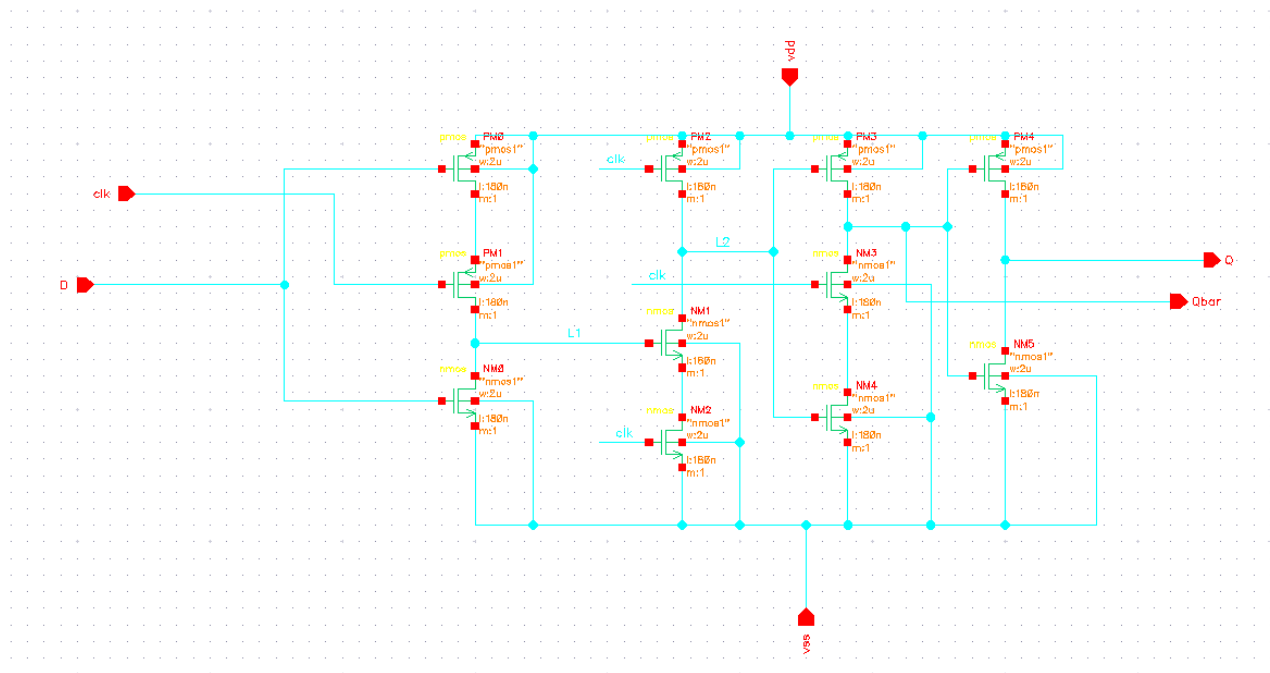
Design and Implementation of a D-Flip Flop

Aim: To design, simulate, layout, and verify a CMOS XOR Gate using Cadence Virtuoso.

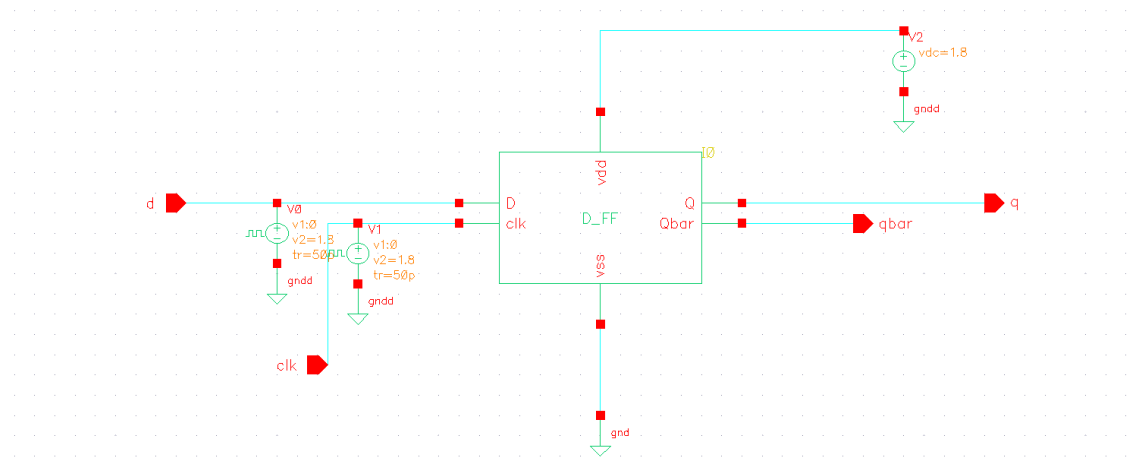
Tools Used: Cadence Virtuoso

- Cadence Virtuoso Schematic Editor – Schematic design
- Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations
- Cadence Spectre Simulator – Circuit simulation engine
- Cadence Virtuoso Layout Editor – Layout creation
- Cadence PVS / Assura – DRC and LVS verification
- Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

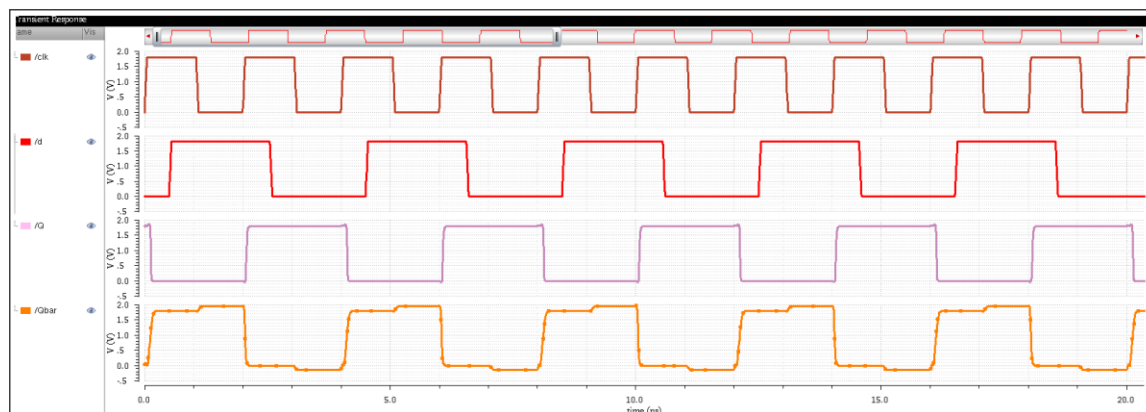
Schematic Diagram:



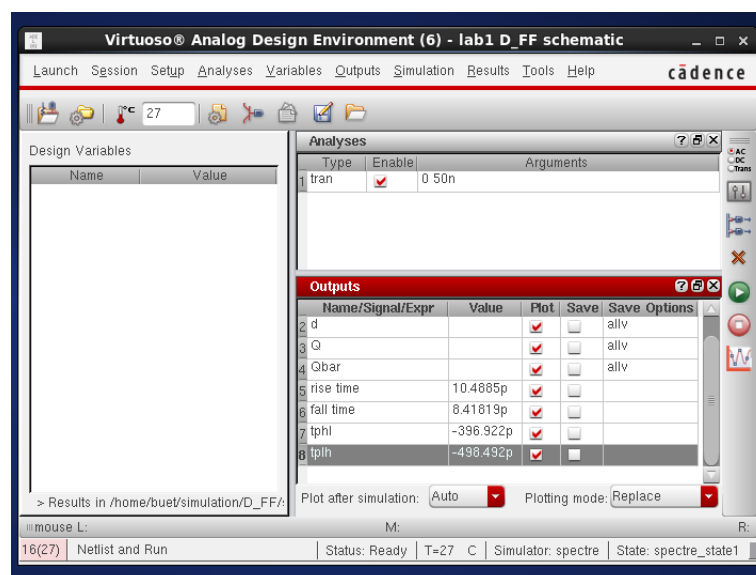
Test Schematic:



Simulation Waveforms (Pre-Layout):



ADE L Window:



Experiment No.6

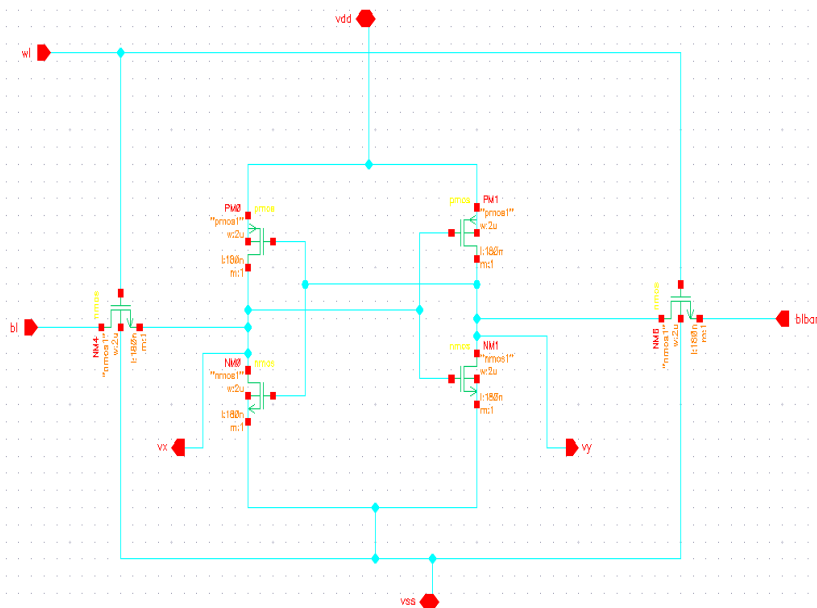
Design and Implementation of a 6T-SRAM

Aim: To design, simulate, layout, and verify a CMOS XOR Gate using Cadence Virtuoso.

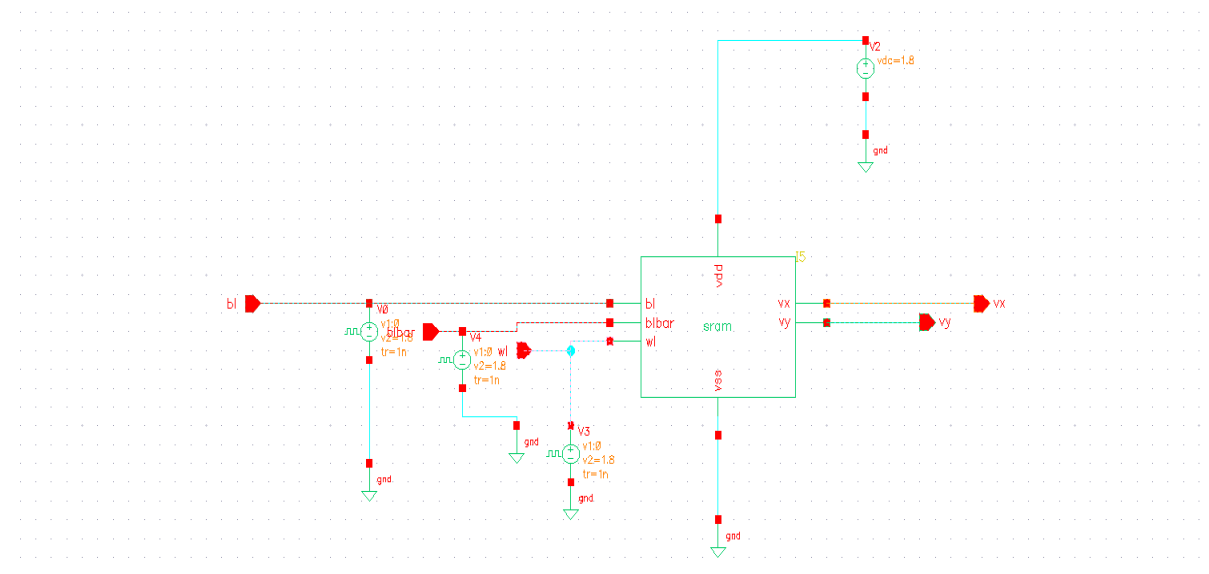
Tools Used: Cadence Virtuoso

- Cadence Virtuoso Schematic Editor – Schematic design
- Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations
- Cadence Spectre Simulator – Circuit simulation engine
- Cadence Virtuoso Layout Editor – Layout creation
- Cadence PVS / Assura – DRC and LVS verification
- Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

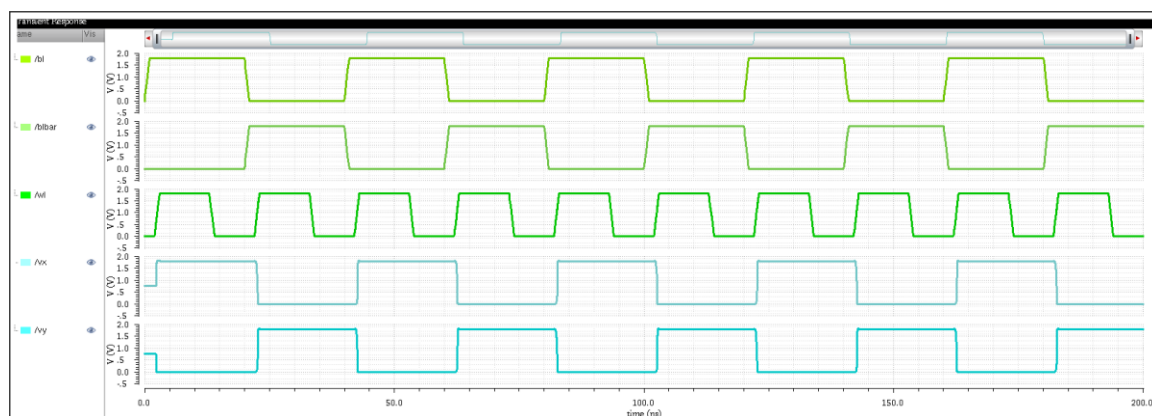
Schematic Diagram:



Test Schematic:



Simulation Waveforms (Pre-Layout):



ADE L Window:

