EXPERIMENT - 09

SINGLE STAGE OPERATIONAL AMPLIFIER

Aim: To design, simulate, and implement the schematic and physical layout of a MOSFET Single stage operational amplifier using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm.

Theory: A single-stage op-amp is the simplest building block that provides voltage gain in one amplifier stage. Common MOS implementations:

- Common-source (CS) amplifier with active load — an NMOS input transistor with a PMOS current-mirror (or PMOS load) producing a high gain and single inverting stage.
- Common-source differential pair (single-ended output) — a single differential pair where one side is used and the other tied to reference (less common as "single-stage" output).

In this report we consider a single common-source stage with an active PMOS load (current mirror), biased by current sources. The stage is inverting: a small positive change at the gate produces a negative change at the output node.

For a single common-source stage with transistor M1 (input) and an active PMOS load whose small-signal resistance is $r_{o,load}$, the small-signal voltage gain (single-ended) is approximately:

$$A_v \approx -g_{m1} \cdot R_{out}$$

where the output resistance R_{out} is the parallel combination of the output resistances seen at the node:

$$R_{out} \approx r_{o1} \parallel r_{o,load}$$

So,

$$A_v \approx -g_{m1}(r_{o1} \parallel r_{o,load})$$

Procedure

Follow the techniques, create a New Library using the option "File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:

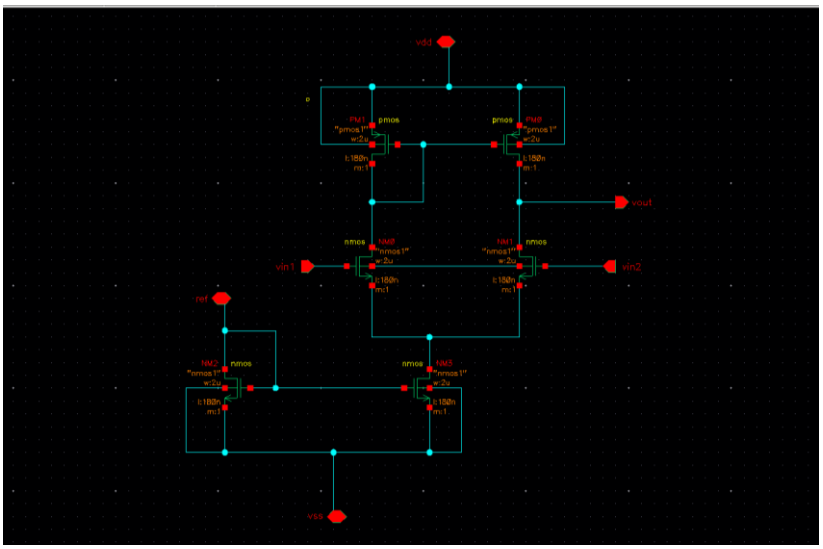


Fig: Schematic of Single Stage Operational Amplifier

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Single stage operational amplifier, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

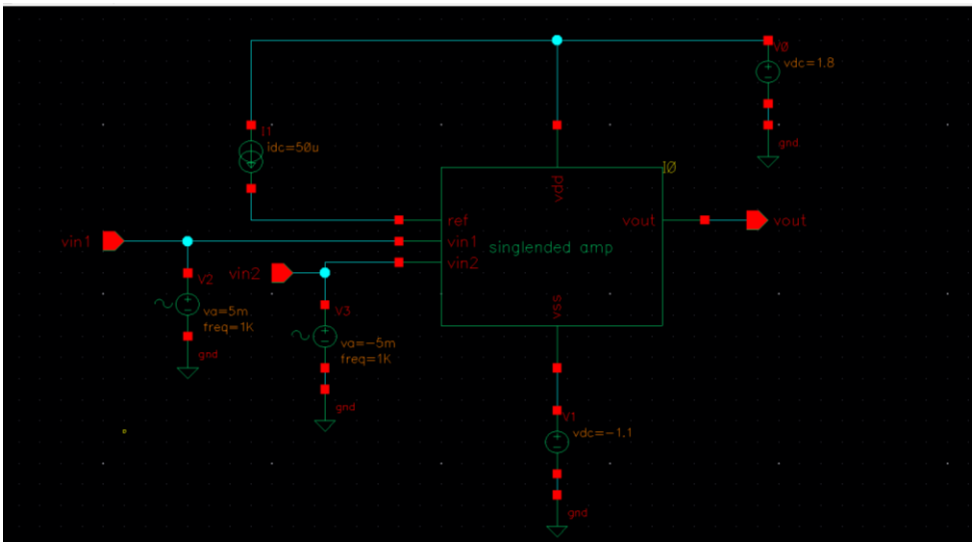


Fig: Test bench schematic of Single Stage Operational Amplifier

Properties of vdc and vsin:

Library Name	Cell Name	Properties
AnalogLib	vdc	DC voltage = 1.8V
AnalogLib	vdc	DC voltage = -1.1V
AnalogLib	vsin	AC magnitude = 1V Amplitude = 5m Frequency = 1KHz
AnalogLib	vsin	AC magnitude = 1V AC Phase = 180 Amplitude = -5m Frequency = 1KHz
AnalogLib	idc	DC current = 50u

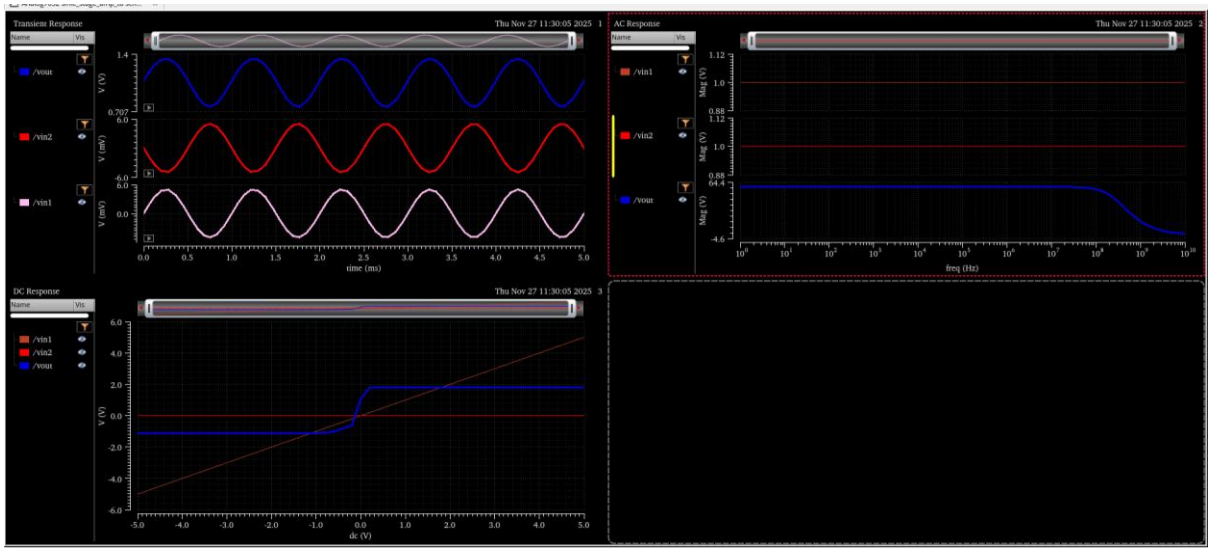
Simulation:

Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "-5" and "Stop" value as "5", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "1" and "Stop" value as "10G", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".



Layout:

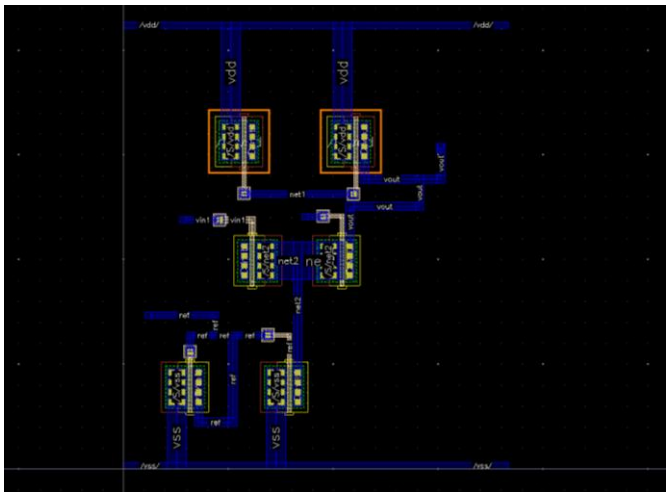


Fig: Single Stage Operational Amplifier layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura → Quantus", select "Technology →gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type →RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

Conclusion:

The Single Stage Operational Amplifier was successfully designed and implemented using Cadence Virtuoso. Pre- layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.