EXPERIMENT - 05

COMMON DRAIN

Aim: To design, simulate, and implement the schematic and physical layout of a MOSFET common drain using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm

Theory: The common-drain amplifier, also known as the source follower, is a MOSFET configuration in which the drain terminal is held at AC ground (usually connected to V_{DD} or through a large bypass capacitor), the input signal is applied to the gate, and the output is taken from the source. Because the output follows the input with a small voltage drop, the circuit behaves similarly to a voltage buffer.

In the common-drain configuration, the MOSFET operates in saturation, where the drain current is given by

$$I_D = \frac{1}{2} k_n (V_{GS} - V_{th})^2.$$

Since the drain is at a fixed voltage, variations in the gate voltage directly influence V_{GS}, which in turn modulates the source voltage. When the source resistor R_S is present, the output voltage is approximately:

$$v_o \approx v_i - V_{GS}.$$

Because V_{GS} is relatively constant for small-signal operation, the output "follows" the input. Using the small-signal hybrid-π model, the output voltage is determined by the transconductance g_m and the source resistance:

$$v_o = \frac{g_m R_S}{1 + g_m R_S} v_i.$$

Thus, the voltage gain A_v is:

$$A_v = \frac{v_o}{v_i} = \frac{g_m R_S}{1 + g_m R_S}.$$

For large $g_m R_S$:

$$A_v \approx 1.$$

Because the gate of a MOSFET is insulated, the input sees only the gate capacitances:

$$R_{in} \approx \infty,$$

making the common-drain a very good voltage buffer.

The output impedance is dominated by the source resistance and MOSFET small-signal parameters:

$$R_{out} \approx \frac{1}{g_m} \parallel r_o.$$

Procedure

Follow the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library
using the option "File → New → Cell View" and instantiate the required devices using the
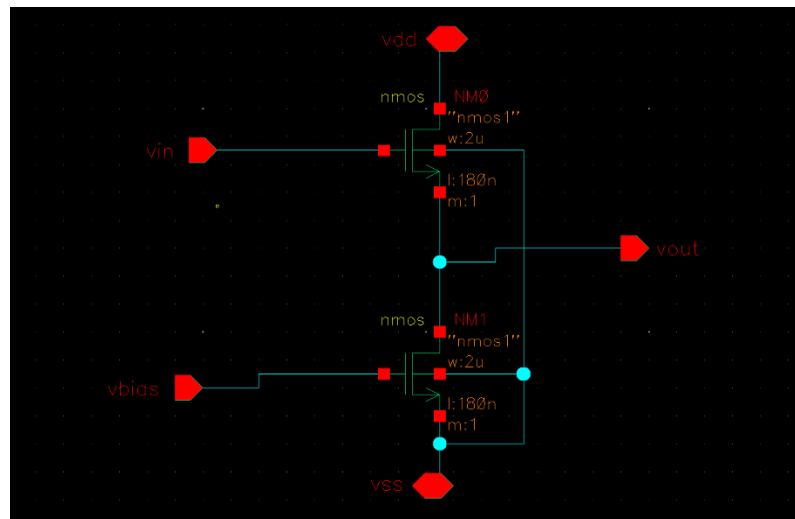"Create → Instance" option.

Schematic Diagram:

Fig: Schematic of Common Drain

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the
symbol of Common drain, DC Voltage Source, Current Source, AC Voltage Source, Resistance
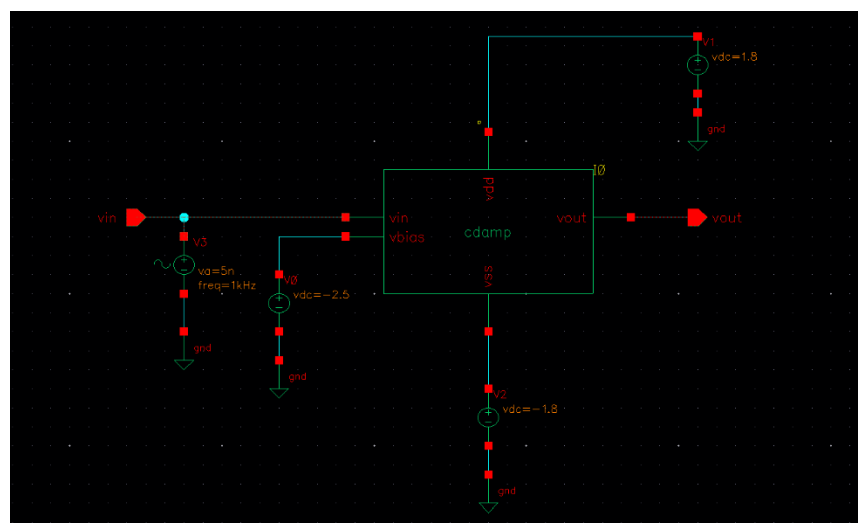and Ground, connect the using wires.

Fig: Test bench schematic of Common Drain

Properties of vdc and vsin:

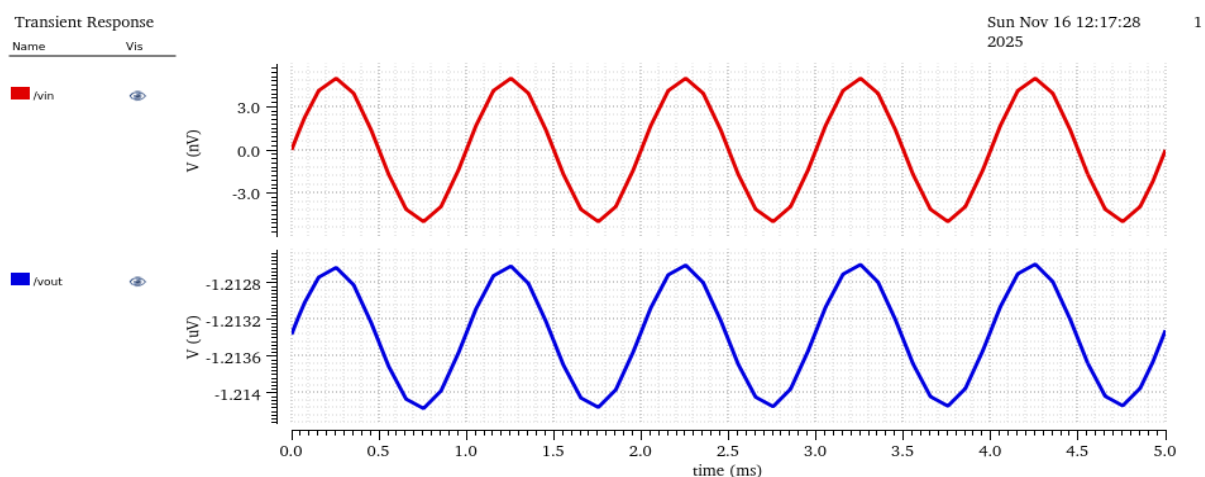| Library Name	Cell Name	Properties
AnalogLib	vdc	Vdd: DC voltage = 1.8V
AnalogLib	vdc	Vss: DC voltage = -1.8V
AnalogLib	vsin	AC magnitude = 1V Amplitude = 5nV Frequency = 1KHz
AnalogLib	Vdc	Vbias: DC voltage = -2.5V

Simulation:

Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "-1" and "Stop" value as "1", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "1" and "Stop" value as "10M", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".
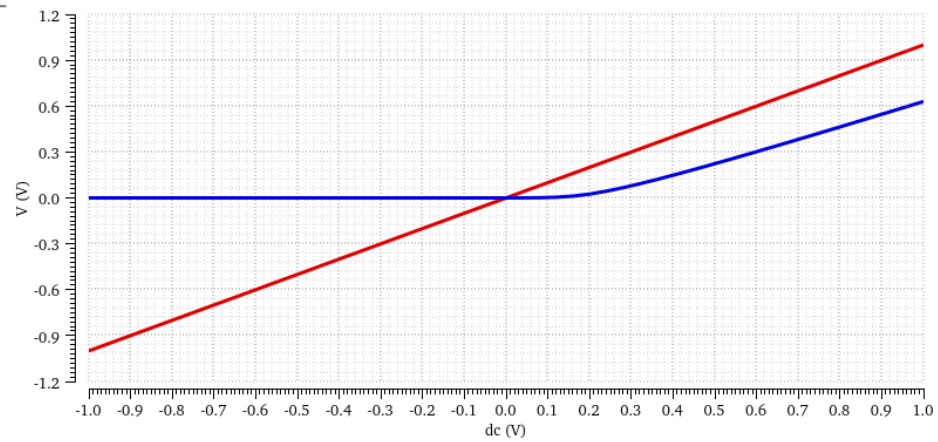
Transient Response:

DC Response:

DC Response

Name	Vis
/vin	👁
/vout	👁

AC Response:

AC Response

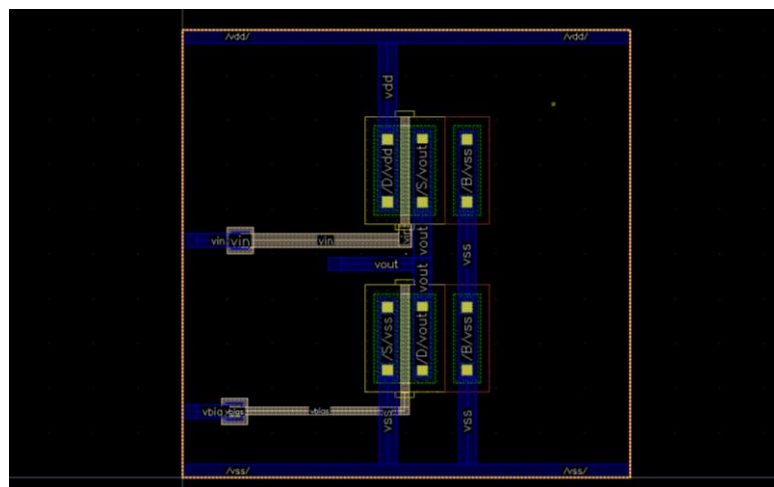| Name	Vis
/vin	👁
/vout	👁
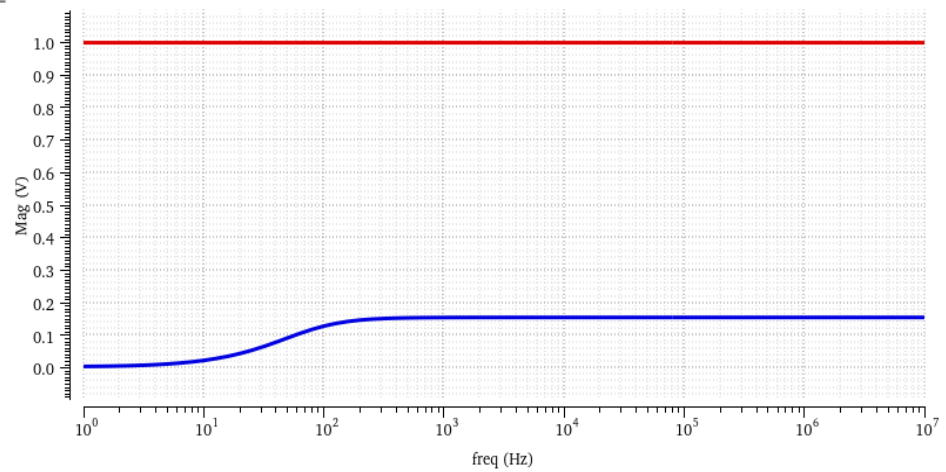
Layout:

Fig: Common Drain layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura → Quantus", select "Technology →gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type →RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

Conclusion:

The common drain was successfully designed and implemented using Cadence Virtuoso. Pre-layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.