EXPERIMENT - 04

COMMON GATE

Aim: To design, simulate, and implement the schematic and physical layout of a MOSFET common gate using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

Software & Technology Used: CADENCE VIRTUOSO, 180nm

Theory: The common-gate (CG) amplifier is a MOSFET configuration in which the gate terminal is AC-grounded, the input signal is applied to the source, and the output is taken at the drain. Because the input enters through the source terminal, the common-gate stage exhibits low input impedance, high output impedance, and moderate voltage gain, making it useful for high-frequency and current-mode applications.

In the common-gate configuration, the MOSFET is biased such that it operates in saturation, where the drain current is

$$I_D = \frac{1}{2} k_n (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}).$$

Using the small-signal hybrid-π model, the input small-signal current is

$$i_i = g_m v_{gs} + \frac{v_{ds}}{r_o}.$$

Since the gate is AC-grounded, $v_{gs} = -v_i$and the small-signal voltage gain becomes:

$$A_v = \frac{v_o}{v_i} = g_m R_D \parallel r_o + 1.$$

In most practical cases, $g_m R_D \gg 1$, so the gain simplifies to:

$$A_v \approx g_m R_D.$$

The small-signal input impedance is:

$$R_{in} \approx \frac{1}{g_m}.$$

The drain terminal exhibits high output resistance:

$$R_{out} \approx r_o.$$

Procedure

Follow the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

Schematic Diagram:

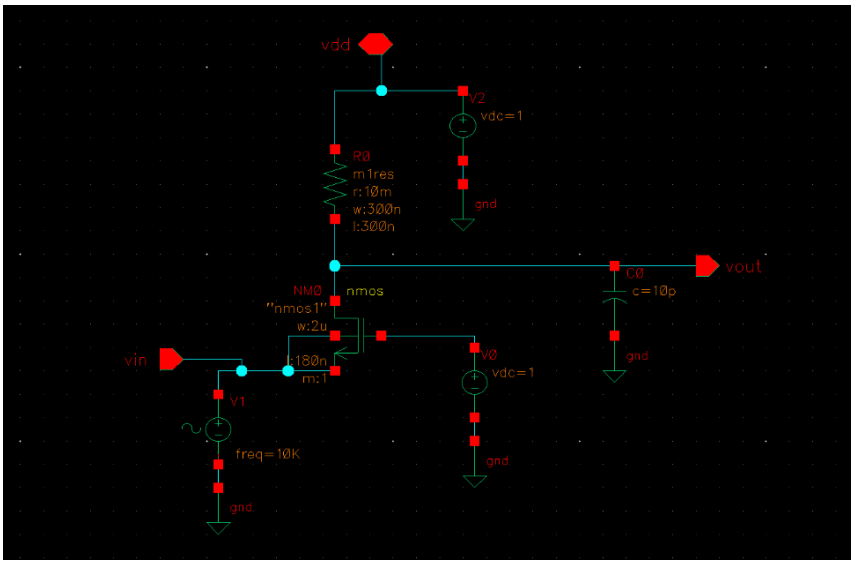


Fig: Schematic of Common Gate

Functional Stimulation:

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Common gate, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

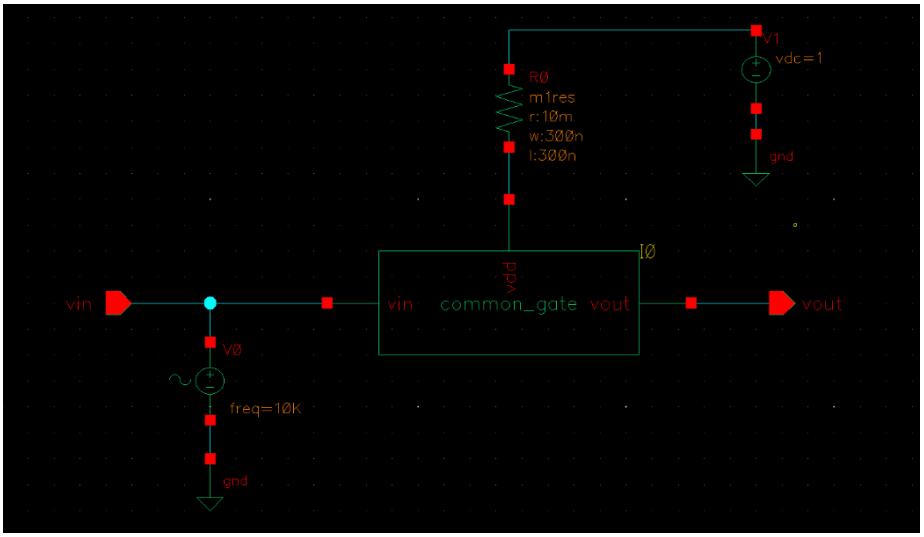


Fig: Test bench schematic of Common Gate

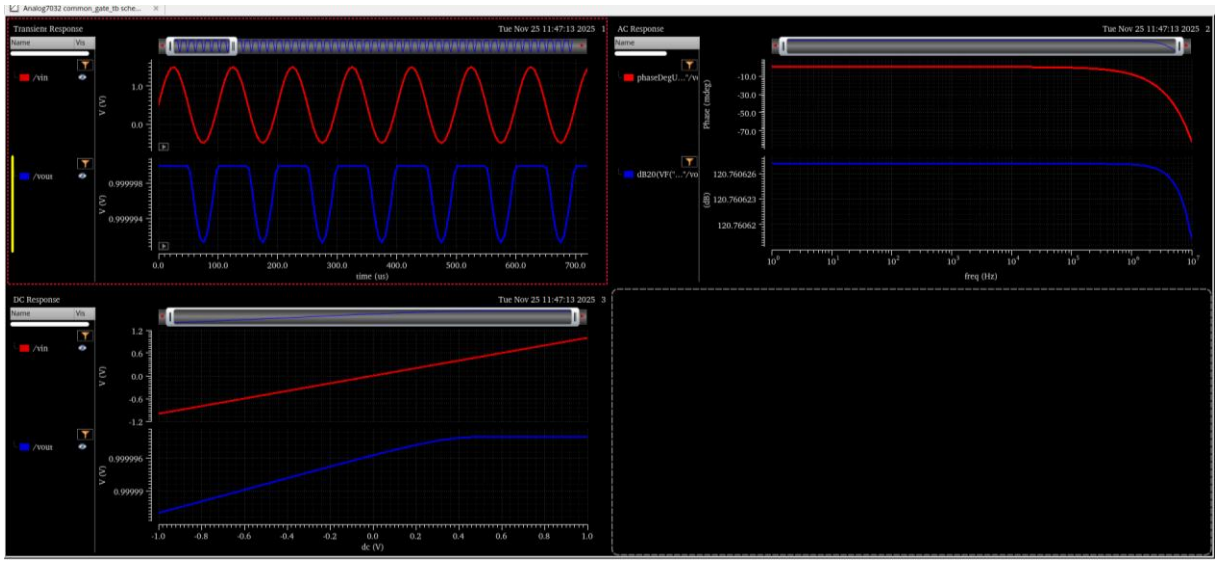
Simulation:

Launch ADE L, import the design variables, mention the values and select the Transient Analysis, DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**Transient Analysis**", select "trans", mention the Stop Time – 5m select Accuracy Defaults - moderate, click on "Apply" and click on "OK".

To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "-1" and "Stop" value as "1", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "1" and "Stop" value as "10M", and from "Sweep Type" option select – logarithmic, points per decade as "10", click on "Apply" and click on "OK".



<u>Layout</u>:

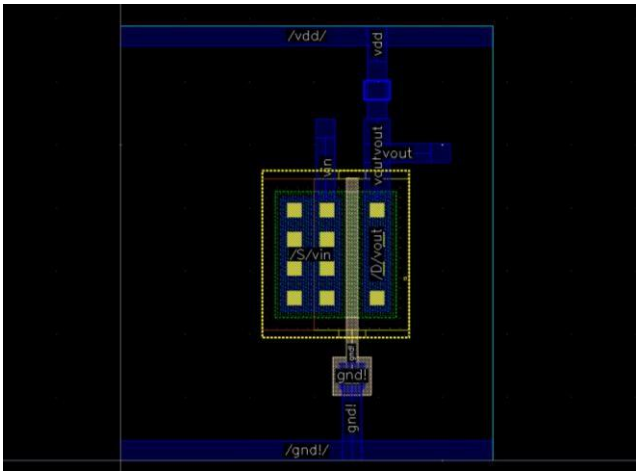


Fig: Common Gate layout

DRC:

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

LVS:

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

QRC:

To extract the Parasitics, select "Assura → Quantus", select "Technology →gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type → RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

Conclusion:

The common gate was successfully designed and implemented using Cadence Virtuoso. Pre-layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.