## EXPERIMENT - 07

## CURRENT MIRRORS

**Aim:** To design, simulate, and implement the schematic and physical layout of a MOSFET current mirrors using Cadence Virtuoso, ensuring correct biasing, gain performance, stability, and layout compliance with DRC and LVS rules.

**Software & Technology Used:** CADENCE VIRTUOSO, 180nm

**Theory:** A current mirror is a circuit block which functions to produce a copy of the current flowing into or out of an input terminal by replicating the current in an output terminal. An important feature of the current mirror is a relatively high output resistance which helps to keep the output current constant regardless of load conditions. Another feature of the current mirror is a relatively low input resistance which helps to keep the input current constant regardless of drive conditions. Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well. Or it can consist of a current-controlled current source (CCCS).

If M1 and M2 are identical and operate in the same region, ideally $I_{OUT} = I_{REF}$. If sizes differ:

$$I_{OUT} \approx I_{REF} \cdot \frac{(W/L)_2}{(W/L)_1}$$

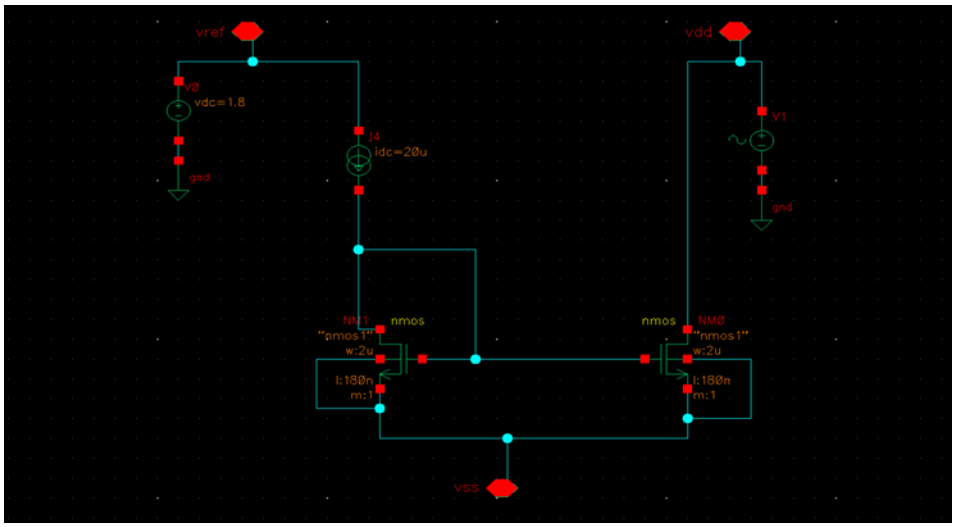
For MOS in saturation (approx):

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

**Procedure**

Follow the techniques, create a New Library using the option
"File → New → Library", create a New Cell View upon selecting the newly created library using the option "File → New → Cell View" and instantiate the required devices using the "Create → Instance" option.

**Schematic Diagram:**



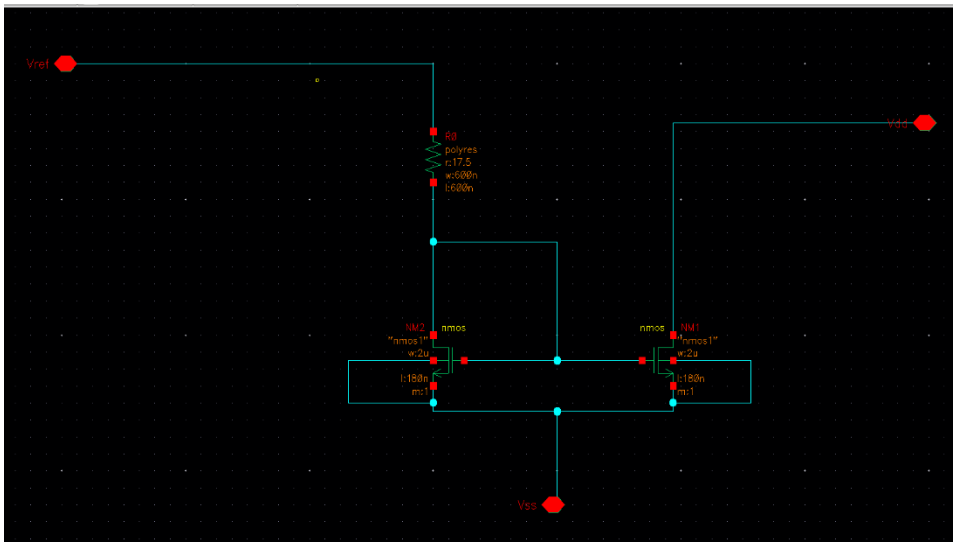



Fig: Schematic of Current Mirror

**Functional Stimulation:**

Using the symbol created, build the Test Schematic. Create a New Cell View, instantiate the symbol of Current mirror, DC Voltage Source, Current Source, AC Voltage Source, Resistance and Ground, connect the using wires.

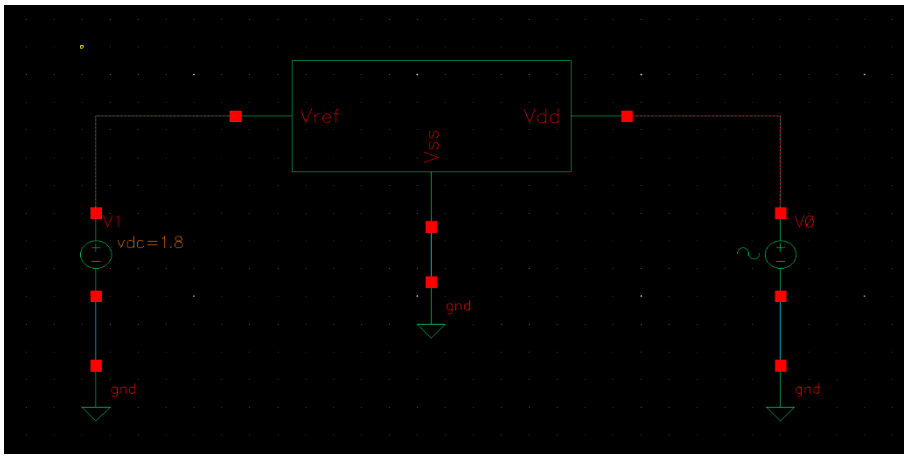



Fig: Test bench schematic of Current mirror

**Properties of vdc and vsin**

| Library Name | Cell Name | Properties |
|---|---|---|
| AnalogLib | Vdc | Vref: DC voltage = 1.8V |
| AnalogLib | Vsin | DC Voltage = 1V<br>AC Magnitude = 1V |

**Simulation:**

Launch ADE L, import the design variables, mention the values and select the DC Analysis and AC Analysis, mention the parameters and choose the signals to be plotted.

To set up a "**DC Analysis**", select "dc", select "DC Voltage" from the list of parameters as shown in the "Select Component Parameter" window and click on "OK". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "0" and "Stop" value as "1", click on "Apply" and click on "OK".

To set up a "**AC Analysis**", select "ac", select "frequency". From the "Sweep Range" option, select "Start-Stop" and mention the "Start" value as "1" and "Stop" value as "1G", click on "Apply" and click on "OK".

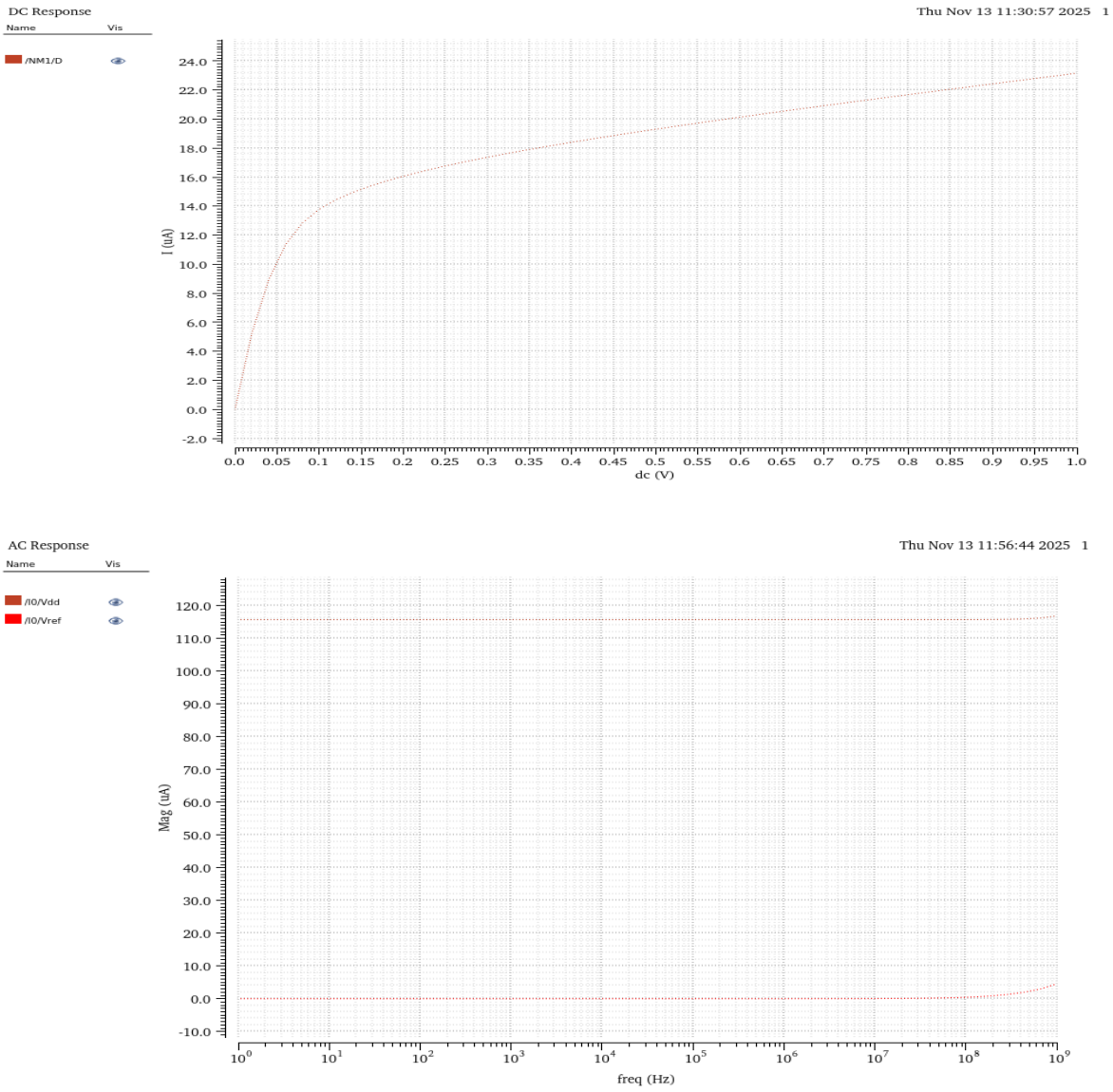



Fig: Pre-layout stimulation of Current mirror

**Layout:**

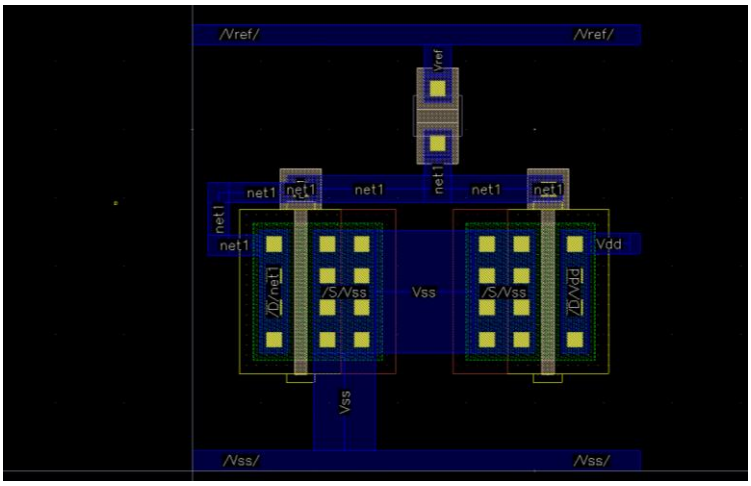



Fig: Current mirror layout

**DRC:**

To check for the DRC violations, browse the "assura_tech.lib" file, select "Assura → Run DRC", verify the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

**LVS:**

To check for the LVS violations, select "Assura → Run LVS", verify the Schematic Design Source and the Layout Design Source, mention a "Run Name", select "Technology → gpdk180" and click on "OK".

**QRC:**

To extract the Parasitics, select "Assura → Quantus", select "Technology → gpdk180", "Output → Extracted View" from the "Setup" option, select "Extraction Type → RC" and "Ref Node → VSS" from the "Extraction", Disable HRCX and click on "OK".

The result can be checked from the Library Manager.

**Conclusion:**

The current mirror was successfully designed and implemented using Cadence Virtuoso. Pre-layout and post-layout simulations confirm improved gain and bandwidth characteristics compared to a simple common-source amplifier. Layout verification (DRC/LVS) validates physical and logical correctness, demonstrating the effectiveness of full-custom VLSI design methodology.