ECE 5003 – CMOS DIGITAL IC DESIGN

VIT-AP UNIVERSITY

Fall Semester 2025-26

M. Tech VLSI DESIGN

School of Electronics Engineering (SENSE)

Engineering Lab report

Submitted to

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Submitted By

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Registration Number - 25MVD7036

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Experiment No.1

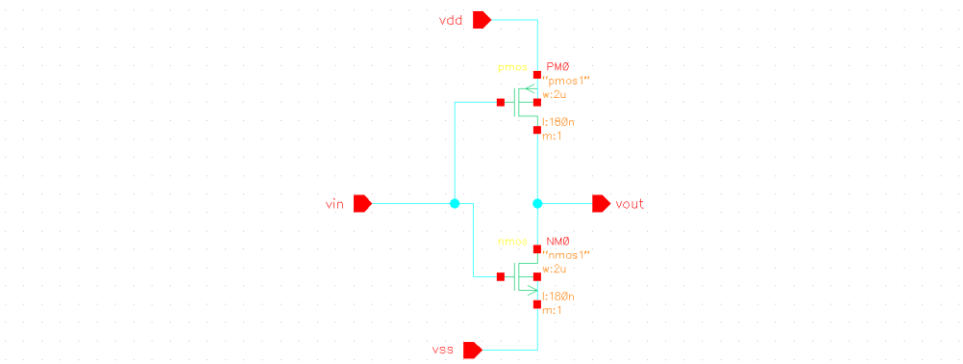
Design and Implementation of a CMOS Inverter

Aim: To design, simulate, layout, and verify a CMOS inverter using Cadence Virtuoso.

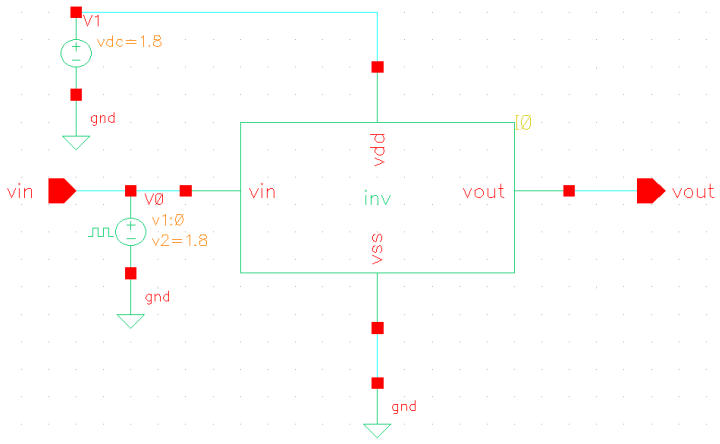
Tools Used: Cadence Virtuoso

- Cadence Virtuoso Schematic Editor – Schematic design
- Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations
- Cadence Spectre Simulator – Circuit simulation engine
- Cadence Virtuoso Layout Editor – Layout creation
- Cadence PVS / Assura – DRC and LVS verification
- Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

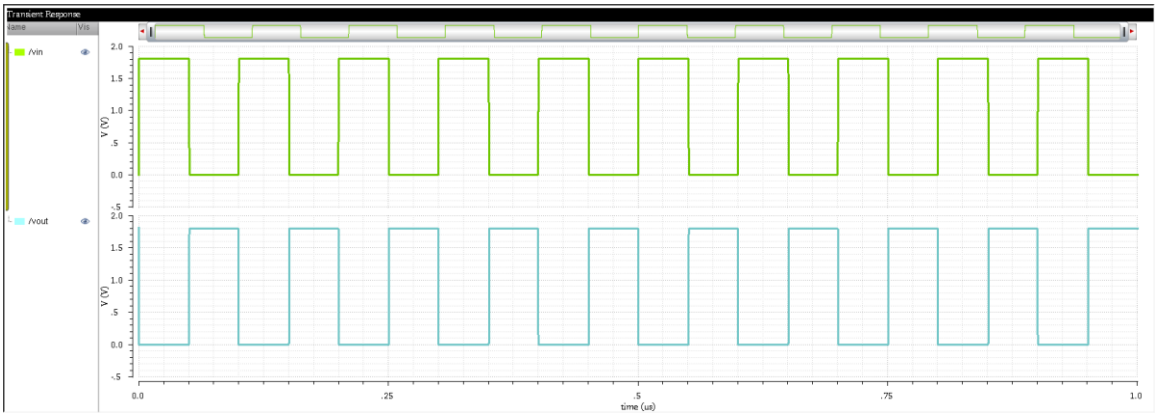
Schematic Diagram:

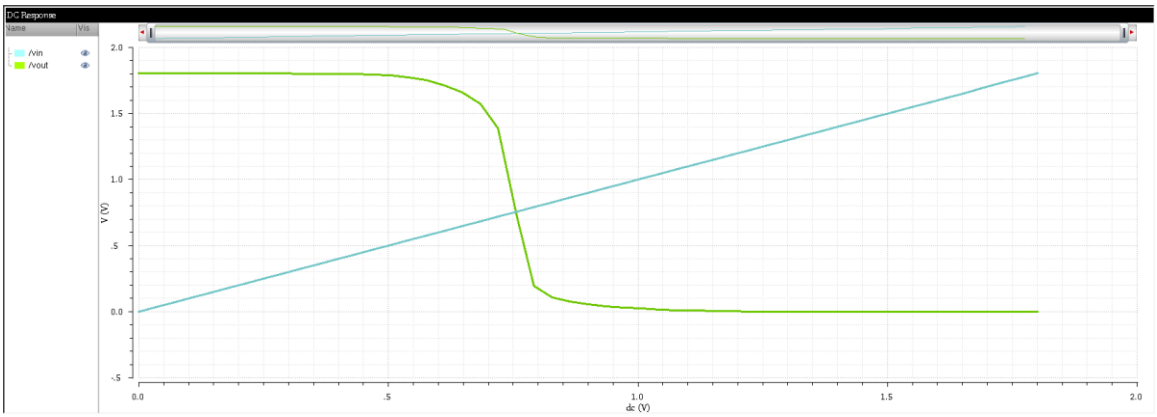


Test Schematic:

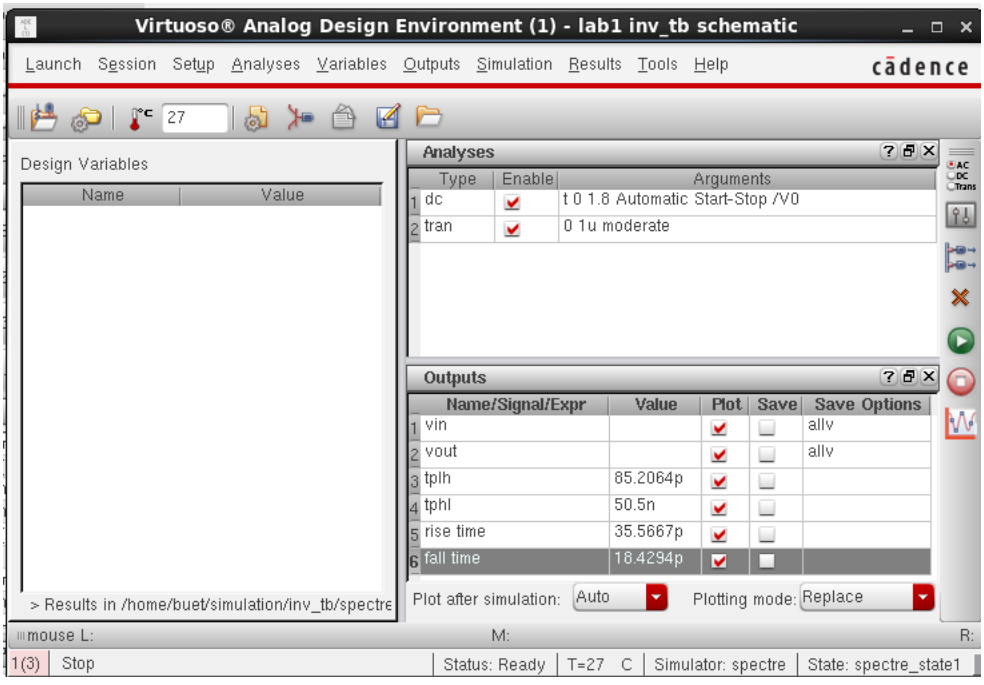


Simulation Waveforms (Pre-Layout):

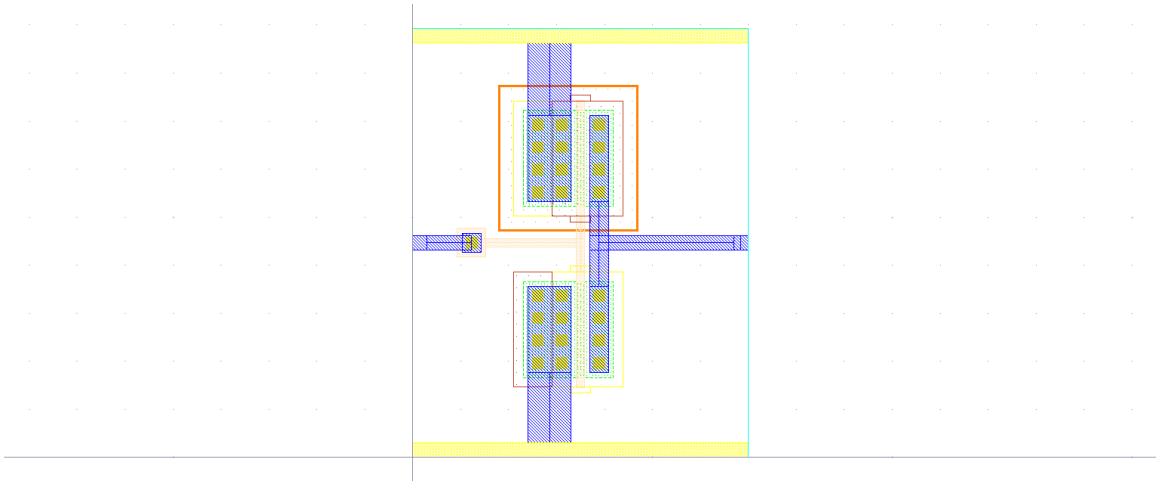




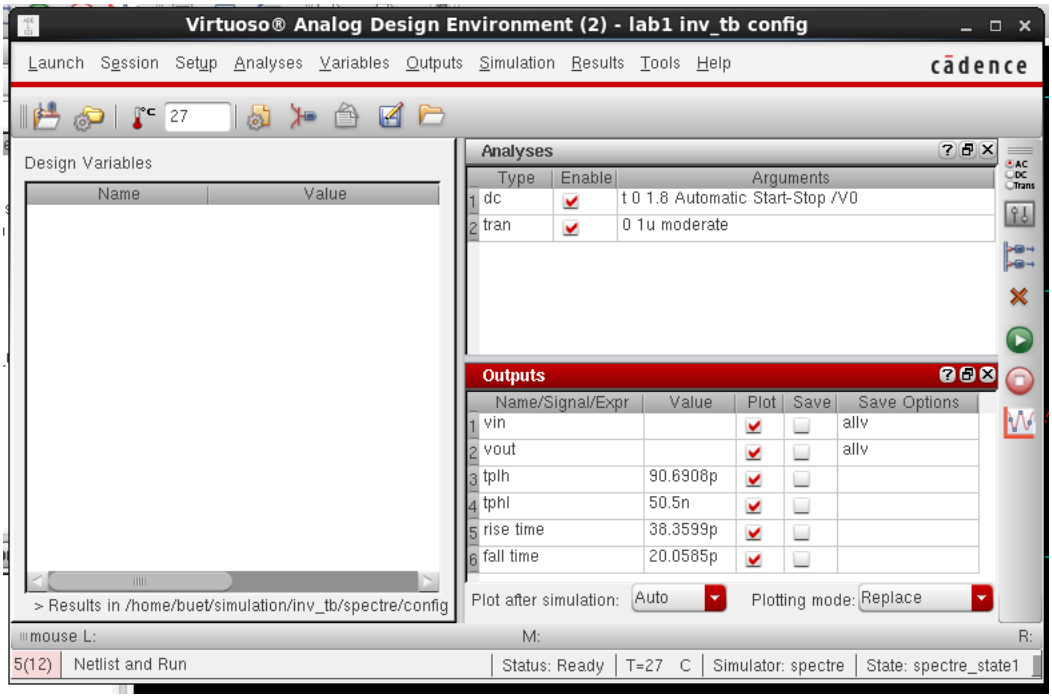
ADE L Window:

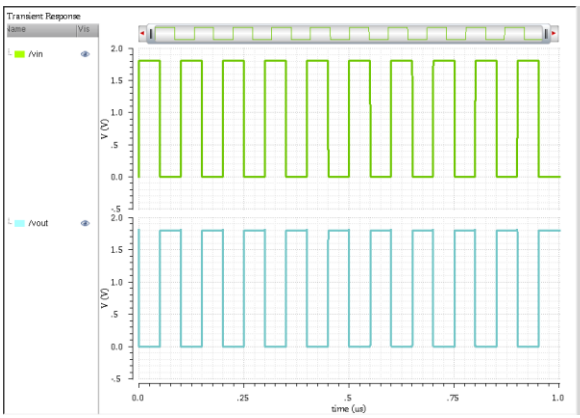


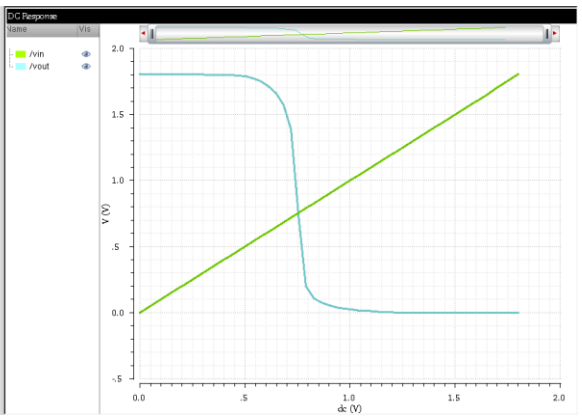
Layout:



Post-Layout Simulation Results:







Experiment No.2

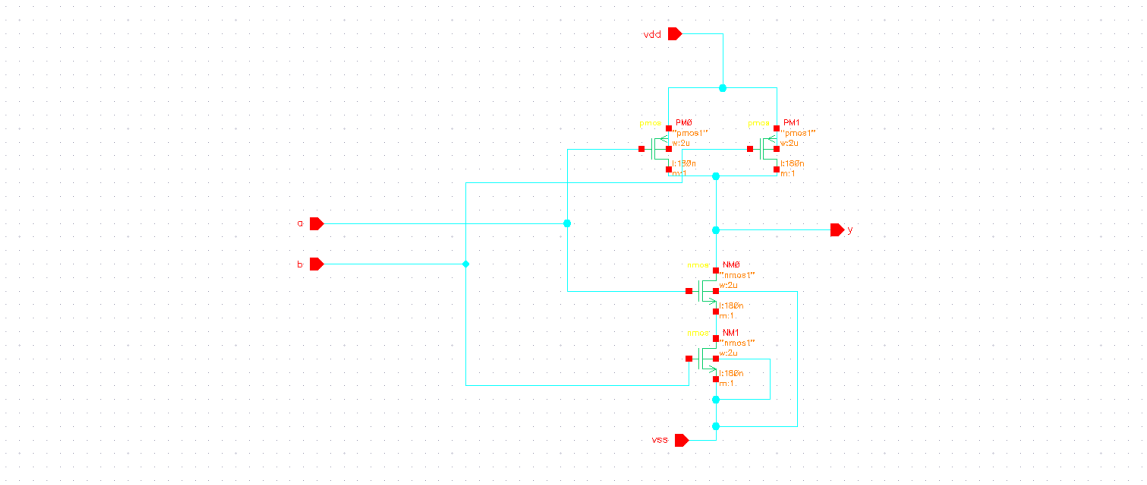
Design and Implementation of a CMOS NAND GATE

Aim: To design, simulate, layout, and verify a CMOS NAND Gate using Cadence Virtuoso.

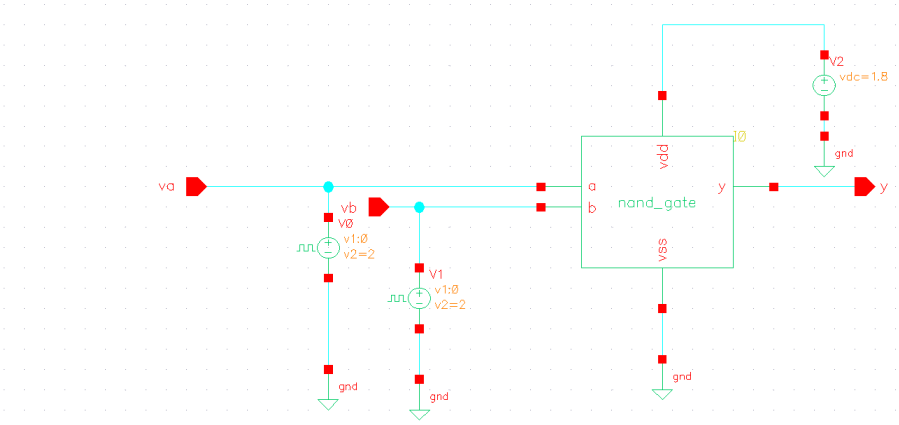
Tools Used: Cadence Virtuoso

- Cadence Virtuoso Schematic Editor – Schematic design
- Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations
- Cadence Spectre Simulator – Circuit simulation engine
- Cadence Virtuoso Layout Editor – Layout creation
- Cadence PVS / Assura – DRC and LVS verification
- Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

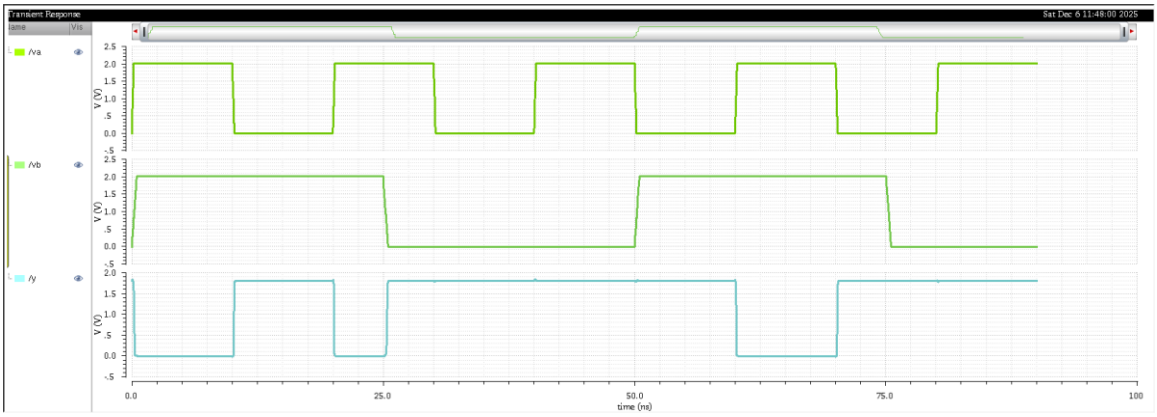
Schematic Diagram:



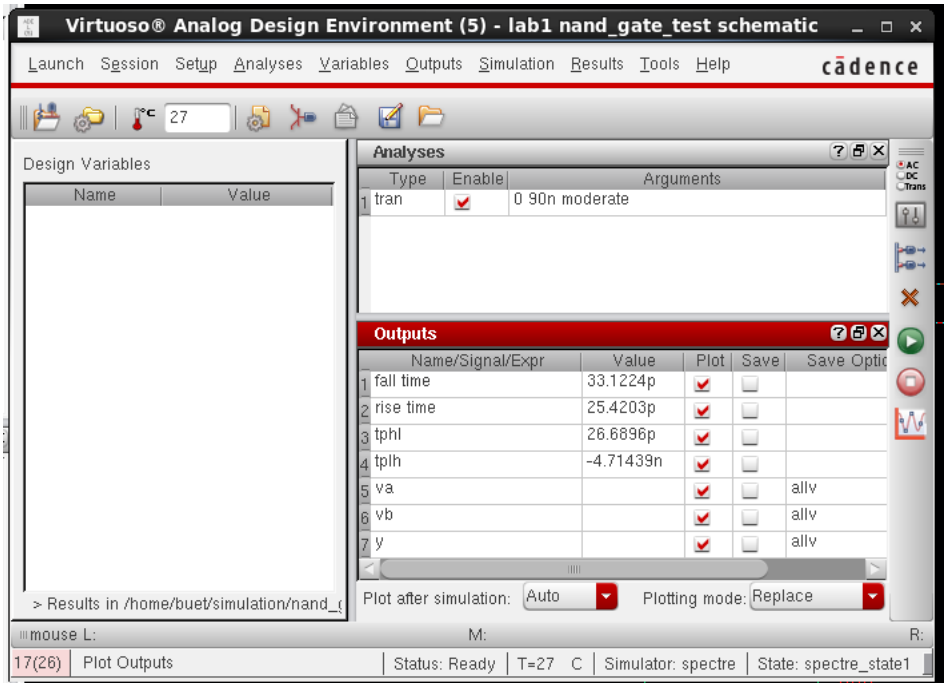
Test Schematic:



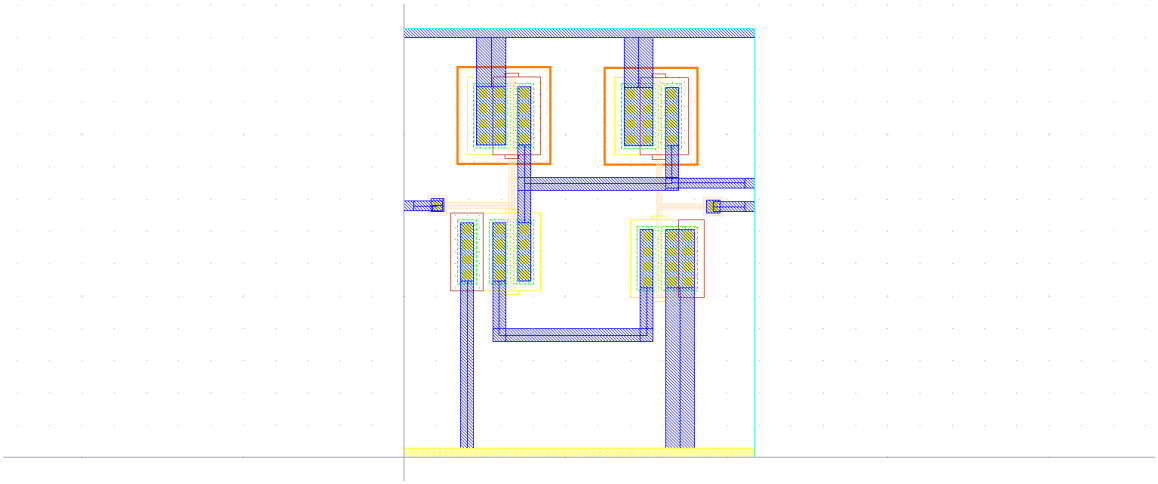
Simulation Waveforms (Pre-Layout):



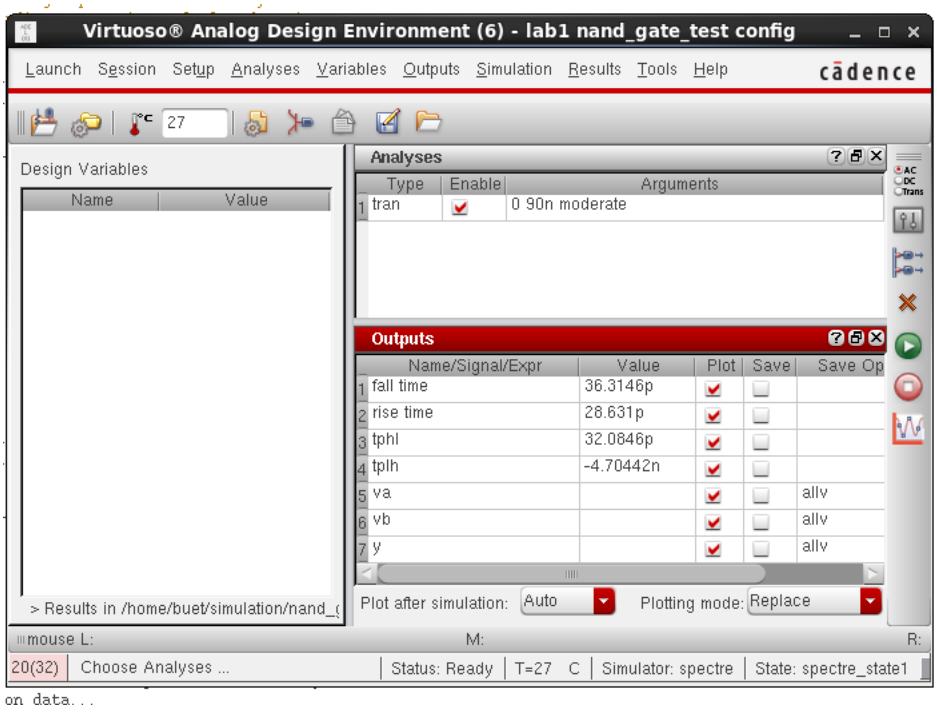
ADE L Window:

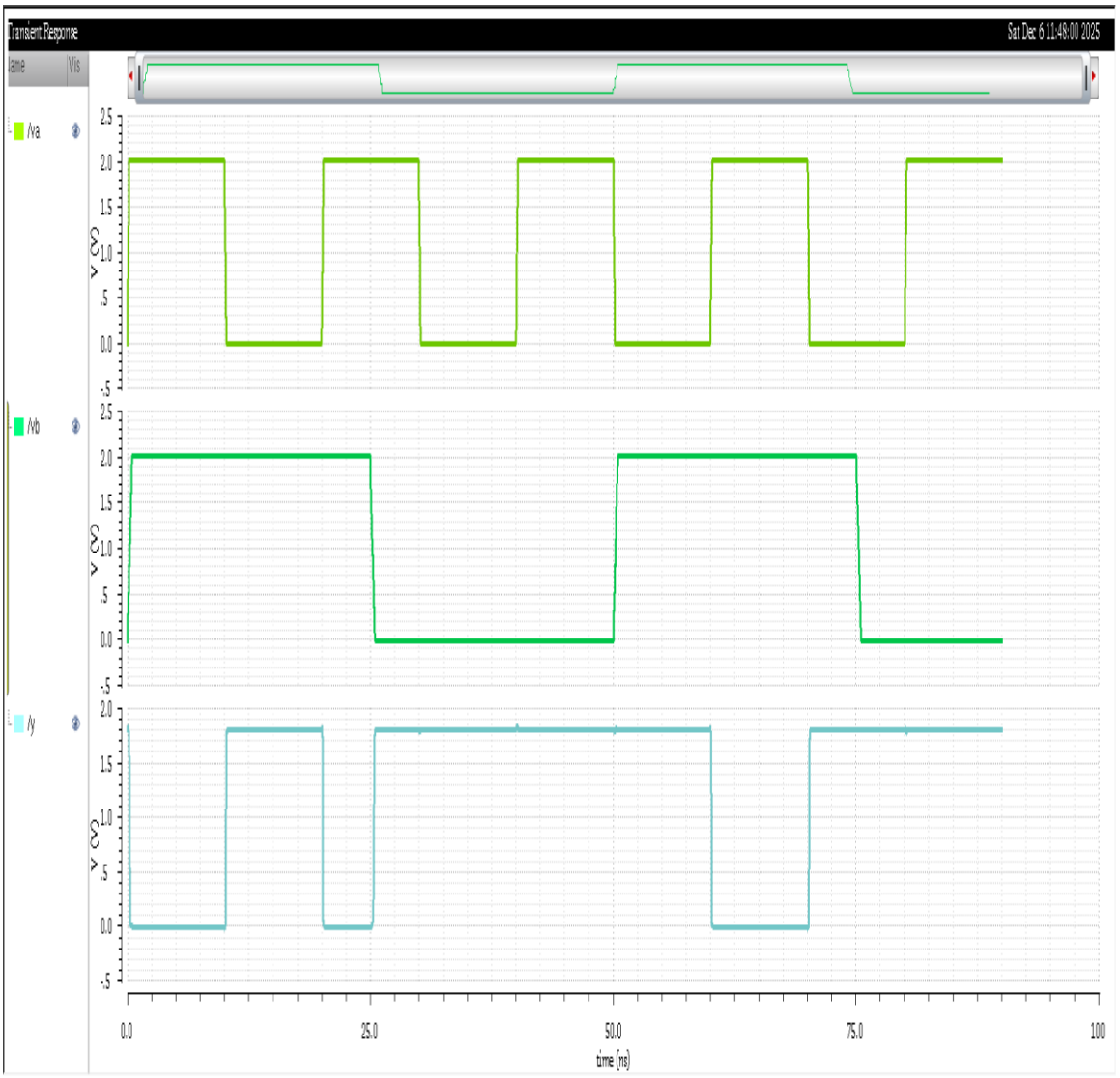


Layout:



Post-Layout Simulation Results:




Transient Response
Sat Dec 6 11:48:00 2025
Name
Vis
/va
/vb
/y
V (V)
2.5
2.0
1.5
1.0
.5
0.0
-.5
0.0
25.0
50.0
75.0
100
time (ns)

Experiment No.3

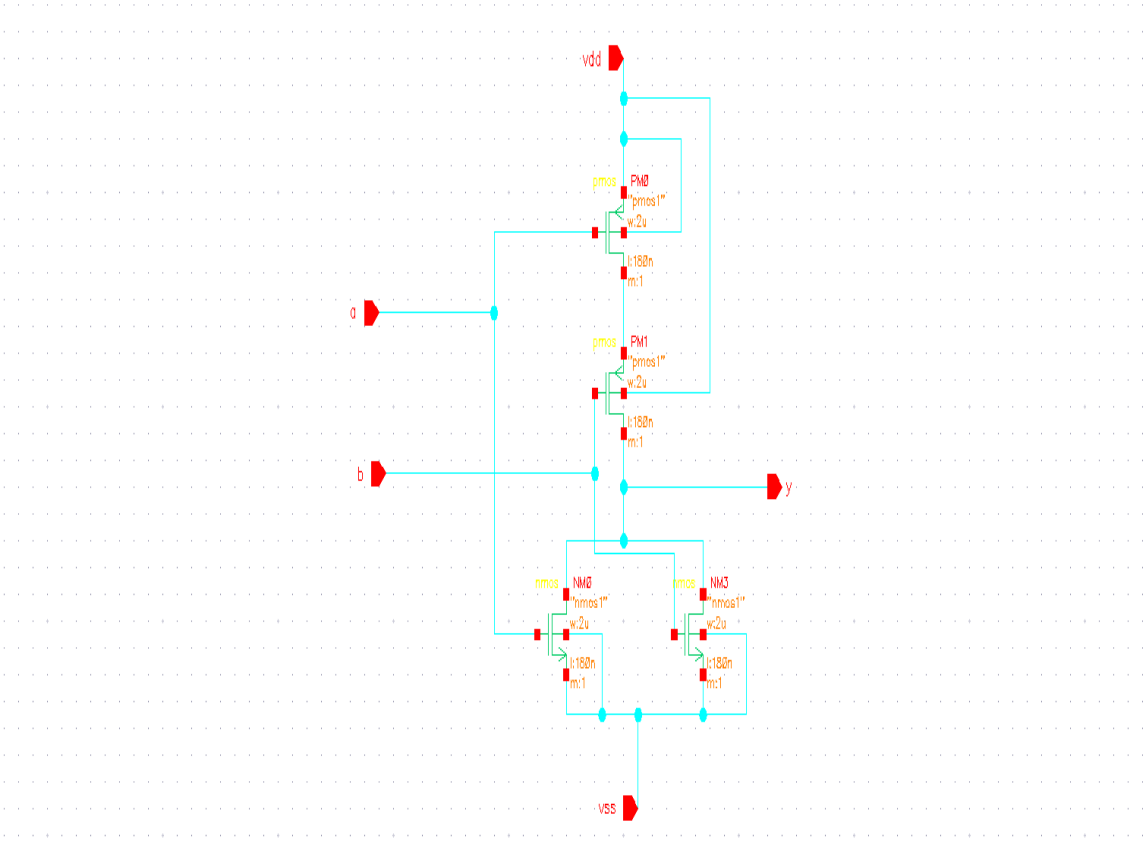
Design and Implementation of a CMOS NOR Gate

Aim: To design, simulate, layout, and verify a CMOS NOR Gate using Cadence Virtuoso.

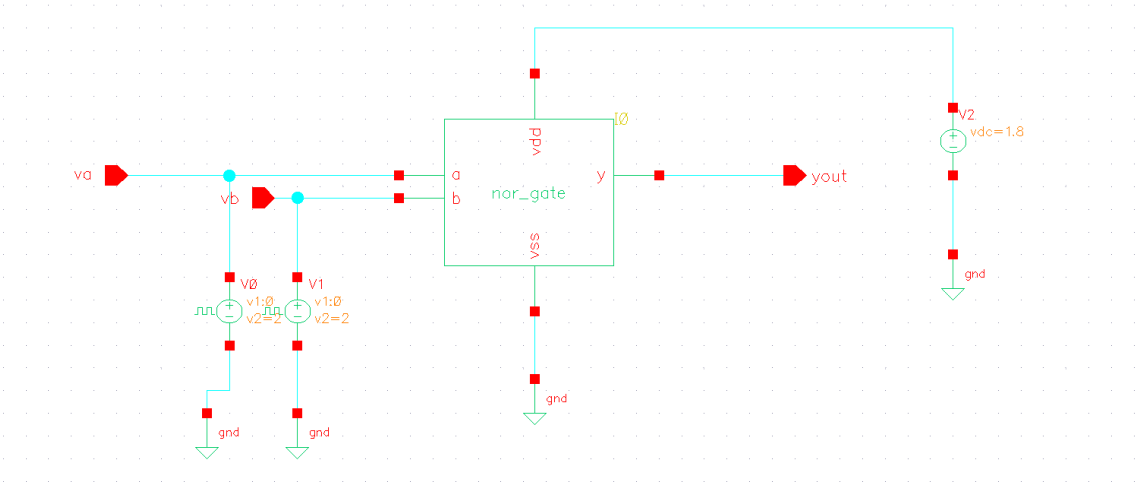
Tools Used: Cadence Virtuoso

- Cadence Virtuoso Schematic Editor – Schematic design
- Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations
- Cadence Spectre Simulator – Circuit simulation engine
- Cadence Virtuoso Layout Editor – Layout creation
- Cadence PVS / Assura – DRC and LVS verification
- Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

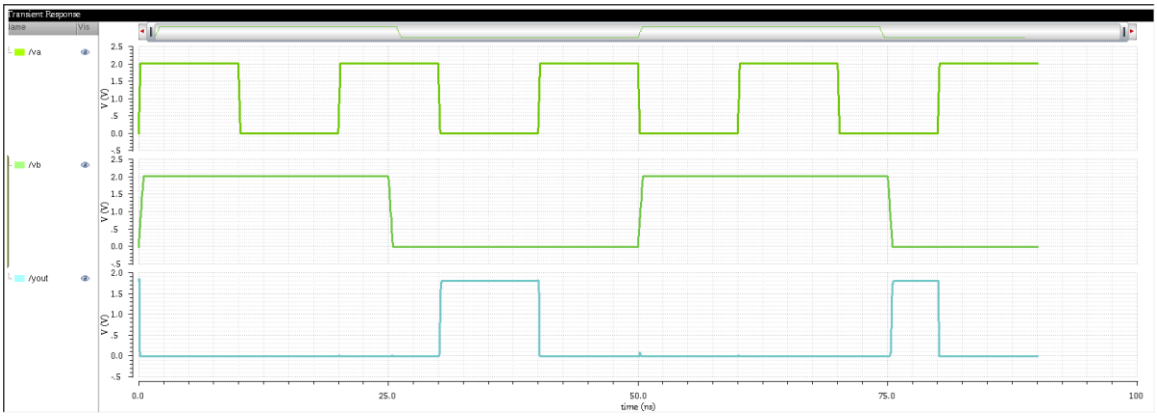
Schematic Diagram:



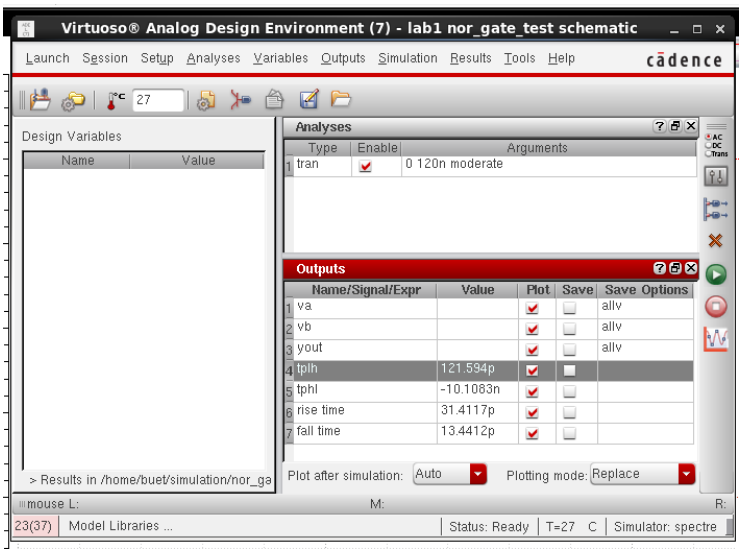
Test Schematic:



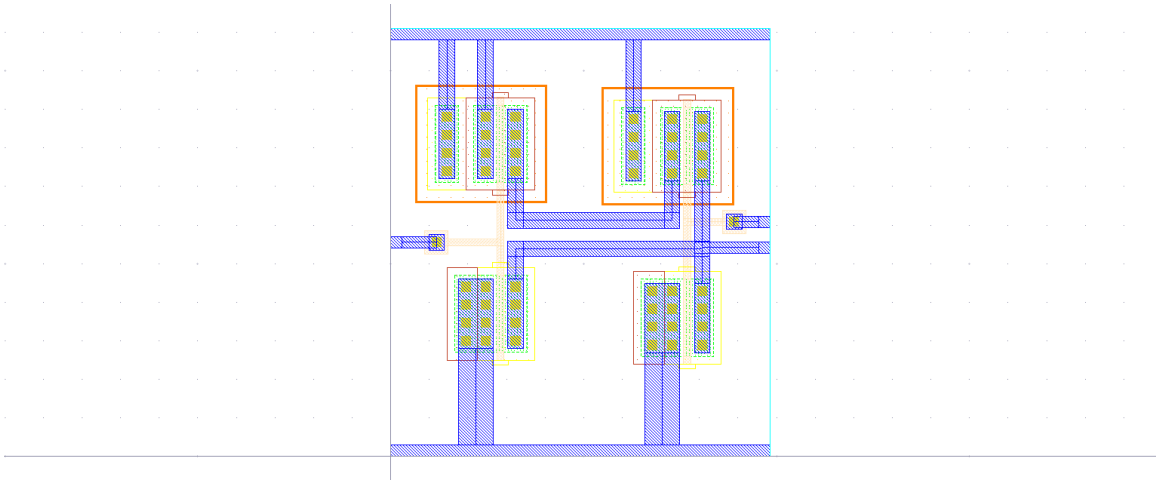
Simulation Waveforms (Pre-Layout):



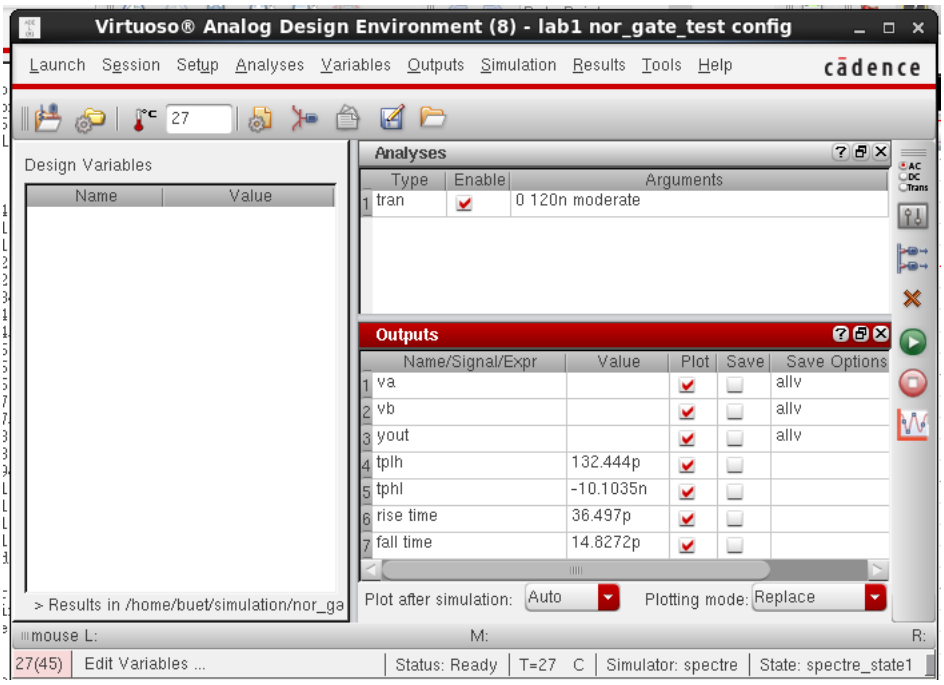
ADE L Window:

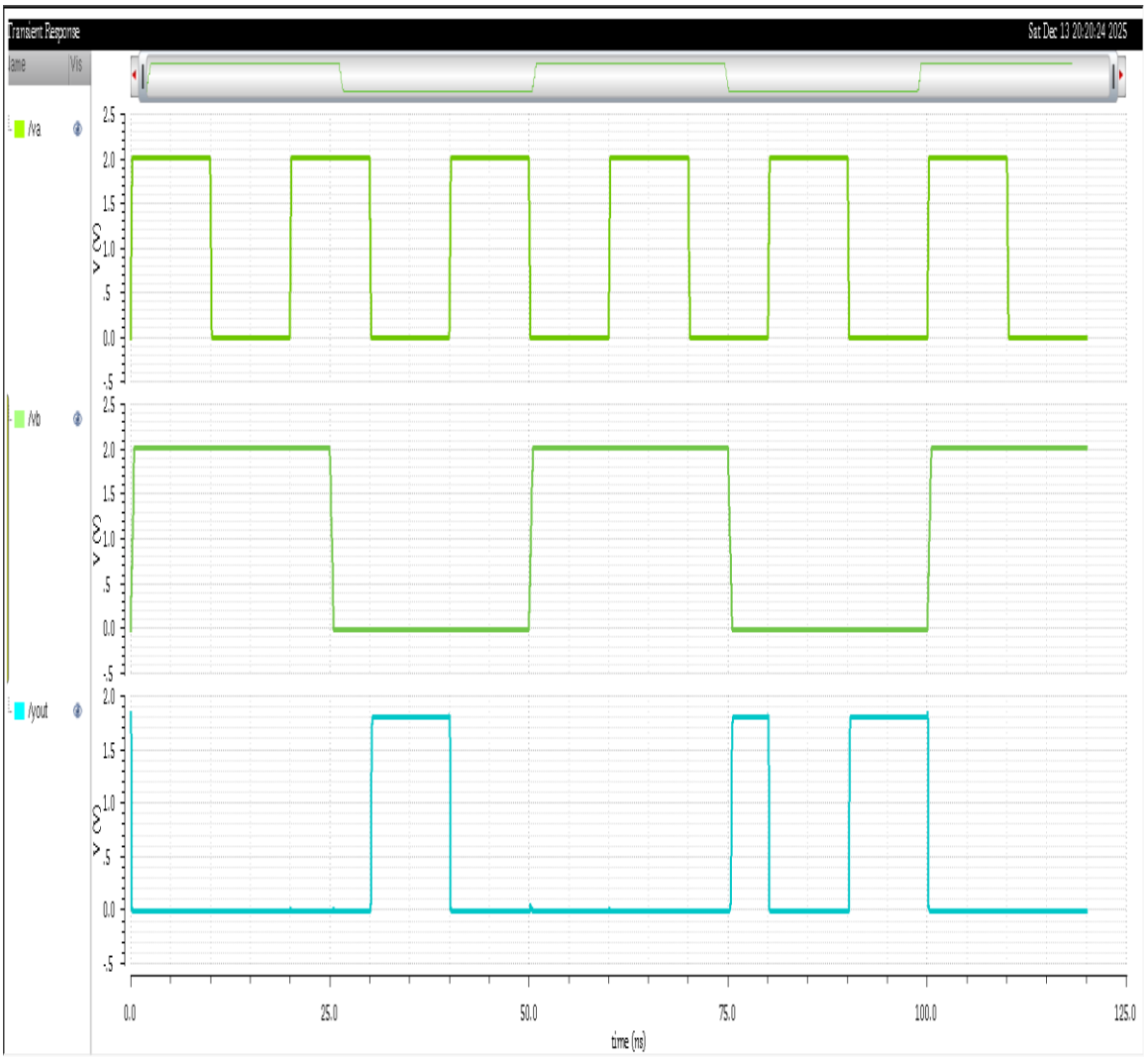


Layout:



Post-Layout Simulation Results:




Transient Response
Sat Dec 13 20:20:24 2025
/va
/vb
/vout
V (V)
time (ns)
0.0
25.0
50.0
75.0
100.0
125.0

Experiment No.4

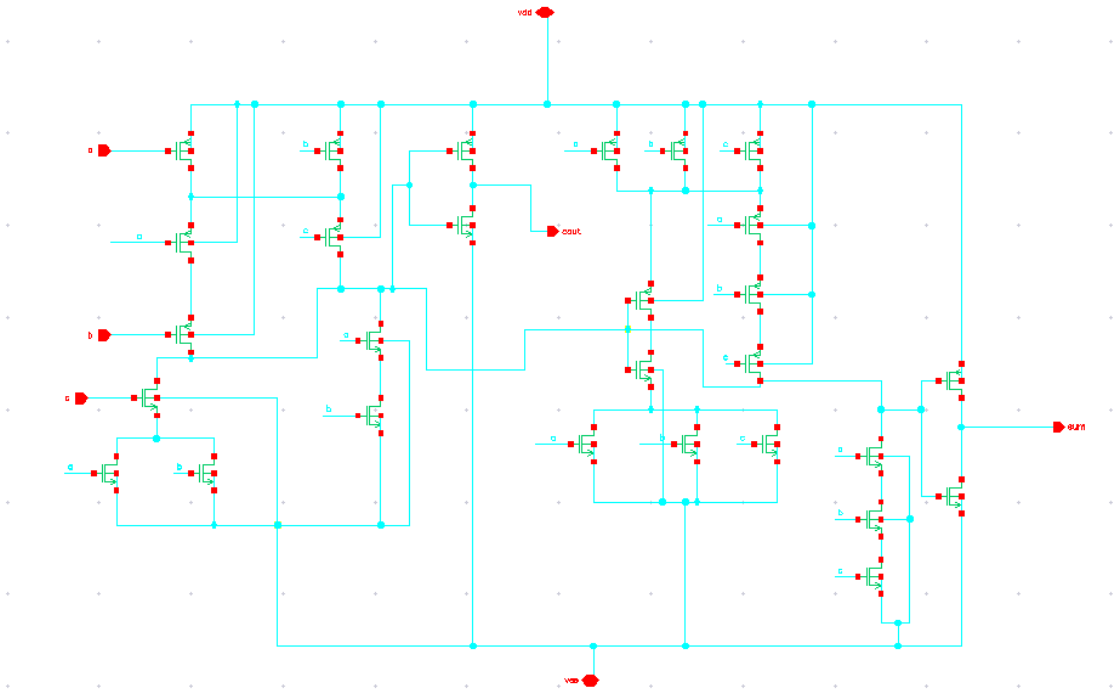
Design and Implementation of a FULL Adder

Aim: To design, simulate, layout, and verify a CMOS FULL Adder using Cadence Virtuoso.

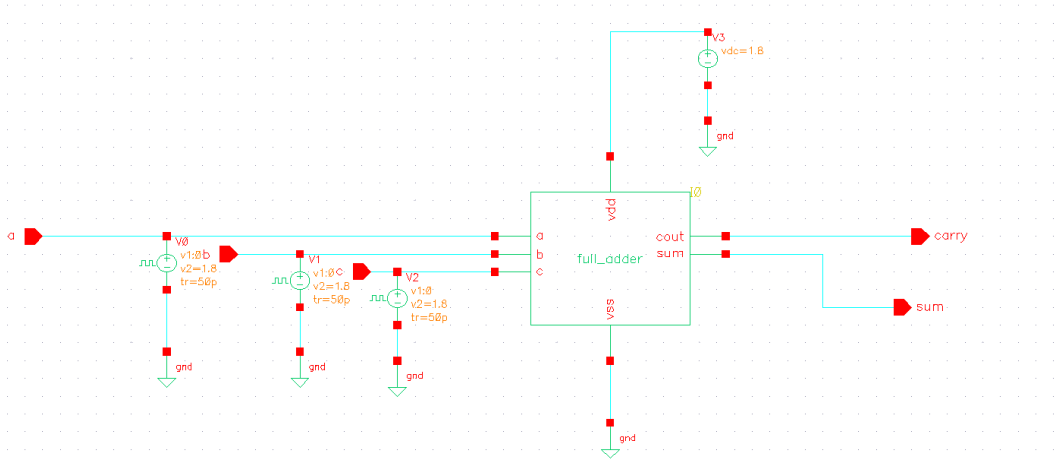
Tools Used: Cadence Virtuoso

- Cadence Virtuoso Schematic Editor – Schematic design
- Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations
- Cadence Spectre Simulator – Circuit simulation engine
- Cadence Virtuoso Layout Editor – Layout creation
- Cadence PVS / Assura – DRC and LVS verification
- Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

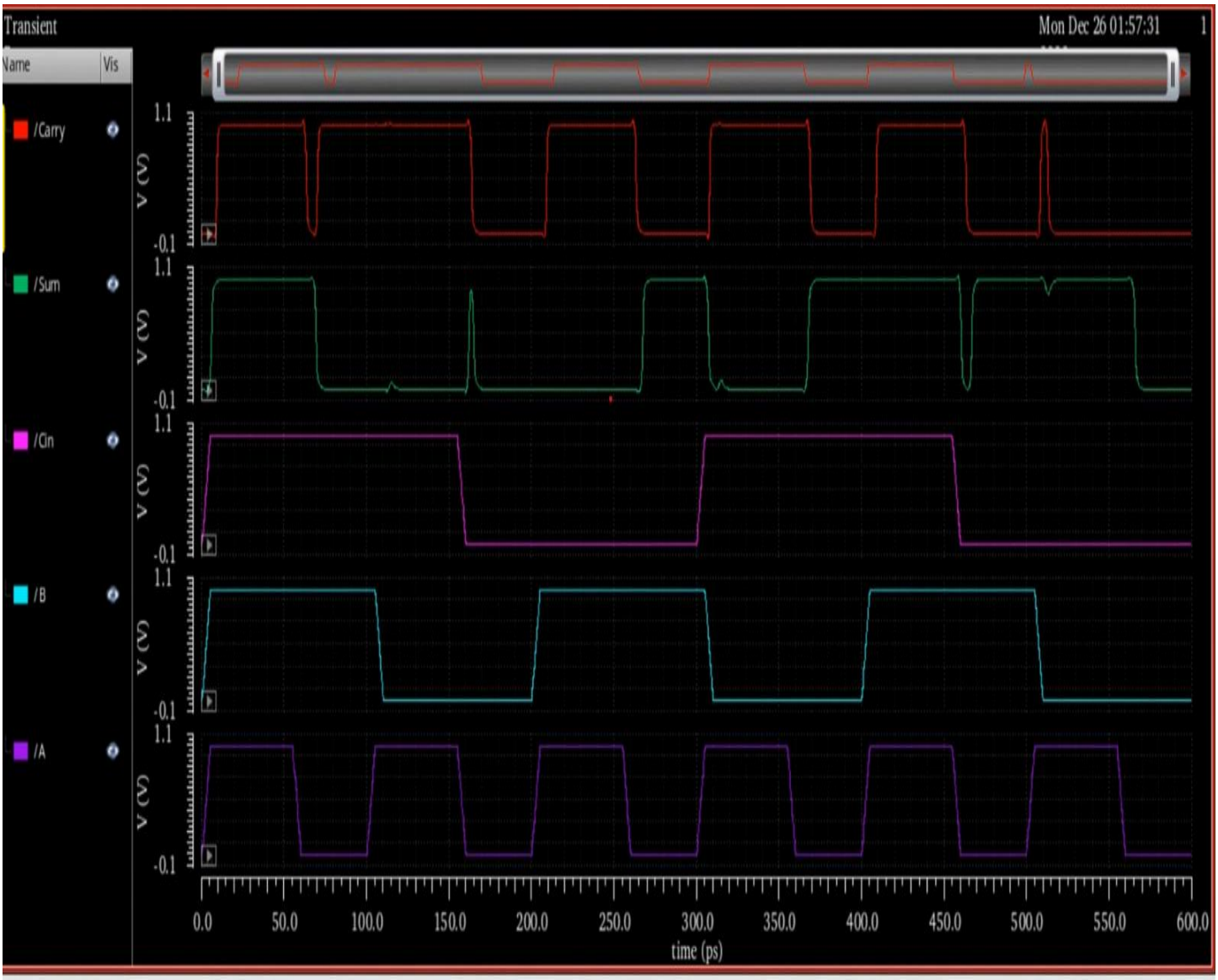
Schematic Diagram:



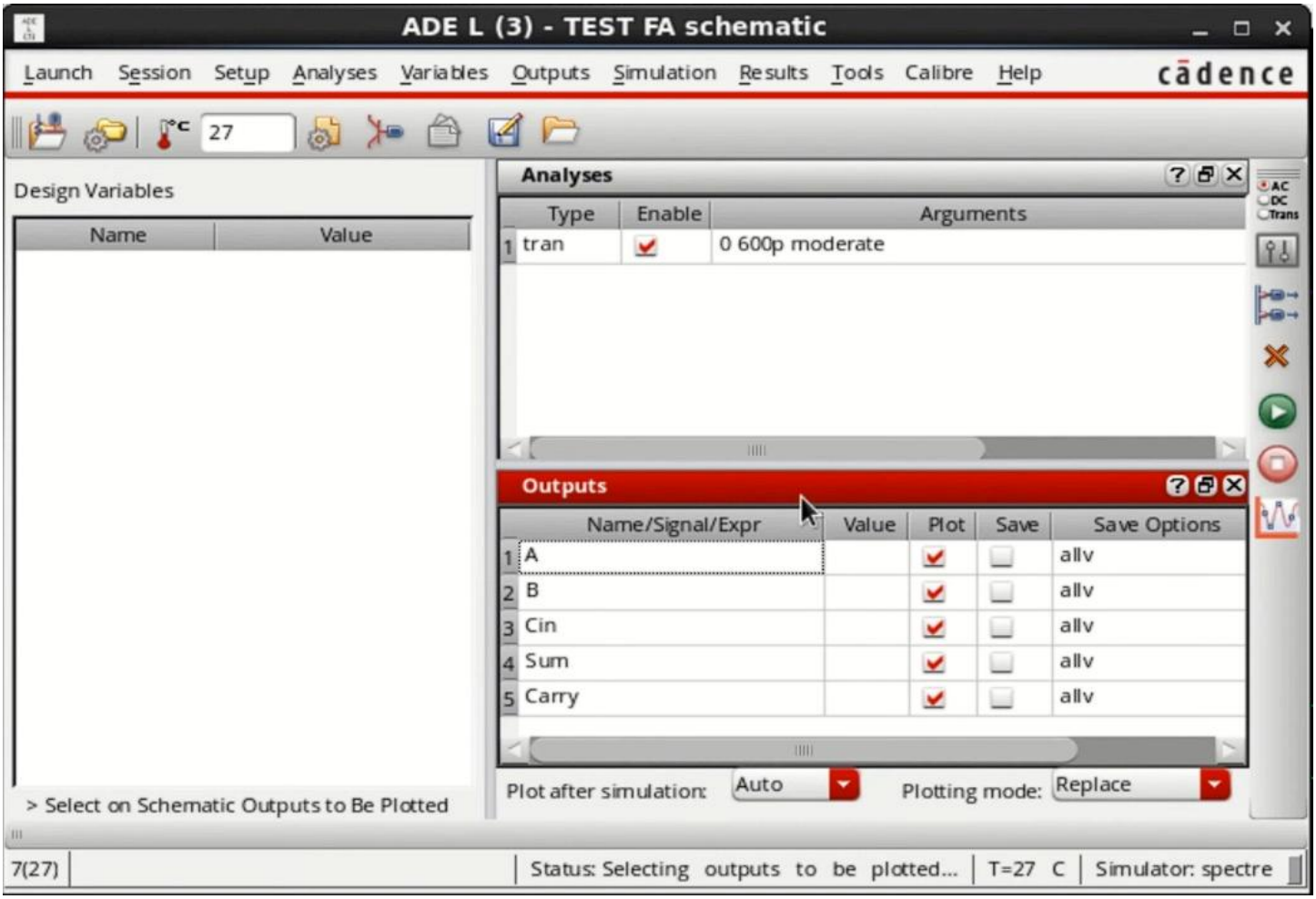
Test Schematic:



Simulation Waveforms (Pre-Layout):



ADE L Window:


ADE L (3) - TEST FA schematic
Launch Session Setup Analyses Variables Outputs Simulation Results Tools Calibre Help
cadence
27
Design Variables
Name Value
> Select on Schematic Outputs to Be Plotted
Analyses
Type Enable Arguments
1 tran 0 600p moderate
AC DC Trans
Outputs
Name/Signal/Expr Value Plot Save Save Options
1 A allv
2 B allv
3 Cin allv
4 Sum allv
5 Carry allv
Plot after simulation: Auto
Plotting mode: Replace
7(27)
Status: Selecting outputs to be plotted...
T=27 C
Simulator: spectre

Experiment No.5

Design and Implementation of a D-Flip Flop

Aim: To design, simulate, layout, and verify a CMOS XOR Gate using Cadence Virtuoso.

Tools Used: Cadence Virtuoso

• Cadence Virtuoso Schematic Editor – Schematic design

• Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations

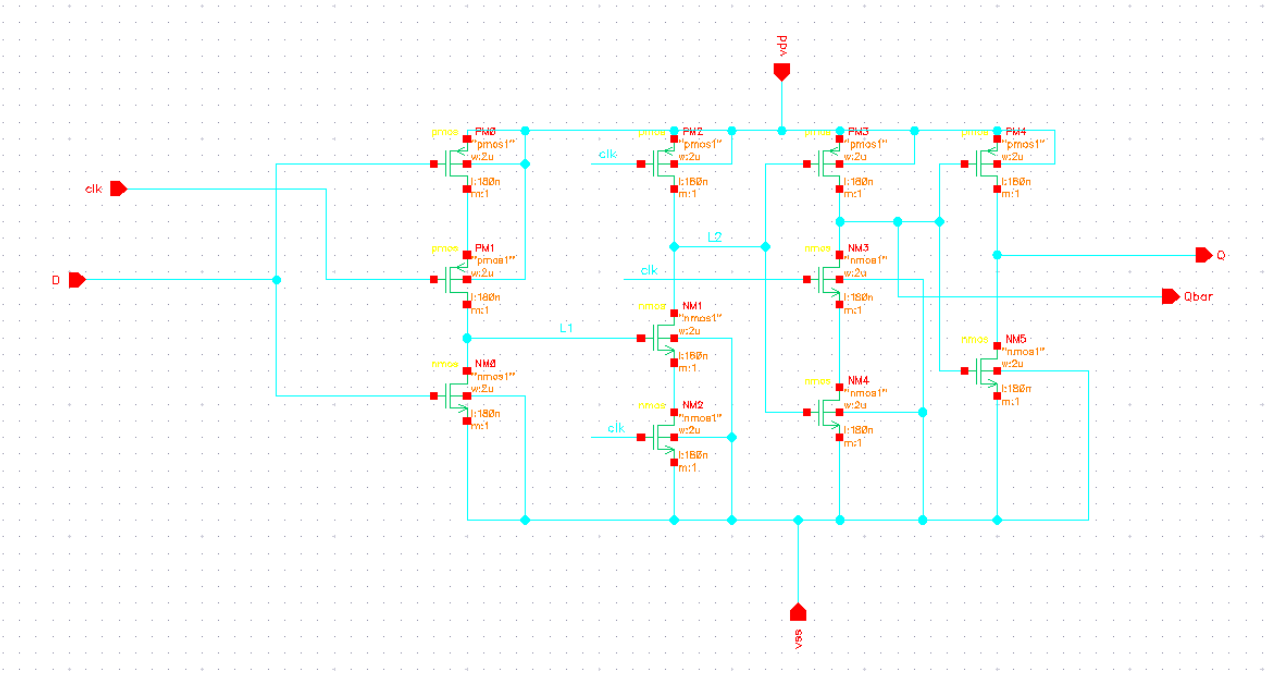
• Cadence Spectre Simulator – Circuit simulation engine

• Cadence Virtuoso Layout Editor – Layout creation

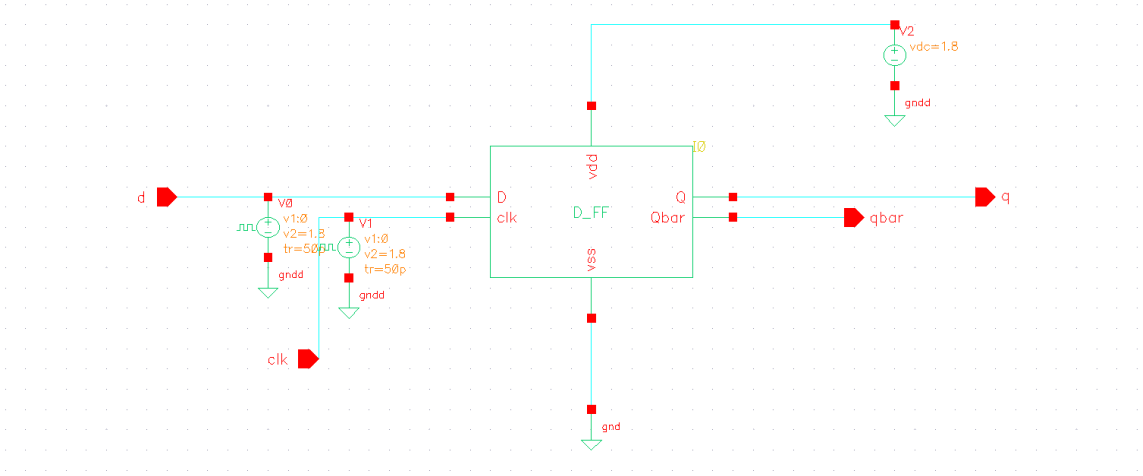
• Cadence PVS / Assura – DRC and LVS verification

• Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

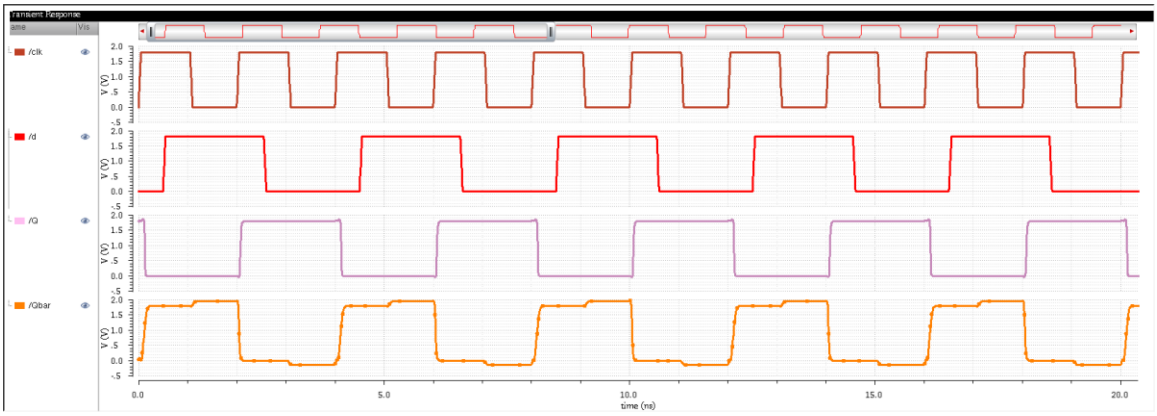
Schematic Diagram:



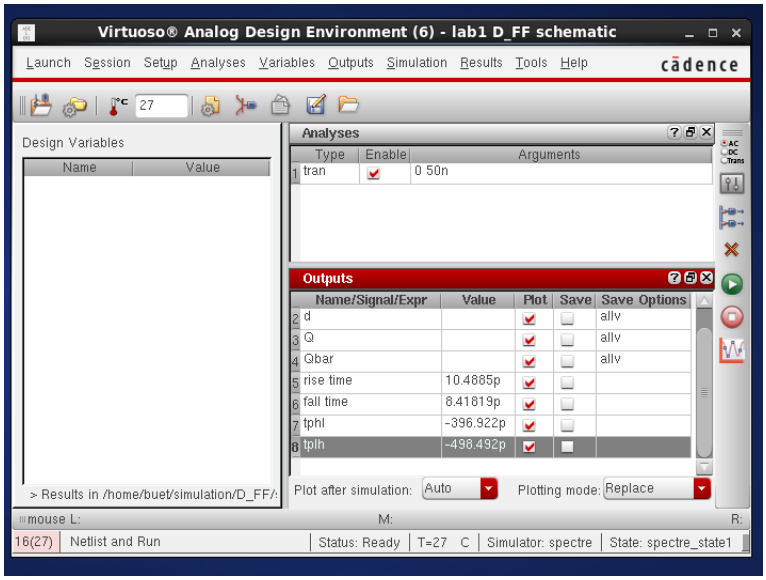
Test Schematic:



Simulation Waveforms (Pre-Layout):



ADE L Window:



Experiment No.6

Design and Implementation of a 6T-SRAM

Aim: To design, simulate, layout, and verify a CMOS XOR Gate using Cadence Virtuoso.

Tools Used: Cadence Virtuoso

• Cadence Virtuoso Schematic Editor – Schematic design

• Cadence ADE L (Analog Design Environment L) – Setting up, running, and analyzing simulations

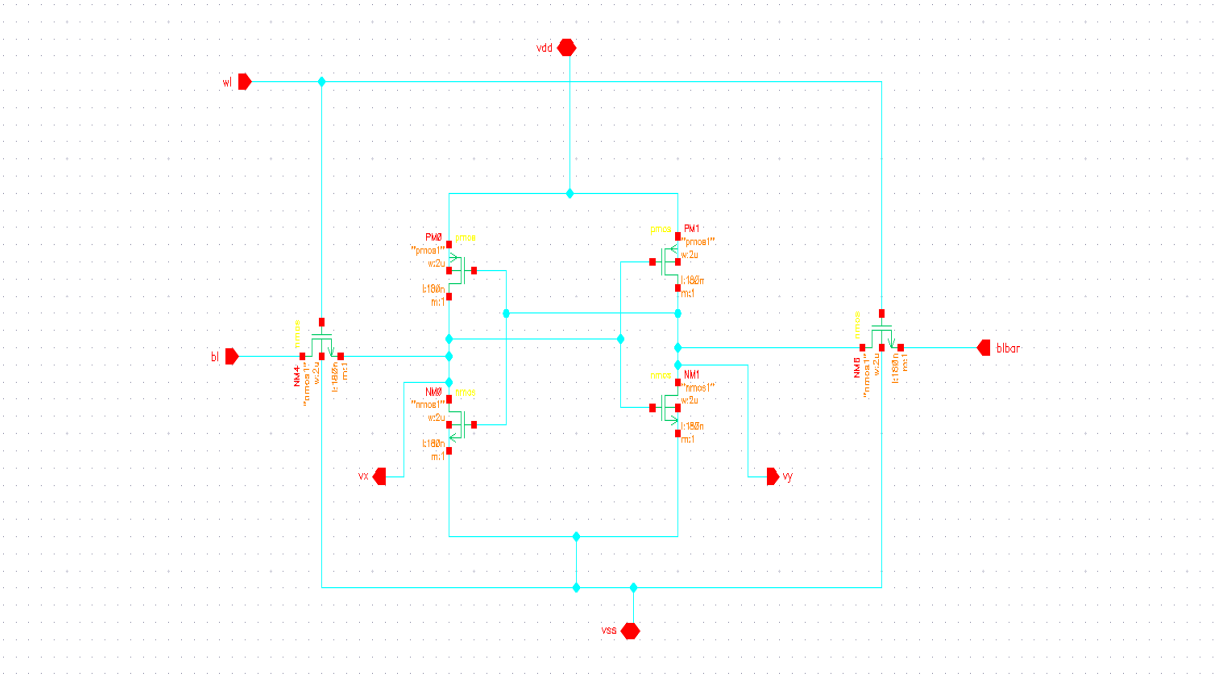
• Cadence Spectre Simulator – Circuit simulation engine

• Cadence Virtuoso Layout Editor – Layout creation

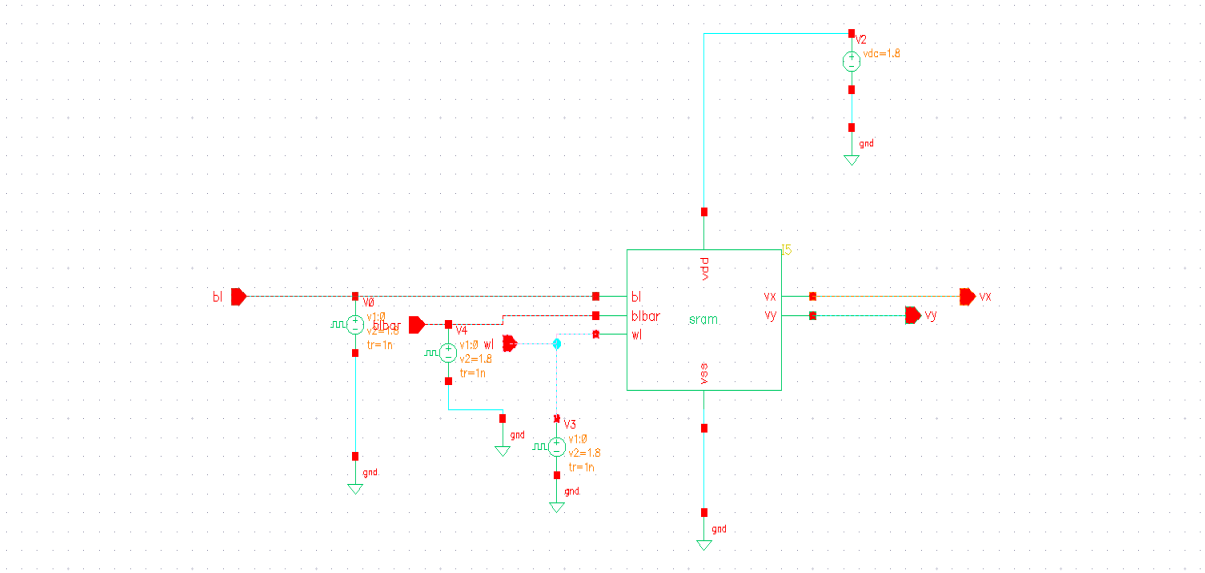
• Cadence PVS / Assura – DRC and LVS verification

• Cadence Quantus QRC (RC Extraction Tool) – Post-layout parasitic extraction

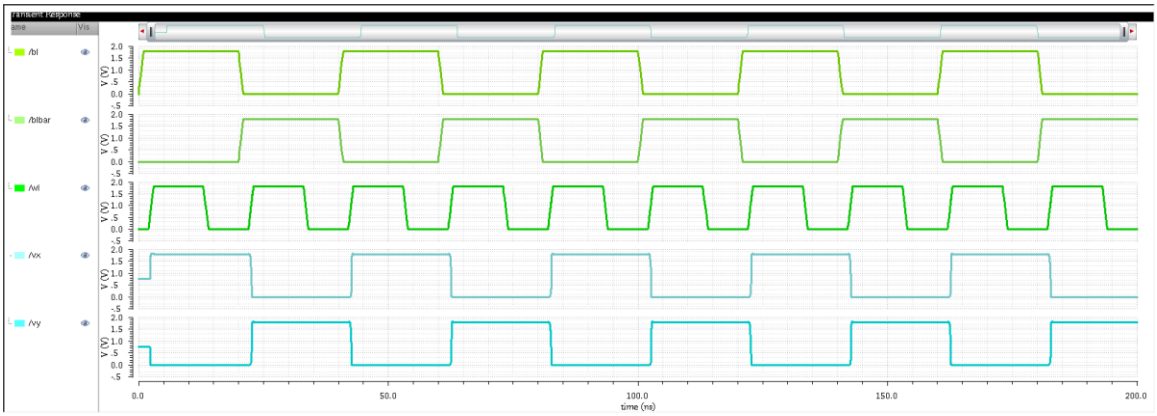
Schematic Diagram:



Test Schematic:



Simulation Waveforms (Pre-Layout):



ADE L Window: