Synthesis Oddities for Equalizer

- We have a bunch of memories that we don't want Synopsys to analyze.
  - dualPort*
  - ROM_*
  - cmdROM

- Look at the verilog for these provided blocks. They have a couple of directives that look like comments. These "translate_off/translate_on" directives tell synopsys to ignore the stuff between them.

- Still we want to do a "***set_dont_touch***" on each of these memories.

- So do a ***set_dont_touch*** on ***[find design dualPort*]*** for instance.

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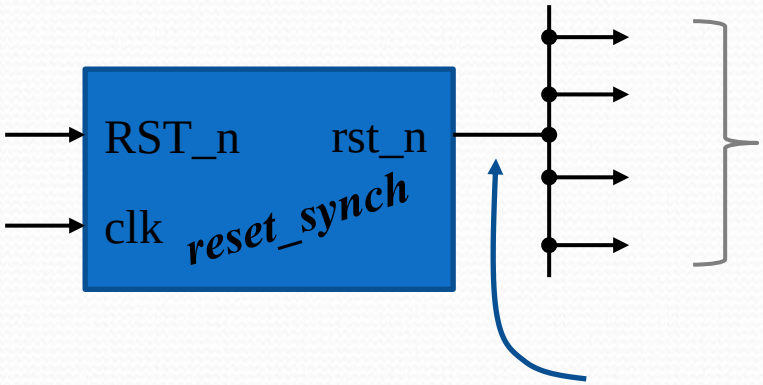

Goes to a whole bunch of flops….don't want Synopsys to buffer it.

rst_n is an internal net to our design, but we want to do a ***set_dont_touch_network*** on it like we do with **clk**. We can find it with ***get_net iRST/rst_n***

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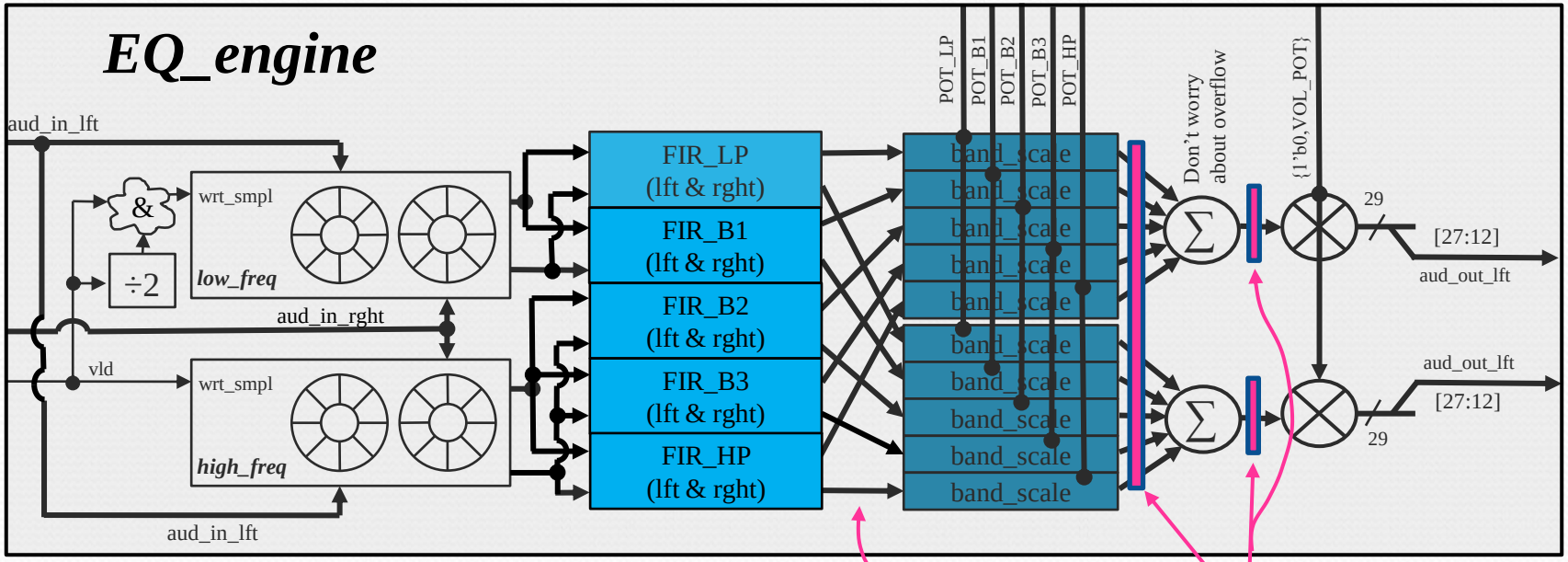

Did you pipeline EQ_engine?

There is a heck of a lot of math going on here kids. Is Synopsys going to be able to fit all this math in a single cycle at a 3ns clock period? You need to insert some flops in this path to pipeline it and ease the timing constraints. Start without flops first and get it functionally working. Add the pipelining flops later, the latency of the flops affects nothing *(they can be free running flops).*