

# Lab 02 - First Verilog

In this lab, you've learned how to do an initial and simple design in Verilog to learn the Vivado tooling and process involved in RTL/FPGA design.

## Rubric

Item	Description	Value
Summary Answers	Your writings about what you learned in this lab.	25%
Question 1	Your answers to the question	25%
Question 2	Your answers to the question	25%
Question 3	Your answers to the question	25%

## Lab Summary

We learned the syntax of verilog and how to implement that to activate certain switches and LED's on the Basys3 board. How to generate the bit stream and program the device with the code we scripted in Vivado and having that code simulated on the board.

## Lab Questions

### 1 - Describe the stages of building a Verilog project in Vivado.

First we created the project in Vivado, then we named the project accordingly and made sure all the necessary settings and files were added. Once done we made sure top.v was in synthesis and simulation and then test.v was in simulation. Then we made sure the project was configured to a Basys3 board. After familiarizing ourselves with the Vivado interface we opened the top.v file and added our code. After adding our code we ran a behavioral simulation, then generated bitstreams to then be uploaded to the Basys3 board. After the bitstream process was done, we connected the Basys3 board and programmed it with our code we wrote in top.v. Resulting in LED's turning on at the resulting switches we had set in our code.

## 2 - What is the value in looking at the elaborated design schematic?

It helps us visualize the connection between switches and LED's we implemented in our code and made sure it was the correct connection we were intending.

## 3 - Why should we simulate our designs frequently? What does the simulation do?

We should simulate our code frequently to make sure that it is functioning as intended and to make sure there are no bugs that would stop our code from working. The simulation shows the switches and LED's we specified are working or not working in a simulated environment.

## Code Submission

Upload a .zip of all your code or a public repository on GitHub.