

Q1

a)

s2	s1	s0	A
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

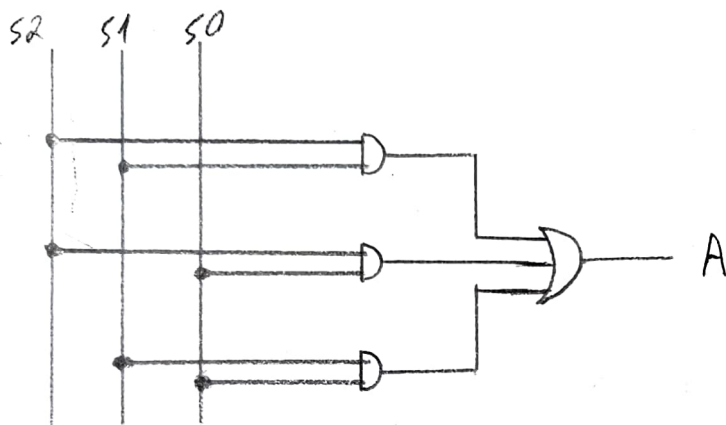
A

s2s1	00	01	11	10
s0	0	0	1	0
1	0	1	1	1

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$$A = s2.s1 + s2.s0 + s1.s0$$

b)



c) Código Verilog

Q2

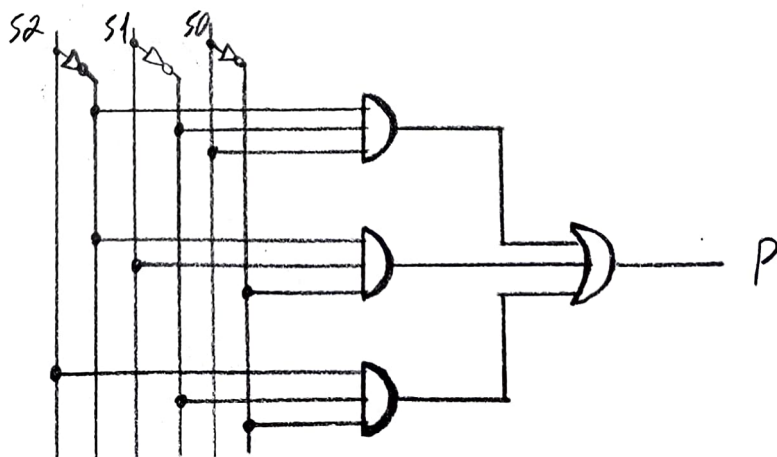
a)

s2	s1	s0	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

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$$P = \overline{s2}.\overline{s1}.s0 + \overline{s2}.s1.\overline{s0} + s2.\overline{s1}.\overline{s0}$$

b)



c) Código Verilog

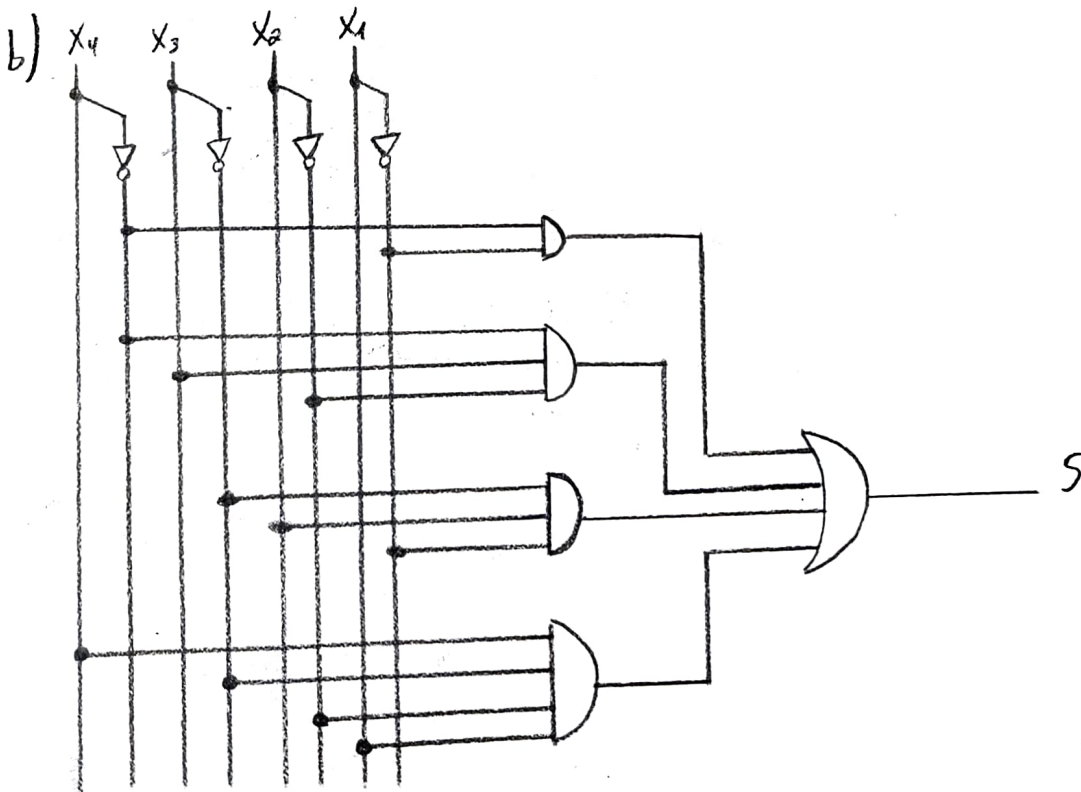
Q3

a) Mapa de Karnaugh:

\underline{S}	$X_4 X_3$		$X_2 X_1$	
	00	01	11	10
00	1	1	0	0
01	0	1	0	1
11	0	0	0	0
10	1	1	0	1

\Rightarrow

$$S = \overline{X_4} \cdot \overline{X_1} + \overline{X_4} \cdot X_3 \cdot \overline{X_2} + \overline{X_3} \cdot X_2 \cdot \overline{X_1} + X_4 \cdot \overline{X_3} \cdot \overline{X_2} \cdot X_1$$



c) Código Verilog

d) Código Test Verilog + GTK WAVE

Q4

a) De acordo com a Tabela Verdade do Full Adder:

$$\Rightarrow \boxed{C_{out,i} = a_i \cdot b_i + c_{in,i-1} \cdot (a_i \oplus b_i)}$$

$$\Rightarrow \boxed{Sum_i = a_i \oplus b_i \oplus c_{in,i}}$$

b) Código Verilog

c) Código Test Verilog