Instituto Tecnológico de Aeronáutica

Divisão de Ciência da Computação - IEC

Departamento de Sistemas de Computação - IEC-SC

EEA-25 - Sistemas Digitais Programáveis

Lista de Exercícios Nº 8

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1 Modeling Finite-State Machines in Verilog (10,0)

1.1 Vending Machine Controller

Consider the system diagram shown in Figure 1:

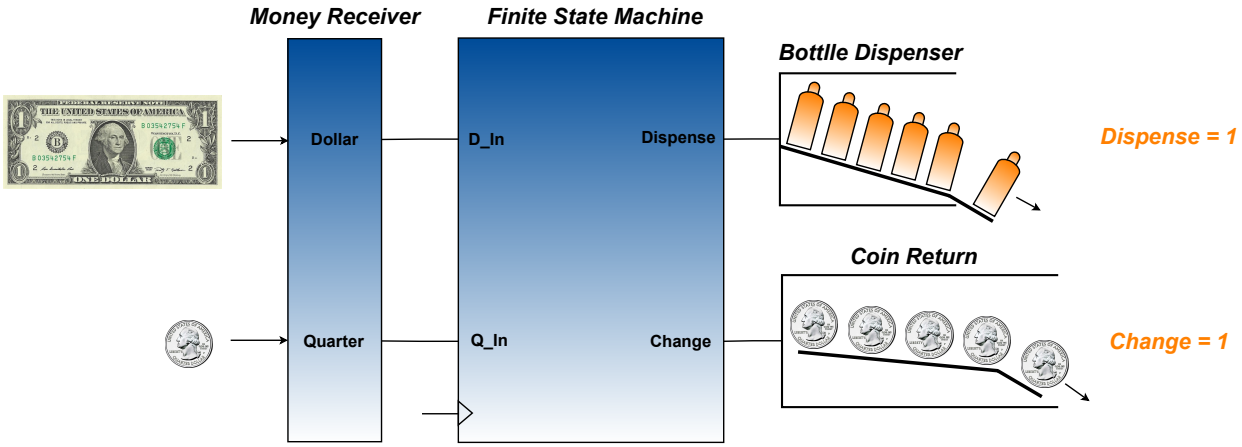

Figura 1: Vending Machine Controller.

You are going to design a simple vending machine controller. The vending machine will sell bottles of water for 75 cents. Customers can enter either a dollar bill or quarters. Once a sufficient amount of money is entered, the vending machine will dispense a bottle of water. If the user entered a dollar, it will return one quarter in change. A ***Money Receiver*** detects when money has been entered.

The receiver sends two logic signals to our circuit indicating whether the a dollar bill or quarter was received. A ***Bottle Dispenser*** system holds the water bottles and will release one bottle when its input signal is asserted. A ***Coin Return*** system holds quarters for change and will release one quarter when its input signal is asserted The money receiver will reject money if a dollar and quarter are entered simultaneously or if a dollar is entered once the user has started entering quarters.

Follow the examples on pages 252, 253 and 254 from Brock J. LaMeres book (Introduction to Logic Circuits & Logic Design with Verilog) to design the vending machine controller. Design the Verilog Model of the vending machine controller. You can use the code on Example 9.15, page 337, as a reference.

You must show your code and the simulation waveforms in GTKWave.