ELEC6232: Analog and Mixed-Signal IC Design

Operational Amplifier Design Assignment

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1 Introduction

This report details the design of a single-stage operational amplifier to be used as a unity-gain buffer which meets the specifications as stipulated in the ELEC6232 Design Assignment. The load capacitance and ADC sampling frequency specifications are:

C_{in}	f_{sample}
3.2pF	16MHz

Table 1: Student specific specification for C_{in} and f_{sample}

2 Amplifier specification derivation

2.1 Unity-gain Bandwidth, f_0

In order to derive the top-level specification for the desired application, we first model amplifer as a first-order system, configured in a unity-gain closed loop control system which illustrated in Figure 1.

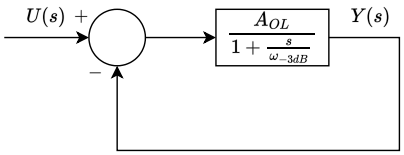


Figure 1: First-order model of system in assignment during ADC acquisition.

To derive the unity-gain bandwidth, ω_0, we derive the transfer function of this system and consider the system in response to a step function $u(t)$. First, let $A(s) = \frac{A_{OL}}{1+\frac{s}{\omega_{-3dB}}}$:

$$\begin{aligned} H(s) &= \frac{A(s)}{1+A(s)} \\ &= \frac{\frac{A_{OL}}{1+\frac{s}{\omega_{-3dB}}}}{1+\frac{s}{\omega_{-3dB}}} \\ &= \frac{\frac{A_{OL}}{1+\frac{s}{\omega_{-3dB}}}}{1+\frac{s}{1+A_{OL}\omega_{-3dB}}} \end{aligned}$$

Note that the closed-loop pole is approximately equal to the unity-gain bandwidth:

$$\begin{aligned} \tau &= \frac{1}{1+A_{OL}\omega_{-3dB}} \\ &\approx \frac{1}{A_{OL}\omega_{-3dB}} \end{aligned} \tag{1}$$

Therefore, the time-domain step response of the system (including the initial conditions) is:

$$y(t) = 1 + 0.25(1 - e^{\frac{t}{\tau}}) \tag{2}$$

In order to meet the minimum settling time constraint of $0.5LSB$ at $0.48T_{sample}$ we set $y(0.48T_{sample}) = 0.5 * (2/2048)$. Rearranging Equation 2 for τ gives:

$$\begin{aligned} \tau &= -\frac{0.48T_{sample}}{ln(1 - \frac{1.25-0.5LSB}{1.25})} \\ \Rightarrow A_{OL}\omega_{-3dB} &= 261.89 \text{ rad s}^{-1} \\ \therefore f_0 &= 41.6 \text{ MHz} \end{aligned} \tag{3}$$

which defines our minimum unity-gain bandwidth.

2.2 Open-loop gain, A_{OL}

To derive the open-loop gain, we simply consider the closed-loop gain of the amplifier, given by:

$$\frac{V_{out}}{V_{in}} = \frac{A_{OL}}{1 + A_{OL}} \tag{4}$$

To meet the DC gain error requirement we require V_{out} in Equation 4 to be less than 0.25LSB for V_{in} = 1.25V. Therefore:

$$\begin{aligned} 0.25\text{LSB} &= \frac{A_{OL}}{1 + A_{OL}} \\ 0.25 \times \frac{2}{2^{11}} &= \frac{A_{OL}}{1 + A_{OL}} \\ \Rightarrow A_{OL} &\approx 2500 \end{aligned}$$

2.3 Open-loop pole, f_{-3dB}

Now that we have f_{0dB} and A_{OL} we can derive the minimum open-loop pole using the following expression for Gain-Bandwidth Product:

$$\begin{aligned} f_{0\text{dB}} &= A_{OL}f_{-3\text{dB}} \\ \Rightarrow f_{-3\text{dB}} &= 16.6 \text{ kHz} \end{aligned}$$

2.4 Output impedeance and transconductance gain, R_{out} and G_m

Using the aforementioned parameters, we can derive R_{out} by using the following expression of the open-loop pole:

$$f_{-3\text{dB}} = \frac{1}{2\pi RC_{in}} \tag{5}$$

Using Equation 5 to do this shows:

$$R_{out} = \frac{1}{2\pi f_{-3\text{dB}} C_{in}}$$
$$R_{out} \approx 5.1\text{M}\Omega$$

To derive G_m we use the formula:

$$\omega_{0\text{dB}} = \frac{G_m}{C_{in}}$$
$$G_m = 601\mu\text{S} \tag{6}$$

3 Amplifier Design

Reviewing the derived amplifier specifications reveals a high open-loop gain, and a moderately high bandwidth. Therefore, a folded-cascode toplogy was chosen as the cascode devices can give us the high gain as well as a moderately high swing. Figure 2 illustrates the topology.

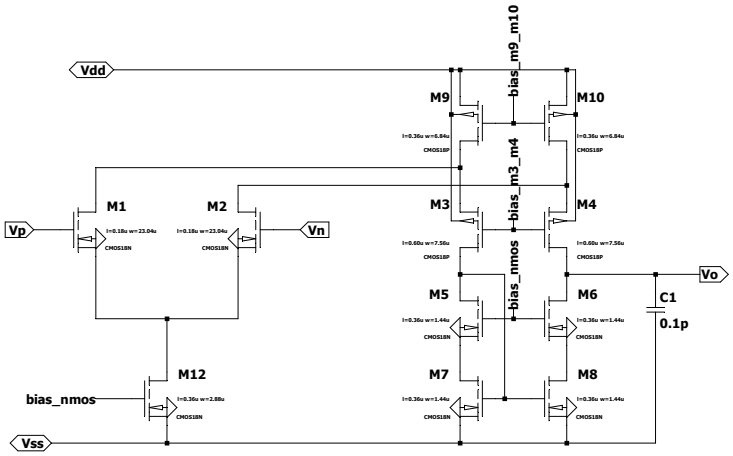


Figure 2: Folded-cascode amplifier with NMOS input differential pair. A small 0.1pF capacitor was added to stabilise the amplifier when the load is disconnected.

3.1 Transistor Sizing Methodology

As there are a lot of transistors in this topology, the op-amp design methodology described in [1] was followed with some modifications. The strategy described is as follows:

- Define a current budget and allocate currents on each device
- Consider the required output swing and allocate overdrive voltages, V_{OV} to each device
- Calculate the required W/L ratios of each device
- Calculate the g_m and r_{DS}, and therefore the gain, A
- If applicable, iterate by changing device widths and lengths to match the gain

The following equations are relevant to this discussion are

$$I_{DS} = \frac{\mu C_{OX}}{2m}\frac{W}{L}V_{OV}^2 \tag{7}$$

$$g_m = \sqrt{\frac{2I_{DS}\mu C_{OX}W}{2mL}} \tag{8}$$

$$A = g_{m[1,2]}\left[g_{m[3,4]}r_{DS[3,4]}(r_{DS[9,10]}||r_{DS[1,2]})||g_{m[5,6]}r_{DS[5,6]}r_{DS[7,8]}\right] \tag{9}$$

Note that Equation 9 is the small signal gain of this amplifier. Let us set a current budget of 100μA. We allocate 50μA to transistors M9 and M10. Through KCL, we determine the currents through the rest of the transistors described in Table 2.

Device	Current (μA)	V_{OV} (mV)
M1 & M2	25	-
M3 & M4	25	200
M5 - M8	25	250
M9 - M10	50	300
M12	50	-

Table 2: Allocation of I_{DS} currents and V_{OV} voltages.

We than allocate overdrive voltages to the devices according to the swing we specify. The upper and lower bound, and the common-mode voltage is determined by the following:

$$\begin{aligned} V_{cm[max]} &= V_{DD} - V_{OV[9,10]} - V_{OV[3,4]} \\ V_{cm[min]} &= 2V_{OV[5:8]} \end{aligned} \tag{10}$$

We can skip the iterative method and calculate the W/L of M1 and M2 by considering the required $g_{m[1,2]}$ using Equation 8. We can also ignore calculating M12 because that serves as part of the tail current source for the differential pair and therefore, is sized according to the biasing of M5-M8. The rest of the transistors are calculated via iteration and are described in Table 3.

	Initial	Final		
Device	W/L	W/L	Width (μm)	Length (μm)
M1 & M2	-	128	23	0.18
M3 & M4	20.3	11.1	7.56	0.60
M5 - M8	3.35	3.6	1.44	0.40
M9 - M10	18.0	19	6.84	0.36
A	519	2588		

Table 3: Table of transistor dimensions. The initial gain was calculated with $L = 0.18\mu$m.

A MATLAB script was written to go through the iteration process faster.

3.2 Bias Circuit

To bias the transistors in the amplifier, we employ current mirrors as illustrated in Figure 3. We simply size these transistors according to how much current each device in the amplifier circuit requires which is described in Table 2.

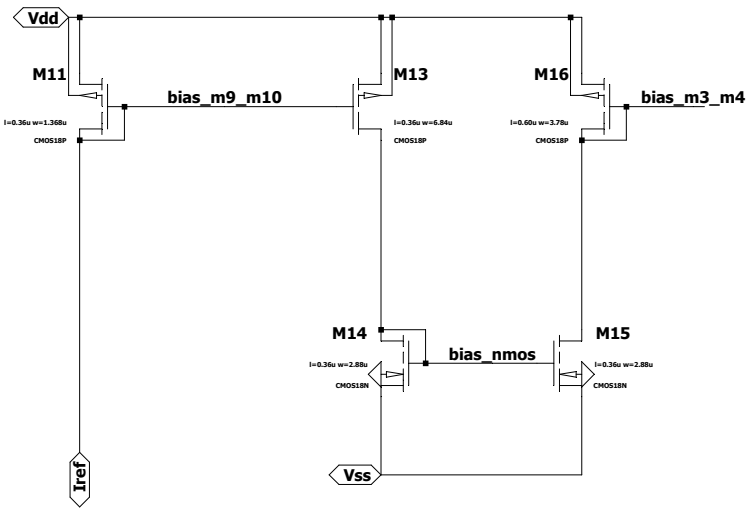


Figure 3: Caption

The dimensions of these transistors are described in Table 4.

Device	Width (μ)m	Length (μm)
M11	0.36	1.368
M13	0.36	6.84
M14 & M15	0.36	2.88
M16	0.36	3.78

Table 4: Bias circuit transistor dimensions.

4 Simulation Results and Analysis

The amplifier described in section 3 was simulated. All results can be found in section 6.

4.1 DC characteristics

With a DC operating point simulation, we obtain an output voltage of 1.25017V. This is less than the upper bound for the DC gain error of no more than 0.25LSB, therefore meeting the specification. Is is notable that the output voltage is *higher* than the input voltage which could not be predicted by Equation 4 as this suggests that the closed-loop gain is higher than 1. This is due to the non-ideal offset voltage of the amplifier.

Figure 4 shows the DC response of the amplifier. As demonstrated

4.2 Frequency Response

Figure 5 shows the frequency response of the amplifier in both loaded and unloaded conditions. The phase margin in both cases are 78.6°and 52.5°respectively which complies with the specification. However, small-signal gain is around 47dB, which is much lower compared to the hand-calculations. This also applies to the unity-gain bandwidths, around 360MHz and 25.9MHz for unloaded and loaded respectively.

4.3 Transient Response

As demonstrated in Equation 2, the amplifier is able to charge the load capacitance up to 1.24962V in 30ns which complies with the settling error and time of 0.5LSB within $0.48T_{sample}$ constraint. While this does meet the specification, it does contrast to the low-gain and bandwidth results which suggest that the amplifier should not be able to meet the specification. The amplifier still does meet the requirements because, supported by the DC simulation response, there is enough DC offset reduce the required step response.

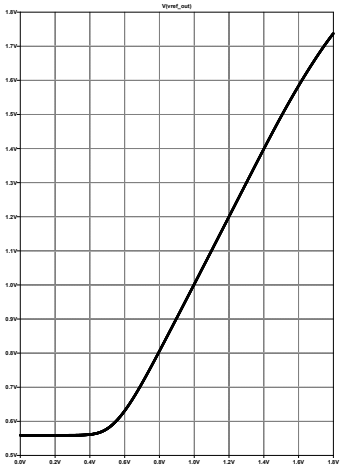
5 Conclusion

To conclude this assignment, a folded-cascode operational amplifier was designed which achieves the provided constraints and derived top-level specification. To improve upon this design, considerations for matching and noise should be added.

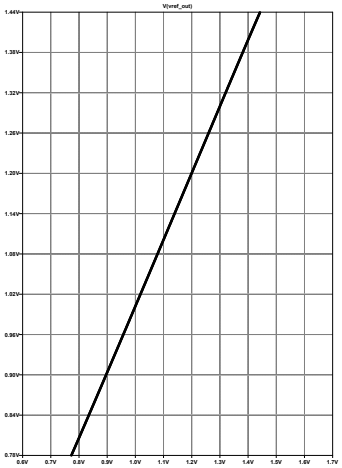
6 Appendix

Device	I_{DS}	g_m	R_{DS}	V_{DS}	V_{DSAT}
Amplifier Devices					
M1	2.53e-05	5.94e-04	80.0e3	9.31e-01	5.48e-02
M2	2.54e-05	5.96e-04	79.4e3	9.30e-01	5.48e-02
M3	2.01e-05	1.60e-04	202.4e3	-2.67e-01	-2.00e-01
M4	-2.00e-05	1.62e-04	357.4e3	-3.08e-01	-1.99e-01
M5	2.01e-05	2.10e-04	564.9e3	1.27	1.64e-01
M6	2.00e-05	2.09e-04	561.8e3	1.23	1.65e-01
M7	2.01e-05	2.03e-05	1.29e3	2.52e-02	5.15e-01
M8	2.00e-05	2.02e-05	1.29e3	2.52e-02	5.15e-01
M9	-4.54e-05	2.84e-04	29.8e3	-2.41e-01	-2.34e-01
M10	-4.54e-05	2.85e-04	30.3e3	-2.42e-01	-2.34e-01
M12	5.07e-05	4.51e-04	191.9e3	6.28e-01	1.88e-01
Bias Devices					
M11	-1.00e-05	6.51e-05	980.4e3	-7.46e-01	-2.32e-01
M13	-5.11e-05	3.37e-04	208.3e3	-1.10	-2.35e-01
M14	5.11e-05	4.54e-04	203.7e3	7.05e-01	1.88e-01
M15	5.16e-05	4.57e-04	214.1e3	8.01e-01	1.88e-01
M16	-5.16e-05	1.67e-04	357.1e3	-9.99e-01	-4.22e-01

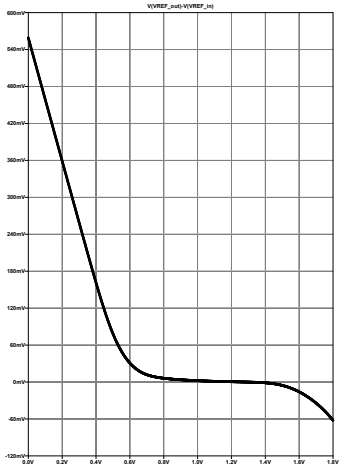
Table 5: Device parameters extracted from DC operating point simulation (V_{in} = 1.25V).



(a) DC transfer characteristic

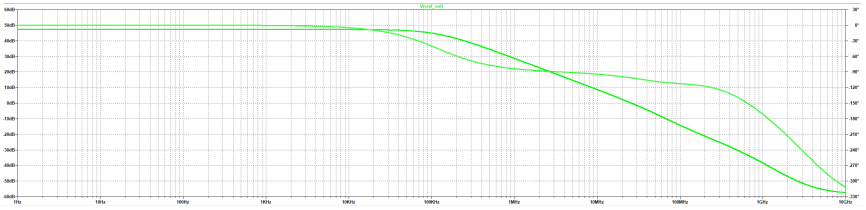


(b) Linear region

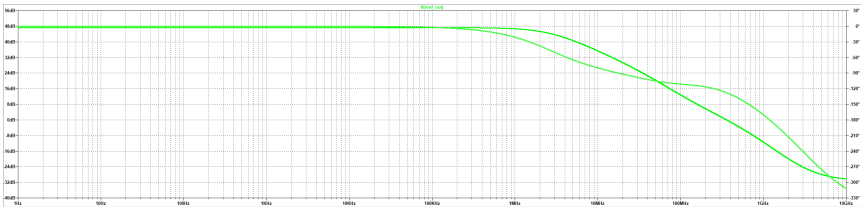


(c) $V_{out} - V_{in}$ vs V_{CM}

Figure 4: DC simulations of amplifier. The DC operating point at 1.25V is 1.25017V

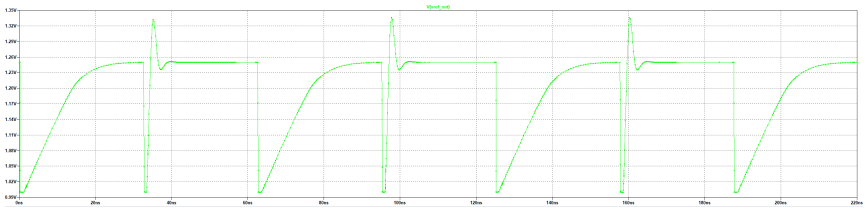


(a) Loaded

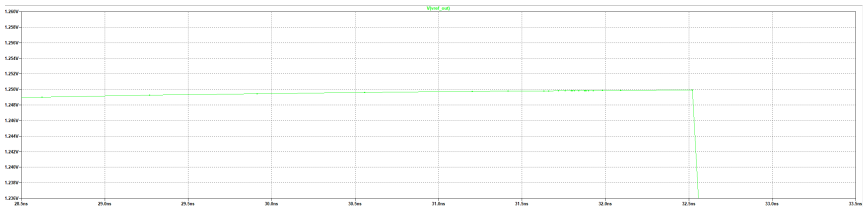


(b) Unloaded

Figure 5: Frequency response of amplifier. $f_{0(load)}$ = 25.9MHz, $f_{0(noload)}$ = 360MHz. PM_{load} = 78.6°, PM_{noload} = 52.5°. The gain is around 47dB.



(a) 2 acquisition and conversion periods



(b) Settling time

Figure 6: Transient response of amplifier in desired application. The settling voltage is around 1.24962V at 30ns.

References

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits 2nd Edition*. Electrical Engineering Series, McGraw-Hill, 2001.