



Banana Pi

Compute module 4

A Banana Pi for deeply compute
embedded application

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Chapter 1. Introduction

1.1 Introduction

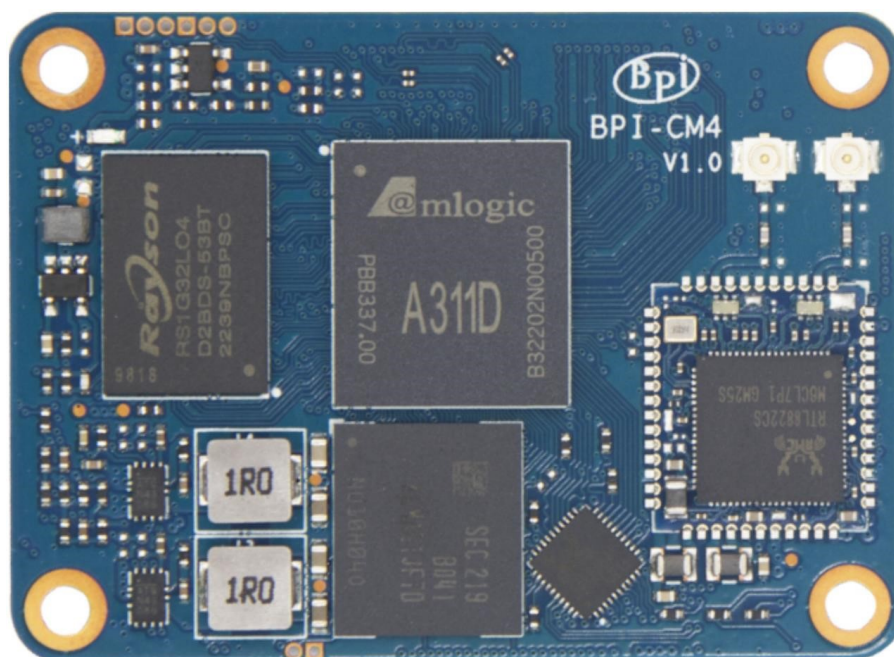


Figure 1. The BPI-CM4

The Banana Pi Compute Module 4(CM4) is a System on Module(SoM) containing processor, DRAM, eMMC Flash and supporting power circuitry. These modules allow a designer to use the Banana Pi hardware and software stack in their own custom systems and form factors. And, these modules offer additional IO interfaces beyond what is provided on Banana Pi boards, providing designers with more options.

The design of the CM4 is loosely based on the Amlogic A311D, Quad core ARM Cortex-A73 and dual core ARM Cortex-A53 CPU, ARM G52MP4(6EE) GPU, NPU for AI at 5.0 TOPS, support Camera and MIPI-CSI interface, HDMI output, 2 Gigabit port, 4G RAM and 16 GB eMMC flash.

for A311D chip PIN limited. just support 1 HDMI, 1 CSI and 1 DSI, Raspberry Pi support 2 HDMI, 2 CSI and 2 DSI, Other is Pin2Pin. you can use Raspberry Pi CM4 baseboard.



for A311D chip PIN limited. just support 1 HDMI, 1 CSI and 1 DSI, Raspberry Pi support 2 HDMI, 2 CSI and 2 DSI, Other is Pin2Pin. you can use Raspberry Pi CM4 baseboard.

1.2 Key Feature

Key feature of the BPI-CM4 are as follows:

- Amlogic A311D Quad core ARM Cortex-A73 and dual core ARM Cortex-A53,ARM G52 MP4(6EE) GPU
- NPU for AI Next generation, deep-neural-network applications, at 5.0 TOPS
- OpenGL ES 3.2, Vulkan 1.1 and OpenCL 2.0 support
- 4GB LPDDR4 RAM
- 16GB eMMC flash (Max 128G)
- MIPI DSI :
 - 1x4-Lane MIPI DSI Display Interface
- MIPI CSI :
 - 1x4-Lane MIPI CSI Camera Interface
- PCIe Interface:
 - 1xPCIe 1-Lane Host,Gen 2(5Gbps)
- HDMI Interface:
 - 1xHDMI 2.1 Output Interface(up tp 4Kx2K@60)
- Gigabit Ethernet PHY supporting
- GPIOs:
 - PCM
 - IIC
 - IIS
 - SPI
 - UART
 - PWM
 - ...
- Single +5V PSU Input
- Support Android and Linux system
- Size: 55x40mm

Chapter 2. Interfaces

2.1 Wireless

The BPI-CM4 supports an onboard wireless module based on Realtek RTL8822CS, supports both

- 2.4GHz & 5GHz IEEE 802.11 a/b/g/n/ac 2x2 MIMO wireless
- Bluetooth 5.0 BR/EDR/LE

These wireless interfaces can be individually enabled or disabled as required via CPU GPIO. In the case of many application environments, a service engineer can enable wireless operation and then disable it when done.

The CPU can also turn on the wireless by itself for data communication, and turn off the wireless after completion to reduce power consumption.

The BPI-CM4 has two standard IPEX-1G connector on the module, If you want to use 2x2 MIMO, need to connect 2x 2.4G&5G antenna.

Banana Pi Ltd has an antenna kit which is certified to be used with the BPI-CM4. If a different antenna is used then separate certification will be required.

2.2 Ethernet

The BPI-CM4 has an onboard Gigabit Ethernet PHY - the [REALTEK RTL8211F](#) - some of the major features of this PHY include;

- IEEE 802.3az-2010
- Built-in Wake-on-LAN
- Crossover Detection & Auto-Correction

A standard RJ45 connector is necessary to provide an Ethernet connection to the BPI-CM4. Can be seen in [Figure 2](#)

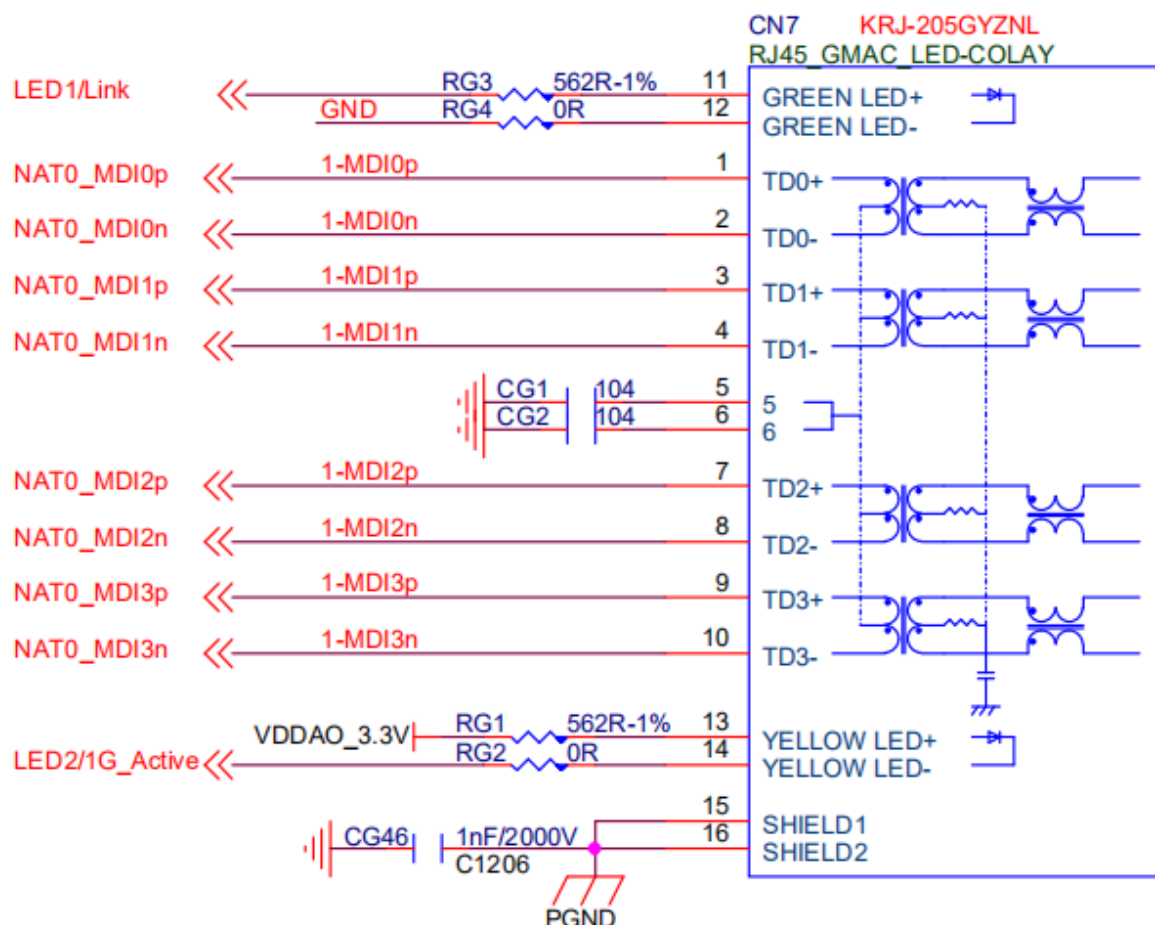


Figure 2. Ethernet Schematic

The differential Ethernet signals should be routed as 100Ω differential pairs, with suitable clearances. Length matching between pairs should be better than 50mm, so in the typical case no length matching is required. However the signals within a pair need to be length matched, ideally to better than 0.15mm.

The PHY also supports up to 2 LEDs to give user status feedback, these are low active. These LEDs can have a range of functions, and you should consult your OS driver to see which functions are supported by your driver.

2.3 PCIe(Gen2 x1)

The BPI-CM4 has an internal PCIe2.0 x1 host controller. Connecting a PCIe device follows the standard PCIe convention. The CM4 has onboard AC coupling capacitors for **PCIe_CLK** and **PCIe_TX** signals. However the **PCIe_RX** signals need external coupling capacitors close to the driving source (the device **TX**), if you are using an external PCIe/NVMe cards these capacitors will be onboard. The PCIe conversion is that if you are wiring directly to an IC then the TX and RX pairs need to be swapped (TX → RX, RX → TX). If you are wiring to a connector then this is typically labelled from the host post of view and so TX RX swaps aren't required. Additionally the **PCIECK_REQN** must be connected to ensure the CM4 produces a clock signal, and the **PERST0_N** should also be connected to ensure the device is correctly reset when required. The differential PCIe signals should be routed as 100Ω

differential pairs, with suitable clearances. There is no need to match the lengths between pairs, only the signals within a Pair need to be length matched ideally to better than 0.1mm



5.10 kernel and

2.4 USB 2.0(HS)/3.0(SS)

The USB 2.0 interface supports up to 480Mbps signalling. The differential pair should be routed as a 90Ω differential pair. The P N signals should ideally be matched to better than 0.15mm.



USB 3.0 or PCIe 2.0 x1

USB 3.0 multiplexed with **PCIe 2.0 x1**. **USB30_RX_P/N** multiplexed with **PCIe_RX_P/N** and **USB30_TX_P/N** multiplexed with **PCIe_TX_P/N**.

BPI-CM4 has two full-speed USB channels, one of which (USB_A) can be USB2.0 x1+ PCIe2.0 x1 or USB3.0 x1, or can use FE1.1s chip (USB 2.0 HUB chip) or VL807 (USB 3.0 HUB chip) Expanded to four-way USB. The other one (USB_B) interface also has OTG(On-The-Go) function at the same time.

2.5 GPIO

BPI-CM4 has 17 pins available for general purpose I/O (GPIO), corresponding to the first half of the standard 40 pins of other BananaPi development boards. These pins have access to internal peripherals; PCM, IIC, UART and PWM. [BPI-CM4 Sch](#) describes these features in detail, and the multiplexing options available. The drive strength and slew rate should ideally be set as low as possible to reduce any EMC issues. GPIOX_17 and GPIOX_18 have 2.2K pull up resistors.

By default, GPIO bank is powered by 3V3, but GPIOX_x GPIOs can be changed to powered by 1.8V.



GPIOX_x Power Bank depending on the selected WiFi module, PCIe WiFi or RTL WiFi (default) is powered by 3.3V, and AMPAK 6275s WiFi is powered by 1.8V.

GPIO

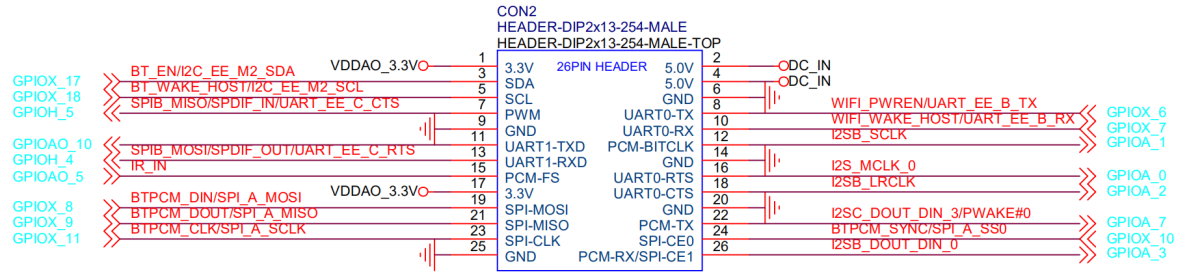


Figure 3. GPIO

2.5.1 Alternative Function Assignments

Table 1. GPIO Alternative Function Assignments

Num	GPIOx_x	PD/PU	ALT0	ALT1	ALT2
3	GPIOX_17	PU	GPIO	I2C_EE_M2_SDA	BT_EN
5	GPIOX_18	PU	GPIO	I2C_EE_M2_SCL	BT_WAKE_HOST
7	GPIOH_5	PU	GPIO	SPDIF_IN	
8	GPIOX_6	PU	GPIO	UART_B_TX	WIFI_PWREN
10	GPIOx_7	PU	GPIO	UART_B_RX	WIFI_WAKE_HOST
11	GPIOAO_10	PD	GPIO		
12	GPIOA_1	PU	GPIO	I2SB_SCLK	
13	GPIOH_4	PD	GPIO	SPDIF_OUT	
15	GPIOAO_5	PU	GPIO	IR_IN	
16	GPIOA_0	PU	GPIO	I2S_MCLK	
18	GPIOA_2	PD	GPIO	I2SB_LRCLK	
19	GPIOX_8	PU	GPIO	SPI_A_MOSI	BTPCM_DIN
21	GPIOX_9	PU	GPIO	SPI_A_MISO	BTPCM_DOUT
22	GPIOA_7	PU	GPIO	I2SC_DOUT_DIN_3	
23	GPIOX_11	PU	GPIO	SPI_A_CLK	BTPCM_CLK
24	GPIOX_10	PU	GPIO	SPI_A_SS0	BTPCM_SYNC
26	GPIOA_3	PU	GPIO	I2SB_DOUT_DIN_0	

2.6 HDMI

The BPI-CM4 supports one HDMI 2.1 interface, it capable of driving 4Kx2K 60fps output.

HDMI signals should be routed as 100Ω differential pairs, each signal within a pair should ideally be matched to better than 0.15mm. Pairs don't typically need any extra matching as

they only have to be matched to 25mm.

CEC, Dynamic HDR and HDCP 2.2 supported. CEC internal 27K pullup resistor and **HDMI_SDA/HDMI_SCL** internal 27K pullup resistor is included in the BPI-CM4.

The BPI-CM4 need extra ESD protection maybe required.

2.7 CSI(MIPI Serial Camera)

The BPI-CM4 supports one camera ports(4 lanes); CSI signals should be routed as 100Ω differential pairs, each signal within a pair should ideally be matched to better than 0.15mm.

The documentation around the CSI interface can be found on the [BananaPi Wiki](#) website while Linux kernel drivers can be found on [Github](#).



Camera sensors supported by the official BananaPi firmware are;ShenZhenShi HongJia OS08A10 V11(sensor: OS08A20). no security device is required on Compute Module devices to use these camera sensors.

2.8 DSI(MIPI Serial Display)

The BPI-CM4 supports one display ports(4 lanes); supports a maximum of data rate per lane of 1Gbit/s.

The DSI interface only supported by offical BananaPi firmware are supported DSI Displays, more infomation can see [BananaPi Wiki](#) website.DSI signals should be routed as 100Ω differential pairs, each signal within a pair should ideally be matched to better than 0.15mm.



BananaPi firmware only supports officially recommended DSI displays, but add and compile your own driver.

2.9 IIC(GPIO Pin3&Pin5)

This IIC bus is not shared with CSI or DSI and can be used arbitrarily.

2.10 IIC(CAM0_SCK/SDA)

This IIC bus(GPIOH_7/GPIOH_6) is used by default for MIPI CSI(Camera sensor), If you don't use, it can also be used for general purpose I/O or to connect other IIC devices.

2.11 IIC(TP_SCK/SDA)

This IIC bus(GPIOA_15/GPIOA_14) is used by default for MIPI DSI Touch Panel(capacitive touch panel), If you don't use, it can also be used for general purpose I/O or to connect other IIC devices.



All IIC buses have 2K2 pull-up resistors on BPI-CM4

2.12 SDIO/eMMC()

The BPI-CM4 supported 16GB eMMC flash (option up to 128GB). The **TF_VDD_EN** signal is used to enable an external power switch to turn on power to the TF_Card. If booting from TF_Card is required then a pullup resistor must also be fitted to default the power to be on.

MICRO SD

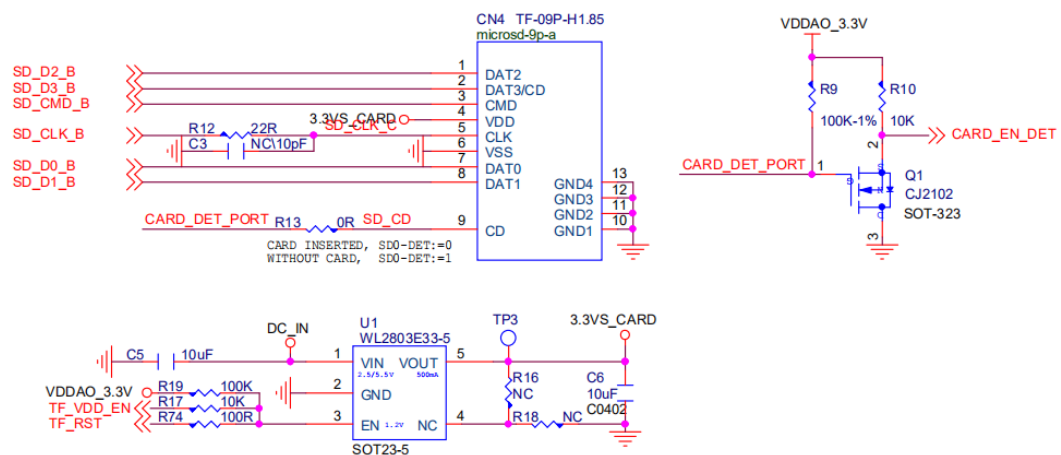


Figure 4. TF Card

2.13 Analog(SARADC_CH2/CH3)

These are the two ADC pins straight out of the CPU.No onboard filtering, 100K pull-up resistors on BPI-CM4.



If you need to use these two ADC pins, you need to consider adding filtering, the recommended value is $1000\text{pF} \sim 0.1\mu\text{F}$

2.14 CPU RST

Pulling this pin low places BPI-CM4 in reset. Removing the pull-down state allows the BPI-CM4 to reset and run again.



To reset BPI-CM4, the **CPU_RST** pin needs to be pulled low for at least 0ms. $T_{CPU_RST_L}>0ms$.

2.15 SYS_LED

This pin is designed to drive an LED to show the BPI-CM4 operating status. If an error occurs during startup, it will blink with the **SYS_LED2** beyond expectations to help the user easily determine the status.

2.16 SYS_LED2

This pin is designed to drive an LED to show the BPI-CM4 operating status. If an error occurs during startup, it will blink with the **SYS_LED2** beyond expectations to help the user easily determine the status.

Chapter 3. Electrical and Mechanical

3.1 Mechanical

The BPI-CM4 is a compact $40 \times 55\text{mm}$ module. The Module is 4.1mm deep, but usually the height after connection is 4.4mm.



The height of 4.4mm after connection is the minimum height between the connector and the fixing stud recommended by bpi. If other connectors and fixing studs of the corresponding height are used, the height needs to be actually measured.

1. $4 \times \text{M3}$ Mounting holes (inset about 4mm from module edge)
2. PCB thickness $1.2\text{mm} \pm 10\%$
3. [Amlogic A311D](#) SoC height including solder balls $1.0 \pm 0.11\text{mm}$
4. Stacking height either:
 - a. 1.5mm with mating connector (clearance under CM4 0mm) : DF40C-100DS-0.4v
 - b. 3.0mm with mating connector (clearance under CM4 1.5mm): DF40HC(3.0)-100DS-0.4v

If the wireless antenna is used it must be orientated towards the edge of the plastic enclosure and any close by metal must have cut outs or the wireless performance will be degraded. It is recommended to fix the antenna outside the case.

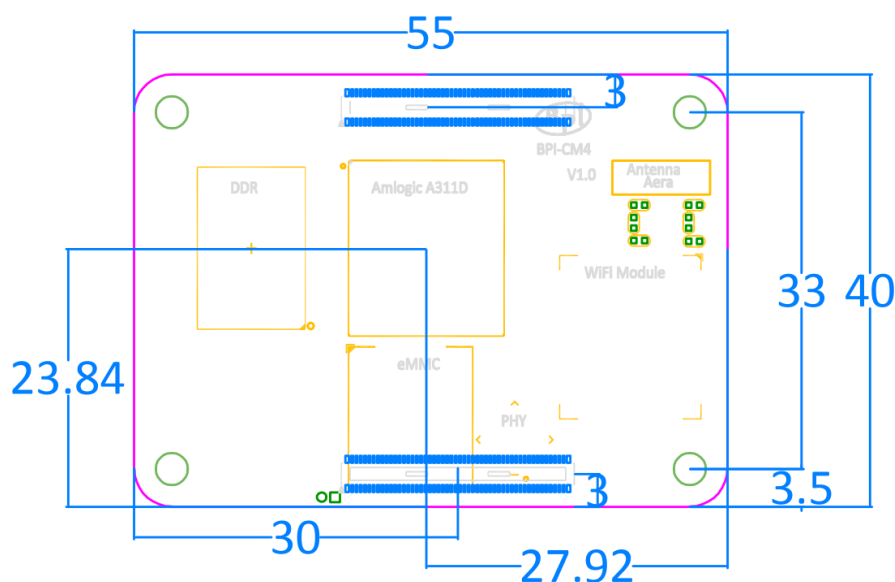


Figure 5. Mechanical



The location and arrangement of components on the Compute Module may change slightly over time due to revisions for cost and manufacturing considerations; however the maximum component

heights and PCB thickness will be kept as specified.

3.2 Thermal

The BPI-CM4 has less passive cooling due to its smaller size, so it may run hotter. In order to ensure the life of BPI-CM4, the core temperature of the main control chip (Amlogic A311D) should be kept below 85 degrees Celsius as much as possible. If the core temperature is found to be higher than 85 degrees Celsius, you can reduce the clock frequency or add additional active and passive cooling methods.

It is important that thermal solution chosen keeps the ambient temperature for the other silicon devices on the CM4 within the operating temperature range.

Operating temperature range: -20°C - +85°C Non-condensing.

3.3 Electrical Specification



Stresses above those listed in Table 3 may cause permanent damage to the device. This is a stress rating only; functional operation of the device under these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V _{IN}	+5V_Input	-0.5	6	V
V _{GPIO_ref}	GPIO Voltage	-0.5	3.6	V
V _{GPIO}	GPIO INPUT Voltage	-0.5	V _{GPIO_ref} +0.5	V

DC Electrical Characteristics

Table 3. Normal GPIO Specifications (For DIO)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IH(gpio)}	High-level Input Voltage	IOVREF/2+0.3		VDDIO+0.3	V
V _{IL(gpio)}	Low-level Input Voltage	-0.3		IOVREF/2-0.3	V
R _{PU/PD}	Built-in pull Up/Down resistor		60K		ohm
IoH/IoL	GPIO driving capability	4 ¹⁾		6 ²⁾	mA

Symbol	Parameter	Min.	Typ.	Max.	Unit
VOH	Output high level with 4 mA loading	VDDIO-0.5			V
VOL	Output low level with 4 mA loading			0.4	V



Minimal driving capability applies when VDDIO LV 1.71V, or VDDIO HV 3.0V, VOL<0.4V Maximal driving capability only applies to applications such as driving LED when VOL<0.6V.

Table 4. Open Drain GPIO Specifications (For DIO_OD)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{IH(OD5V)}	High-level Input Voltage	2.2		5.5	V
V _{IL(OD5V)}	Low-level Input Voltage	-0.3		0.8	V
V _{IH(OD3.3V)}	High-level Input Voltage	2.2		3.6	V
V _{IL(OD3.3V)}	Low-level Input Voltage	-0.3		0.8	V
R _{PU/PD}	No built-in pull up/down resistor on OD IO	-	-	-	ohm
I _O	OD IO driving low capability	4 ¹⁾		6 ²⁾	mA
VOL	Output low level with mini I _O loading			0.4	V



Minimal driving capability applies when VDDIO LV 1.71V, or VDDIO HV 3.0V, VOL<0.4V Maximal driving capability only applies to applications such as driving LED when VOL<0.6V.

Chapter 4. Pin Out

4.1 Pin out define

Table 5. Pin out define of BPI-CM4

Pin Num	Signal	Description
1	GND	Ground (0V)
2	GND	Ground (0V)
3	NAT0_MDI3p	Ethernet MDI 3 Positive (connect to Transformer or RJ45 Connector)
4	NAT0_MDI1p	Ethernet MDI 1 Positive (connect to Transformer or RJ45 Connector)
5	NAT0_MDI3n	Ethernet MDI 3 Negative (connect to Transformer or RJ45 Connector)
6	NAT0_MDI1n	Ethernet MDI 1 Negative (connect to Transformer or RJ45 Connector)
7	GND	Ground (0V)
8	GND	Ground (0V)
9	NAT0_MDI2n	Ethernet MDI 2 Negative (connect to Transformer or RJ45 Connector)
10	NAT0_MDI0n	Ethernet MDI 0 Negative (connect to Transformer or RJ45 Connector)
11	NAT0_MDI2p	Ethernet MDI 2 Positive (connect to Transformer or RJ45 Connector)
12	NAT0_MDI0p	Ethernet MDI 0 Positive (connect to Transformer or RJ45 Connector)
13	GND	Ground (0V)
14	GND	Ground (0V)
15	Ethernet_LED2/1G_Active	Low Active Ethernet Activity indicator (3.3V signal) Typically a Yellow LED is connected to this pin.Represents the negotiated rate
16	LINUX_Debug_RX	Debug Uart RX.Usually under Linux system
17	Ethernet_LED1/Link	Low Active Ethernet Activity indicator (3.3V signal) Typically a Green LED is connected to this pin.Represents the link state
18	LINUX_Debug_TX	Debug Uart TX.Usually under Linux system

Pin Num	Signal	Description
19	Ethernet_0_LED0/C FG_EXT	Reserved.From PHY chip
20	NC	No connection pin.
21	SYS_LED2	Low Active Pi Activity LED.Max 3.3V tolerant (VOL<0.4V). Default drives the Green LED
22	GND	Ground (0V)
23	GND	Ground (0V)
24	GPIOA_0	General purpose input/output bank A signal 0.Typically a 3.3V signal
25	GPIOA_3	General purpose input/output bank A signal 3.Typically a 3.3V signal
26	GPIOA_2	General purpose input/output bank A signal 2.Typically a 3.3V signal
27	GPIOA_4	General purpose input/output bank A signal 4.Typically a 3.3V signal
28	GPIOA_7	General purpose input/output bank A signal 7.Typically a 3.3V signal
29	GPIOAO_11	General purpose input/output bank AO signal 11.Typically a 3.3V signal
30	GPIOAO_10	General purpose input/output bank AO signal 10.Typically a 3.3V signal
31	GPIOH_5	General purpose input/output bank H signal 5.Typically a 3.3V signal
32	GND	Ground (0V)
33	GND	Ground (0V)
34	GPIOH_4	General purpose input/output bank H signal 4.Typically a 3.3V signal
35	GPIOA_15	General purpose input/output bank A signal 15.Typically a 3.3V signal
36	GPIOA_14	General purpose input/output bank A signal 14.Typically a 3.3V signal
37	GPIOAO_5	General purpose input/output bank AO signal 5.Typically a 3.3V signal
38	GPIOX_11	General purpose input/output bank X signal 11.Typically a 3.3V signal

Pin Num	Signal	Description
39	GPIOX_10	General purpose input/output bank X signal 10. Typically a 3.3V signal
40	GPIOX_9	General purpose input/output bank X signal 9. Typically a 3.3V signal
41	GPIOA_11	General purpose input/output bank A signal 11. Typically a 3.3V signal
42	GND	Ground (0V)
43	GND	Ground (0V)
44	GPIOX_8	General purpose input/output bank X signal 8. Typically a 3.3V signal
45	GPIOA_12	General purpose input/output bank A signal 12. Typically a 3.3V signal
46	GPIOA_5	General purpose input/output bank A signal 5. Typically a 3.3V signal
47	GPIOA_13	General purpose input/output bank A signal 13. Typically a 3.3V signal
48	GPIOA_6	General purpose input/output bank A signal 6. Typically a 3.3V signal
49	GPIOA_1	General purpose input/output bank A signal 1. Typically a 3.3V signal
50	GPIOA_9	General purpose input/output bank A signal 9. Typically a 3.3V signal
51	GPIOX_7	General purpose input/output bank X signal 7. Typically a 3.3V signal
52	GND	Ground (0V)
53	GND	Ground (0V)
54	GPIOA_10	General purpose input/output bank A signal 10. Typically a 3.3V signal.
55	GPIOX_6	General purpose input/output bank X signal 6. Typically a 3.3V signal.
56	GPIOX_18	General purpose input/output bank X signal 18. Typically a 3.3V signal.
57	SD_CLK_B	SDCARD Clock signal.
58	GPIOX_17	General purpose input/output bank X signal 17. Typically a 3.3V signal.
59	GND	Ground (0V)

Pin Num	Signal	Description
60	GND	Ground (0V)
61	SD_D3_B	SDCARD Data3 signal.
62	SD_CMD_B	SDCARD Command signal.
63	SD_D0_B	SDCARD Data0 signal.
64	NC	No connection pin.
65	GND	Ground (0V)
66	GND	Ground (0V)
67	SD_D1_B	SDCARD Data1 signal.
68	NC	No connection pin.
69	SD_D2_B	SDCARD Data2 signal.
70	NC	No connection pin.
71	GND	Ground (0V)
72	NC	No connection pin.
73	NC	No connection pin.
74	GND	Ground (0V)
75	TF_VDD_EN	Output to Power switch for the SDCARD. The CM4 sets this pin High (3.3V) to signal that Power to the SDCARD should be turned on. If booting from the SDCARD is required then a pullup should also be fitted so the power defaults to on.
76	CARD_DET	SDCARD detection signal.
77	+5V_Input	4.75V-5.25V Main power input
78	NC	No connection pin.
79	+5V_Input	4.75V-5.25V Main power input.
80	GPIOH_7	General purpose input/output bank H signal 7. Typically a 3.3V signal.
81	+5V_Input	4.75V-5.25V Main power input.
82	GPIOH_6	General purpose input/output bank H signal 6. Typically a 3.3V signal.
83	+5V_Input	4.75V-5.25V Main power input..
84	CM4_3V3_OUTPUT	3.3V +/-2.5% Power Output. Usually not used as an extended power supply it can be used as a reference potential.
85	+5V_Input	4.75V-5.25V Main power input.

Pin Num	Signal	Description
86	CM4_3V3_OUTPUT	3.3V +/-2.5% Power Output.Usually not used as an extended power supply it can be used as a reference potential.
87	+5V_Input	4.75V-5.25V Main power input.
88	CM4_1V8_OUTPUT	1.8V +/-2.5% Power Output.Usually not used as an extended power supply it can be used as a reference potential.
89	NC	No connection pin.
90	CM4_1V8_OUTPUT	1.8V +/-2.5% Power Output.Usually not used as an extended power supply it can be used as a reference potential.
91	NC	No connection pin.
92	CPU_RST	System reset input.Pull low to reset the system.
93	NC	No connection pin.
94	SARADC_CH3	ADC channel 3 input.In the official firmware this pin is used as Hardware ID.
95	SYS_LED	Low active Output to drive Power On LED.
96	ADC_KEY	ADC channel 2 input.In the official firmware this pin is used as AD_KEY.
97	NC	No connection pin.
98	GND	Ground (0V)
99	NC	No connection pin.
100	GPIOH_8	General purpose input/output bank H signal 8.Typically a 3.3V signal.
101	USBOTG_B_ID	USB OTG mini-receptacle identifier.
102	PCIECK_REQN	request-acknowledge communication between PCIe devices.
103	USBOTG_B_DM	USB 2.0 Port B negative data signal(OTG).
104	USB_A_DP	USB 2.0 Port A positive data signal(HOST only).
105	USBOTG_B_DP	USB 2.0 Port B positive data signal(OTG).
106	USB_A_DM	USB 2.0 Port A negative data signal(HOST only).
107	GND	Ground (0V)
108	GND	Ground (0V)
109	PERST0_N	Used to control the reset operation of PCIe devices.
110	PCIE_CLKP	PCIe reference clock positive signal.
111	NC	No connection pin.
112	PCIE_CLKN	PCIe reference clock negative signal.

Pin Num	Signal	Description
113	GND	Ground (0V)
114	GND	Ground (0V)
115	MIPI_CSI_D0N	MIPI CSI data 0 negative input
116	PCIE_SOC_RXP	PCIE or USB3.0 input positive signal
117	MIPI_CSI_D0P	MIPI CSI data 0 positive input
118	PCIE_SOC_RXN	PCIE or USB3.0 input negative signal
119	GND	Ground (0V)
120	GND	Ground (0V)
121	MIPI_CSI_D1N	MIPI CSI data 1 negative input
122	PCIE_TX0_P	PCIE or USB3.0 output positive signal
123	MIPI_CSI_D1P	MIPI CSI data 1 positive input
124	PCIE_TX0_N	PCIE or USB3.0 input negative signal
125	GND	Ground (0V)
126	GND	Ground (0V)
127	MIPI_CSI_CLKAN	MIPI CSI CLK negative input for channel A
128	NC	No connection pin.
129	MIPI_CSI_CLKAP	MIPI CSI CLK positive input for channel A
130	NC	No connection pin.
131	GND	Ground (0V)
132	GND	Ground (0V)
133	MIPI_CSI_D2N	MIPI CSI data 2 negative input
134	NC	No connection pin.
135	MIPI_CSI_D2P	MIPI CSI data 2 positive input
136	NC	No connection pin.
137	GND	Ground (0V)
138	GND	Ground (0V)
139	MIPI_CSI_D3N	MIPI CSI data 3 negative input
140	MIPI_CSI_CLKBN	MIPI CSI CLK negative input for channel B
141	MIPI_CSI_D3P	MIPI CSI data 3 positive input
142	MIPI_CSI_CLKBP	MIPI CSI CLK negative input for channel B
143	NC	No connection pin.

Pin Num	Signal	Description
144	GND	Ground (0V)
145	NC	No connection pin.
146	NC	No connection pin.
147	NC	No connection pin.
148	NC	No connection pin.
149	NC	No connection pin.
150	GND	Ground (0V)
151	HDMI_TXCEC	HDMI CEC signal.
152	NC	No connection pin.
153	HDMI_HPDC	HDMI Hot Plugin Detection
154	NC	No connection pin.
155	GND	Ground (0V)
156	GND	Ground (0V)
157	NC	No connection pin.
158	NC	No connection pin.
159	NC	No connection pin.
160	NC	No connection pin.
161	GND	Ground (0V)
162	GND	Ground (0V)
163	NC	No connection pin.
164	NC	No connection pin.
165	NC	No connection pin.
166	NC	No connection pin.
167	GND	Ground (0V)
168	GND	Ground (0V)
169	Reserved	Reserved.Audio DAC line-out right channel positive signal
170	HDMI_TX2P	HDMI TMDS data 2 positive output
171	Reserved	Reserved.Audio DAC line-out left channel positive signal
172	HDMI_TX2N	HDMI TMDS data 2 negative output
173	GND	Ground (0V)
174	GND	Ground (0V)

Pin Num	Signal	Description
175	MIPI_D0_N	MIPI DSI data 0 negative output or Bidirectional in LP mode.
176	HDMI_TX1P	HDMI TMDS data 1 positive output.
177	MIPI_D0_P	MIPI DSI data 0 positive output or Bidirectional in LP mode.
178	HDMI_TX1N	HDMI TMDS data 1 negative output.
179	GND	Ground (0V)
180	GND	Ground (0V)
181	MIPI_D1_N	MIPI DSI data 1 negative output.
182	HDMI_TX0P	HDMI TMDS data 0 positive output.
183	MIPI_D1_P	MIPI DSI data 1 positive output.
184	HDMI_TX0N	HDMI TMDS data 0 negative output.
185	GND	Ground (0V)
186	GND	Ground (0V)
187	MIPI_CLK_N	MIPI DSI clock negative output.
188	HDMI_TXCP	HDMI TMDS clock positive output.
189	MIPI_CLK_P	MIPI DSI clock positive output.
190	HDMI_TXCN	HDMI TMDS clock negative output.
191	GND	Ground (0V)
192	GND	Ground (0V)
193	MIPI_D2_N	MIPI DSI data 2 negative output.
194	MIPI_D3_N	MIPI DSI data 3 negative output.
195	MIPI_D2_P	MIPI DSI data 2 positive output.
196	MIPI_D3_P	MIPI DSI data 3 positive output.
197	GND	Ground (0V)
198	GND	Ground (0V)
199	HDMI_SDA	HDMI SDA(IIC) signal. 2.2K pull-up resistors on BPI-CM4
200	HDMI_SCL	HDMI SCL(IIC) signal. 2.2K pull-up resistors on BPI-CM4

4.2 Pin comparison between BPI-CM4 and Raspberry Pi Compute Module 4

Table 6. Pin comparison between BPI-CM4 and Raspberry Pi Compute Module 4

RPI CM4	BPI-CM4	Pin Num	Pin Num	BPI-CM4	RPI CM4
GND	GND	1	2	GND	GND
Ethernet_Pair3_P	NAT0_MDI3p	3	4	NAT0_MDI1p	Ethernet_Pair1_P
Ethernet_Pair3_N	NAT0_MDI3n	5	6	NAT0_MDI1n	Ethernet_Pair1_N
GND	GND	7	8	GND	GND
Ethernet_Pair2_N	NAT0_MDI2n	9	10	NAT0_MDI0n	Ethernet_Pair0_N
Ethernet_Pair2_P	NAT0_MDI2p	11	12	NAT0_MDI0p	Ethernet_Pair0_P
GND	GND	13	14	GND	GND
Ethernet_nLED3_1G-Active	Ethernet_LED2/1G_Active	15	16	LINUX_Debug_RX	Ethernet_SYNC_IN
Ethernet_nLED2_1G-Link	Ethernet_LED1/Link	17	18	LINUX_Debug_TX	Ethernet_SYNC_OUT
Ethernet_nLED1_Y	Ethernet_0_LED0/CFG_EXT	19	20	NC	EEPROM_nWP
Pi_nLED_Activity	SYS_LED2	21	22	GND	GND
GND	GND	23	24	GPIOA_0	I2S_MCLK/GPIO26
GPIO21/I2S_DO	GPIOA_3	25	26	GPIOA_2	I2S_LRCLK/GPIO19
GPIO20/I2S_DI	GPIOA_4	27	28	GPIOA_7	GPIO13
GPIO16	GPIOAO_11	29	30	GPIOAO_10	GPIO6
GPIO12	GPIOH_5	31	32	GND	GND
GND	GND	33	34	GPIOH_4	GPIO5
ID_SC	GPIOA_15	35	36	GPIOA_14	ID_SD
GPIO7/SPI-CE1	GPIOAO_5	37	38	GPIOX_11	SPI-CLK/GPIO11
GPIO8/SPI-CE0	GPIOX_10	39	40	GPIOX_9	SPI-MISO/GPIO9
GPIO25	GPIOA_11	41	42	GND	GND
GND	GND	43	44	GPIOX_8	SPI-MOSI/GPIO10
GPIO24/UART0-CTS	GPIOA_12	45	46	GPIOA_5	GPIO22

RPI CM4	BPI-CM4	Pin Num	Pin Num	BPI-CM4	RPI CM4
GPIO23/UART0-RTS	GPIOA_13	47	48	GPIOA_6	UART1-RXD/GPIO27
GPIO18/I2S_SCLK	GPIOA_1	49	50	GPIOA_9	UART1-TXD/GPIO17
GPIO15/UART0-RXD	GPIOX_7	51	52	GND	GND
GND	GND	53	54	GPIOA_10	PWM/GPIO4
GPIO14/UART0-TXD	GPIOX_6	55	56	GPIOX_18	SCL/GPIO3
SD_CLK	SD_CLK_B	57	58	GPIOX_17	SDA/GPIO2
GND	GND	59	60	GND	GND
SD_DAT3	SD_D3_B	61	62	SD_CMD_B	SD_CMD
SD_DAT0	SD_D0_B	63	64	NC	SD_DAT5
GND	GND	65	66	GND	GND
SD_DAT1	SD_D1_B	67	68	NC	SD_DAT4
SD_DAT2	SD_D2_B	69	70	NC	SD_DAT7
GND	GND	71	72	NC	SD_DAT6
SD_VDD_Override	NC	73	74	GND	GND
SD_PWR_ON	TF_VDD_EN	75	76	CARD_DET	Reserved/SD_DET
+5V_Input	+5V_Input	77	78	NC	GPIO_VREF
+5V_Input	+5V_Input	79	80	GPIOH_7	SCL0_Camera_3V3
+5V_Input	+5V_Input	81	82	GPIOH_6	SDA0_Camera_3V3
+5V_Input	+5V_Input	83	84	CM4_3V3_OUTPUT	CM4_3V3_OUTPUT
+5V_Input	+5V_Input	85	86	CM4_3V3_OUTPUT	CM4_3V3_OUTPUT
+5V_Input	+5V_Input	87	88	CM4_1V8_OUTPUT	CM4_1V8_OUTPUT
/WL_nDisable_3V3	NC	89	90	CM4_1V8_OUTPUT	CM4_1V8_OUTPUT
/BT_nDisable_3V3	NC	91	92	CPU_RST	RUN_PG/Reset_3V3
/nRPIBOOT_3V3	NC	93	94	SARADC_CH3	AnalogIP1/USBC_CC2

RPI CM4	BPI-CM4	Pin Num	Pin Num	BPI-CM4	RPI CM4
PI_LED_nPWR	SYS_LED	95	96	ADC_KEY	AnalogIP0/USBC_CC1
Camera_PWD_GPIO	NC	97	98	GND	GND
GLOBAL_EN_5V	NC	99	100	GPIOH_8	nEXTRST
USB_OTG_ID_3V3	USBOTG_B_ID	101	102	PCIECK_REQN	PCIe_CLK_nREQ_3V3
USB_N	USBOTG_B_DM	103	104	USB_A_DP	Reserved
USB_P	USBOTG_B_DP	105	106	USB_A_DM	Reserved
GND	GND	107	108	GND	GND
PCIe_nRST_3V3	PERST0_N	109	110	PCIe_CLKP	PCIe_CLK_P
VDAC_COMP_TV	NC	111	112	PCIe_CLKN	PCIe_CLK_N
GND	GND	113	114	GND	GND
CAM1_D0_N	MIPI_CSI_D0N	115	116	PCIe_SOC_RXP	PCIe_RX_P
CAM1_D0_P	MIPI_CSI_D0P	117	118	PCIe_SOC_RXN	PCIe_RX_N
GND	GND	119	120	GND	GND
CAM1_D1_N	MIPI_CSI_D1N	121	122	PCIe_TX0_P	PCIe_TX_P
CAM1_D1_P	MIPI_CSI_D1P	123	124	PCIe_TX0_N	PCIe_TX_N
GND	GND	125	126	GND	GND
CAM1_C_N	MIPI_CSI_CLKAN	127	128	NC	CAM0_D0_N
CAM1_C_P	MIPI_CSI_CLKAP	129	130	NC	CAM0_D0_P
GND	GND	131	132	GND	GND
CAM1_D2_N	MIPI_CSI_D2N	133	134	NC	CAM0_D1_N
CAM1_D2_P	MIPI_CSI_D2P	135	136	NC	CAM0_D1_P
GND	GND	137	138	GND	GND
CAM1_D3_N	MIPI_CSI_D3N	139	140	MIPI_CSI_CLKBN	CAM0_C_N
CAM1_D3_P	MIPI_CSI_D3P	141	142	MIPI_CSI_CLKBP	CAM0_C_P
HDMI1_HOTPLUG_5V	NC	143	144	GND	GND
HDMI1_SDA_5V	NC	145	146	NC	HDMI1_TX2_P
HDMI1_SCL_5V	NC	147	148	NC	HDMI1_TX2_N
HDMI1_CEC_5V	NC	149	150	GND	GND
HDMI0_CEC_5V	HDMI_TXCEC	151	152	NC	HDMI1_TX1_P

RPI CM4	BPI-CM4	Pin Num	Pin Num	BPI-CM4	RPI CM4
HDMI0_HOTPLUG_5V	HDMI_HPDC	153	154	NC	HDMI1_TX1_N
GND	GND	155	156	GND	GND
DSI0_D0_N	NC	157	158	NC	HDMI1_TX0_P
DSI0_D0_P	NC	159	160	NC	HDMI1_TX0_N
GND	GND	161	162	GND	GND
DSI0_D1_N	NC	163	164	NC	HDMI1_CLK_P
DSI0_D1_P	NC	165	166	NC	HDMI1_CLK_N
GND	GND	167	168	GND	GND
DSI0_C_N	NC	169	170	HDMI_TX2P	HDMI0_TX2_P
DSI0_C_P	NC	171	172	HDMI_TX2N	HDMI0_TX2_N
GND	GND	173	174	GND	GNF
DSI1_D0_N	MIPI_D0_N	175	176	HDMI_TX1P	HDMI0_TX1_P
DSI1_D0_P	MIPI_D0_P	177	178	HDMI_TX1N	HDMI0_TX1_N
GND	GND	179	180	GND	GND
DSI1_D1_N	MIPI_D1_N	181	182	HDMI_TX0P	HDMI0_TX0_P
DSI1_D1_P	MIPI_D1_P	183	184	HDMI_TX0N	HDMI0_TX0_N
GND	GND	185	186	GND	GND
DSI1_C_N	MIPI_CLK_N	187	188	HDMI_TXCP	HDMI0_CLK_P
DSI1_C_P	MIPI_CLK_P	189	190	HDMI_TXCN	HDMI0_CLK_N
GND	GND	191	192	GND	GND
DSI1_D2_N	MIPI_D2_N	193	194	MIPI_D3_N	DSI1_D3_N
DSI1_D2_P	MIPI_D2_P	195	196	MIPI_D3_P	DSI1_D3_P
GND	GND	197	198	GND	GND
HDMI0_SDA_5V	HDMI_SDA	199	200	HDMI_SCL	HDMI0_SCL_5V

All ground pins should be connected. Attention should be paid to mechanical stability when designing expansion boards.

Strict attention should be paid to the IO level to avoid damage to the chip. and do not input reverse voltage.

Chapter 5. Power

5.1 Power up sequencing

The BPI-CM4 requires a single +5V supply, and it is not recommended to use the +3.3V and +1.8V output of the core board to power peripheral devices.

All pins should not have any power applied to them before the +5V rail is applied.

+5V should rise monotonically to 4.75V and stay above 4.75V for the entire operation of the BPI-CM4.

System operation begins when both +5V rails are above 4.75V and CPU_RST is high. CPU_RST has an internal RC delay on the core board to make it rise after +5V rises. The order of events is as follows

1. +5V rises
2. CPU_RST rises
3. +1.8V rises
4. +3.3V rises

5.2 Power down sequencing

The Operating System should be shut down to ensure that the file system remains consistent, before the power is removed. If this can't be achieved, then a filesystem like btrfs, f2fs or overlayfs should be considered.

Once the Operating System has shutdown the +5V rail can be removed.

During the shutdown sequence the +3.3v will be discharged before the +1.8v rail.

Appendix A: Official Support

- Official wiki Getting Started: [Getting Started with CM4](#)
- Official wiki Products: [BPI-CM4 Computer module and development Kit](#)
- Official Forum (EN): [BPI-CM4 Forum\(EN\)](#)
- Official Forum (CN): [BPI-CM4 Forum\(CN\)](#)



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Banana Pi open source hardware community

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