

**ROCHESTER INSTITUTE OF TECHNOLOGY
MICROELECTRONIC ENGINEERING**

BJT IC Design

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3-5-2021 BJT_IC_Design.pptx



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OUTLINE

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Differential Amplifier
Biasing, Current Sources, Mirrors
Output Stages
Operational Amplifiers
References
Homework Questions



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INTRODUCTION

This document introduces analog integrated circuit (IC) design. The big difference for integrated circuits is that large value resistors and capacitors require lots of space on a microchip. The microchip can be smaller (reducing cost and increasing profit) if a capacitor can be avoided by using several transistors instead. In some cases the capacitors are required and are almost always provided external to the microchip as a component on the circuit board. In the capacitor coupled BJT multistage amplifier large value capacitors are used between each stage (and for emitter bypass) to separate the DC voltages. In the analog IC the differential amplifier rejects the DC voltages between cascaded stages and level shifting is also used between amplifier stages. Thus we will start with the presentation of the differential amplifier. It gives the same gain as the common emitter amplifier (or common source if MOSFETs are used) but can be cascaded without capacitors between amplifier stages.



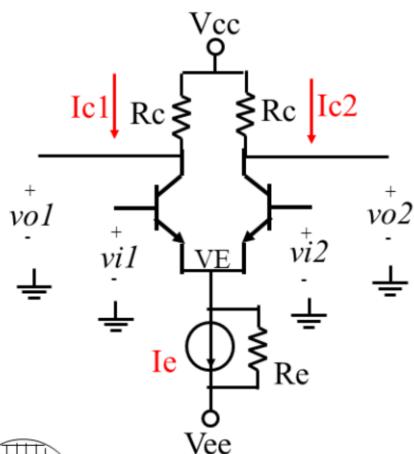
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Please read.

THE DIFFERENTIAL AMPLIFIER



DC Analysis – assume:
Identical transistors,
 $Re=\infty$, $v_{in1}=v_{in2}=0$

Then
 $I_{c1}=I_{c2}=I_e/2$
 $V_{o1}=V_{o2}=V_{cc}-R_c I_e/2$

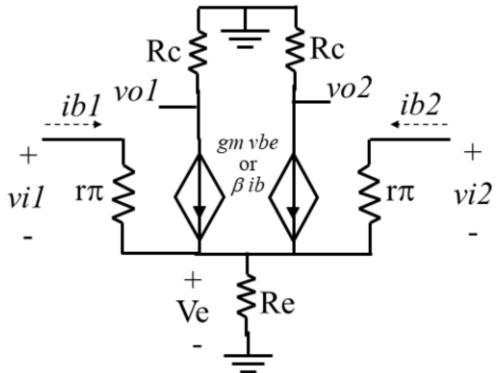
Example: If $I_e = 6\text{mA}$
 $V_{cc} = 10$, $V_{ee} = -10$ and
 $R_c = 2\text{k}\Omega$
Assume $V_{in1} = V_{in2} = 0$
 $V_{o1} = V_{o2} = 4.0 \text{ volts}$
 $V_E = -0.7$
 $V_{CE} = 4.7$

This is a basic differential amplifier (with BJT's... could also use MOSFETs). This circuit will amplify the difference signal between Vin 1 and Vin 2. It will reject (not amplify) signals that are common to Vin1 and Vin2. For example if Vin 1 is a small amplitude sinusoid on a DC component of 2 volts and Vin 2 is no sinusoid but also has a DC value of 2 volts, the sinusoid will be amplified and the 2 volts will be rejected (treated as zero volts DC into the amplifier). There are two inputs and two outputs. Vin 1 and Vout 1 have a phase inversion, Vin 1 and Vout 2 are non-inverting. Similar for Vin 2, Vout 2 (inverting) and Vout 1 (non-inverting).

The DC analysis is shown in the slide above. The DC current I_e splits equally to such that $I_{c1}=I_{c2}=I_e/2$. Ohms law gives V_{o1} and $V_{o2} = V_{cc}-R_c I_e/2$

Go through the DC analysis example shown.

SMALL SIGNAL ANALYSIS



Lets define:

Differential input voltage

$$vid = vi_1 - vi_2$$

Common input voltage

$$vic = (vi_1 + vi_2)/2$$

Differential Output Voltage

$$Vod = Vo_1 - Vo_2$$

Common output voltage

$$Voc = (Vo_1 + Vo_2)/2$$

Single sided output voltage

$$Voss = Vo_1 \text{ or } Vo_2$$



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Once the DC analysis is completed we can find gm , $r\pi$ and r_o for each transistor. Then we draw the ac equivalent circuit by replacing capacitors and voltage sources with a “short”, and current sources with an “open”.

Then do circuit analysis to find gains, input resistance and output resistance. Since we have more than one input and output and we have differential signals and common mode signals we have several different gains that we could compute. Five different voltage gains are defined in the figure above. We will derive the results for all of these in the next few pages.

VOLTAGE GAINS: Avd, Avc, CMRR

Differential mode voltage gain, $\text{Avd} = V_{od} / v_{id}$

$$\text{Let } v_{in1} = v_{id}/2 + v_{ic}^0 \text{ and } v_{in2} = -v_{id}/2 + v_{ic}^0 \quad \text{eq. 1.}$$

$$i_{b1} = (v_{in1} - V_e) / r\pi \text{ also } i_{b2} = (v_{in2} - V_e) / r\pi$$

$$i_{b1} = (v_{id}/2 - V_e) / r\pi \quad i_{b2} = (-v_{id}/2 - V_e) / r\pi$$

$$V_{o1} = -\beta i_{b1} R_C \text{ also } V_{o2} = -\beta i_{b2} R_C$$

$$V_{od} = V_{o1} - V_{o2} = -\beta i_{b1} R_C - -\beta i_{b2} R_C$$

$$V_{od} = (\beta R_C / r\pi) (v_{id}/2 + v_{id}/2)$$

$$\boxed{\text{Avd} = -\frac{\beta R_C}{r\pi} = -\text{gm} R_C}$$

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The first gain we will derive is the Differential Mode Voltage Gain, Avd. It is the differential mode output voltage $V_{od} = (V_{o1} - V_{o2})$ divided by the differential mode input voltage, $V_{id} = v_{i1} - v_{i2}$. For pure differential input we make the common mode input voltages $v_{ic} = \text{zero}$, eq.1.

If you follow the algebra you get to the results shown in the box at the bottom of the page. You might recognize the results as identical to a BJT common emitter amplifier with on load resistor and no source resistor.

VOLTAGE GAINS: Avd, Avc, CMRR

$$\text{Common Mode Voltage Gain } Avc = \frac{V_{oc}}{V_{ic}} = \frac{(V_{o1} + V_{o2})/2}{(v_{in1} + v_{in2})/2}$$

Let $V_{id} = 0$ thus $v_{in1} = v_{in2} = V_{ic}$ eq.1.

$$V_e = 2 \operatorname{Re}(\beta + 1) i_b$$

$$i_b = (V_{ic} - V_e) / r\pi$$

$$i_b = \frac{V_{ic} - 2 \operatorname{Re}(\beta + 1) i_b}{r\pi} \text{ Rearranging; } i_b = \frac{V_{ic}}{2 \operatorname{Re}(\beta + 1) + r\pi}$$

$$V_{oc} = \frac{-\beta i_b R_c + -\beta i_b R_c}{2} \text{ and } i_b = i_b$$

$$\text{Thus } V_{oc} = -\beta R_c i_b = \frac{-\beta R_c V_{ic}}{2 \operatorname{Re}(\beta + 1) + r\pi}$$

$$Avc = \frac{V_{oc}}{V_{ic}} = \frac{-\beta R_c}{2 \operatorname{Re}(\beta + 1) + r\pi}$$



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Next we find the common mode gain, Avc as defined in the box at the top of the page. We make the differential inputs $v_{id} = 0$ to have pure common mode input voltages, eq. 1. Looking at the ac equivalent circuit we see that the i_b currents from the input on the left and from the input on the right they which become $(\beta + 1)$ times bigger when they exit at the emitter of each transistor. They then combine and flow through R_e creating voltage drop $V_e = 2 \operatorname{Re}(\beta + 1) i_b$. The algebra that follows gives the result shown in the box at the bottom of the slide. If β is large the $r\pi$ in the denominator can be neglected. (and $\beta \sim = \beta + 1$ and they cancel each other giving a common mode gain of $\sim R_c / 2 \operatorname{Re}$ and R_e is the current source parallel resistance that is large, resulting in a small common mode gain, probably less than 1 V/V).

OTHER RESULTS

Single Sided Output Differential Voltage Gain:

$$\frac{V_{oss}}{V_{id}} = \frac{1}{2} - \frac{\beta R_c}{r\pi}$$

note: half

Single Sided Output Common Mode Voltage Gain:

$$\frac{V_{oss}}{V_{ic}} = \frac{-\beta R_c}{2R_e(\beta+1) + r\pi}$$

note: same

Common Mode Rejection Ratio: CMRR is a figure of merit used to compare differential amplifiers

$$CMRR = \frac{A_{vd}}{A_{vc}}$$

Differential Mode Input Resistance:

$$R_{id} = 2r\pi$$

Common Mode Input Resistance:

$$R_{ic} = r\pi + (\beta+1)2R_e$$



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This slide shows (but does not derive) other results of interest. The single sided gains are important because it is common to have single output in operational amplifiers for example. The single sided differential voltage gain is just $\frac{1}{2}$ of the differential output gain calculated two pages above. The single sided differential output can be inverting or non inverting depending on which of the two outputs is used. Note: the common mode gain is the same for differential output or single sided output.

CMRR is often expressed in $dB = 20\log_{10}(A_{vd}/A_{vc})$

VARIATIONS

Variations:

1. Resistor between emitter and –Vee rather than current source
2. Series base resistors
3. Emitter resistors
4. Various types of current sources
5. Darlington configuration
6. FET's
7. Single sided outputs
8. Active loads
9. unbalanced or non symmetrical circuits



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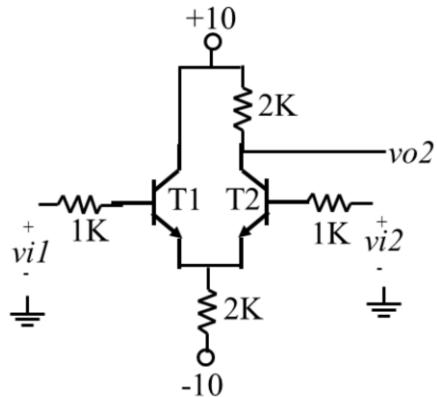
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These are some of the variations you will see in different designs. The approach is the same. DC analysis, AC equivalent circuit, AC analysis for the desired gain or resistance.

EXAMPLE DIFFERENTIAL AMPLIFIER

Analyze the following differential amplifier, $\beta=200$



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This is a differential amplifier example with a different schematic.

The approach is the same. DC analysis, AC equivalent circuit, AC analysis for the desired gain or resistance.

SOLUTION TO EXAMPLE ON PREVIOUS PAGE

DC Analysis:

Small Signal Analysis:

Hand Calculation: (for this circuit)

$$Avd = \frac{1}{2} gm R_c r_{pi} / (1K + r_{pi}) = 62$$

or

$$Avd = \frac{1}{2} \beta R_c / (r_{pi} + 1K) = 62$$



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Try to do this example. If you get stuck the solution is shown at the end of this document.

SUMMARY

1. The differential amplifier should amplify the difference between the two input voltages.
2. The differential amplifier should suppress signals that are common to both inputs.
3. The differential amplifier with a constant current source is superior to the differential amplifier with just a resistor.
4. The common mode rejection ratio is used as a figure of merit for comparison.
5. The differential amplifier is a dc amplifier as well as an ac amplifier. (no capacitors)



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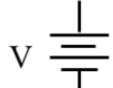
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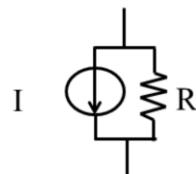
Please read. Now you know everything about differential amplifiers....
Just kidding but you have a start...

CURRENT SOURCE OR SINK

Current sources can provide constant DC current and are open circuits in the AC equivalent circuits. (similar to voltage sources providing constant DC voltages and are short circuits in AC equivalent circuits.) Voltage sources have a small series resistance that represents the internal resistance (often neglected, zero). Current sources have a large parallel resistance the represents the internal resistance. The term **source or sink** is sometimes used to represent the direction of current flow (not always).



DC Voltage Source



DC Current Source



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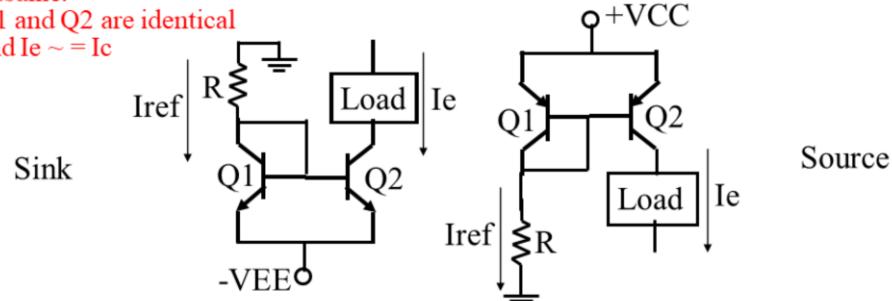
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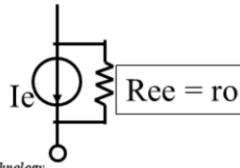
Please read. I am pretty sure you already know this but I just wanted to write it down.

SIMPLE CURRENT SOURCE/SINK/MIRROR

Assume:

Q1 and Q2 are identical
and $I_e \sim = I_c$  I_e for Q1

$$I_{ref} = I_e = (V_{EE} - 0.7)/R$$

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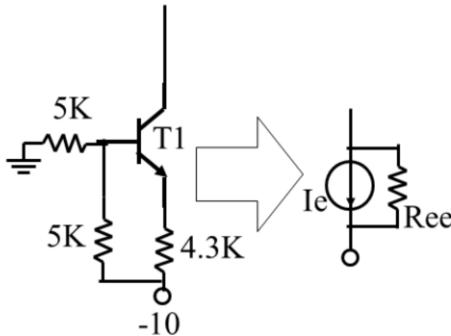
The voltage V_{be} for Q1 is equal to the voltage V_{be} for Q2 thus the emitter currents I_e are the same.

These are current sources or sinks using BJTs (could use MOSFETs). A reference current is set by R and the supply voltage. The current source I_e is equal to I_{ref} because V_{be} of Q1 and Q2 are equal.

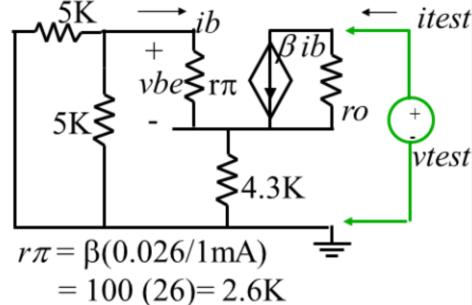
The R_{ee} for these current source/sink is the small signal output resistance in parallel with the current source and is equal to r_o for the simple current source/sink shown.

CURRENT SOURCE (HW Problem 1)

There are many types of current sources. Consider the following:



What is I_e ? (Ans: $\sim 1\text{mA}$)



$R_{\text{ee}} = \infty$ if $r_o = \infty$ (not useful)

R_{ee} is calculated by students in pro.1.

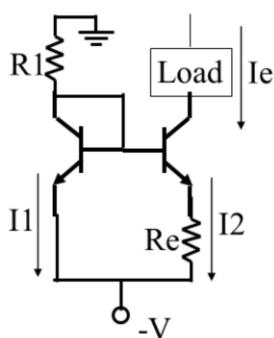
R_{ee} in this example is 4.68 Meg

if $\beta = 100$ and $r_o = 100\text{K}$



The value of R_{ee} is the current source small signal output resistance calculated from the ac equivalent circuit. Like finding R_{Th} for a network with a dependent source. We apply an imaginary voltage v_{test} and find i_{test} . R_{th} is $V_{\text{test}}/i_{\text{test}} = R_{\text{ee}}$

You will be asked to do this for one of your homework assignments.

LOW CURRENT CURRENT SOURCE

Recall:

$$I_E = I_{SE} e^{V_{BE}/V_T} \quad \text{and} \quad V_T = Kt/q$$

$$V_{BE1} = V_{BE2} + I_2 R_E$$

$$Kt/q \ln I_1/I_S = Kt/q \ln I_2/I_S + I_2 R_E$$

$$Kt/q \ln(I_1/I_2) = I_2 R_E$$

note: I_2 is always smaller than I_1
 I_e can be small without R_1 being large.
 R_E is \sim Meg ohms



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The R_E in this current source is good because it makes R_E large (MEG ohms). The current will be lower than the reference current which is often desired.

We just have to solve the equation shown in the box to design or analyze this type of current source.

LOW CURRENT CURRENT SOURCE**Example 1: suppose I1 = 1 mA and I2 is 10 uA find Re**

$$KT/q \ln(I1/I2) = I2Re$$

$$0.026 \ln(1mA/10uA) = 10uA Re$$

$$0.1197 = 10uA Re$$

$$Re = 11.97K$$

Example 2: suppose I1 = 1 mA and Re = 20K find I2

$$KT/q \ln(I1/I2) = I2Re$$

$$0.026 \frac{\ln(1mA/I2)}{I2} = 20K$$

Try I2 =	Left Side =
1uA	179K
5uA	27.6K
6uA	22.2K
7uA	18.4K
Etc.	



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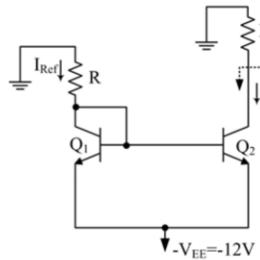
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Two different examples. In the first example you know the reference current I1 and you want to calculate Re to provide a smaller current, you also know I2. That is straight forward algebra. In the second example you know Re and the reference current I1 and want to find I2. That is more difficult because I2 is in the argument for ln and on the right side of the equation. I use trial and error trying to make both sides of the equation equal. You do know that I2 is less than the reference current I1.

MORE CURRENT SOURCES

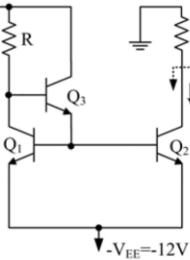
$$I_o = I_{ref} / (1+2/\beta)$$



(a)

Ree = ro

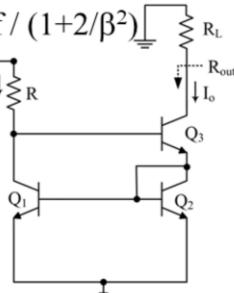
$$I_o = I_{ref} / (1+2/\beta^2)$$



(b)

Ree = ro

$$I_o = I_{ref} / (1+2/\beta^2)$$



(c)

Ree = MEG ohms

(a) Basic, (b) Current-buffered, and (c) Wilson current sources.

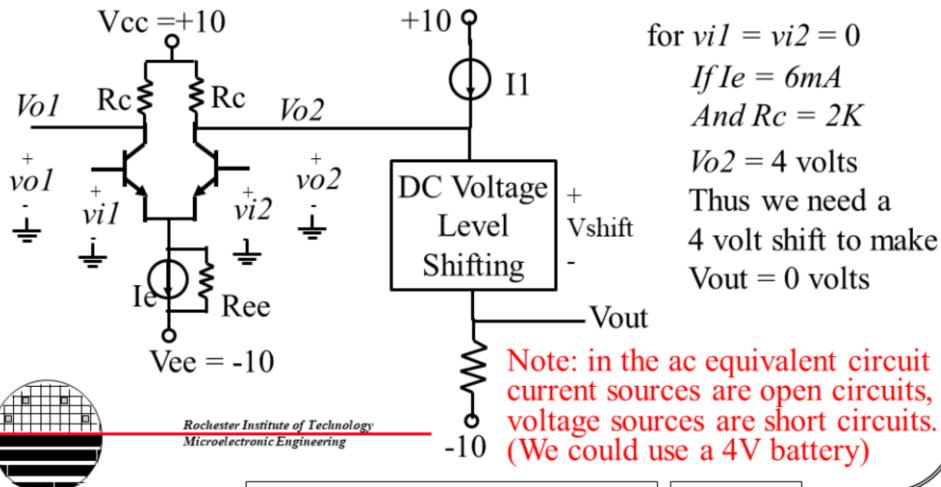


In all these circuits the current in Q2 is equal to the Current in Q1.
Ree is large for the Wilson current source. Ree = ro for others

Here are some other current sources/sinks where we pay attention to the base current (don't assume it is small compared to the emitter current). The current buffered is less sensitive to changes in Beta especially low values of Beta. The Wilson current source is current buffered but also has a Ree higher than ro. (could be MEG ohms, see page 15)

LEVEL SHIFTING

It would be nice to have DC zero volts out when we have zero volts in. We can achieve this by adding a level shifting stage.



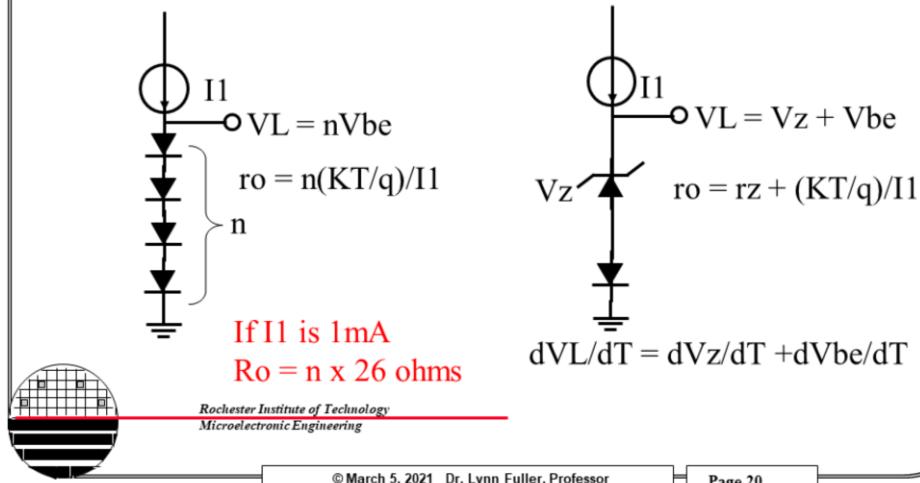
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Level shifting stages are used to make v_{out} zero when $v_{in1}=v_{in2}$ is zero. The level shifting can also have high input impedance to not disturb the symmetry of the differential amplifier. It might have voltage gain of one or some realizations have voltage gain as well as level shifting. We will look at several different level shifting configurations.

VOLTAGE SOURCES / REFERENCES

Voltage sources should have constant voltage and zero source resistance.

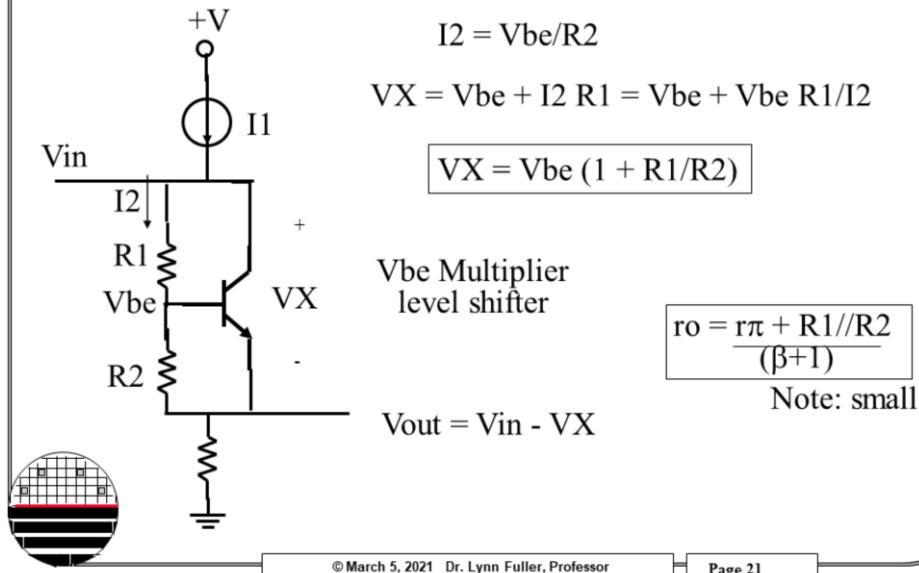


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The level shifting stage is like putting a DC voltage source in the signal path. That would give a constant DC voltage shift and in the ac equivalent circuit it would look like a short. So a current source in series with a resistor will give a DC shift but in the ac equivalent circuit the Resistor remains in the signal path. A string of diodes give a DC voltage of ~0.7 for each diode. In the ac equivalent circuit the diode is replaced by $(KT/q)/I_1$ for each diode. A zener diode may have a lower ac equivalent resistance, r_z . (it is 1/slope in the breakdown region)

LEVEL SHIFTING

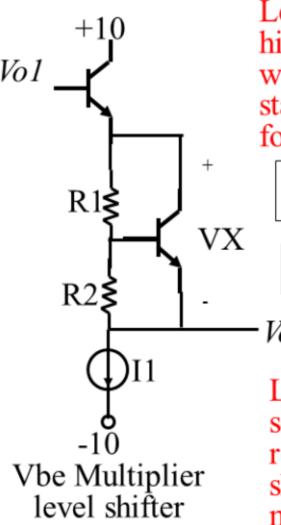
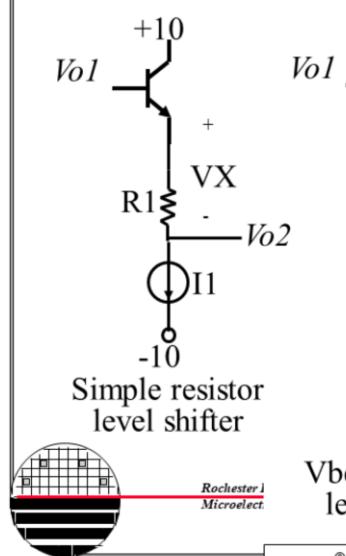


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This circuit gives level shifting of V_X which is set with R_1 and R_2 as shown in the box. The small signal ac resistance is r_o which can be small as desired.

LEVEL SHIFTING – WITH HIGH INPUT RESISTANCE



Level shifting should have high input resistance, R_{in} , so it will not “load” the previous stage. Common collector input for high input resistance.

$$R_{in} = (r_\pi + r_o + (\beta+1)R_L)$$

$$VX = V_{be} \left(1 + \frac{R_1}{R_2} \right)$$

Level shifting should have low series resistance. The series resistance in the simple level shifter is $\sim R_1$, $r_o/(\beta+1)$ in Vbe multiplier circuit.

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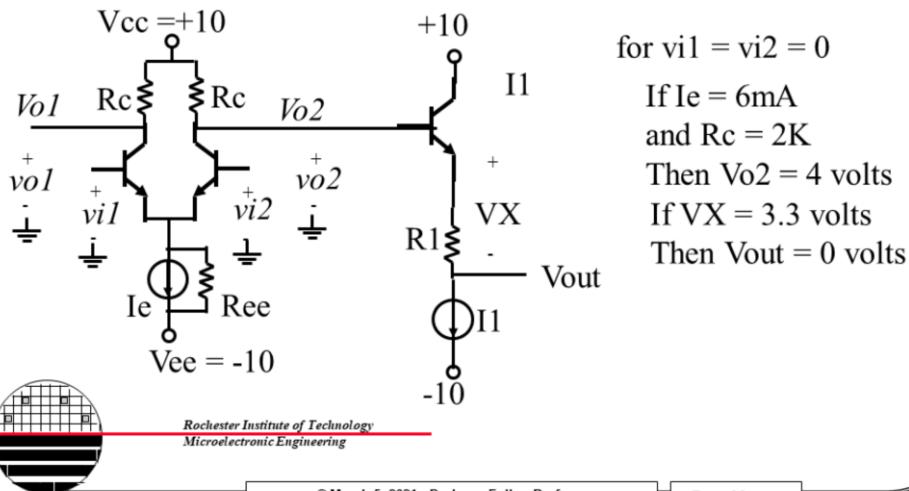
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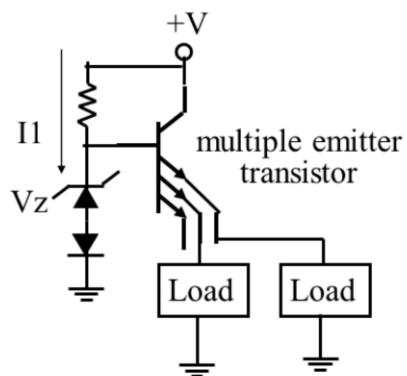
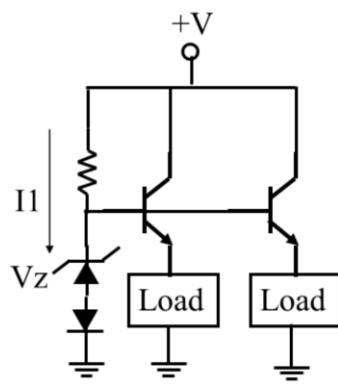
V_o2 goes to the output stage but I don't know what R_L is exactly. However R_{in} could be high. The DC level shift is $0.7 + VX$ and VX is shown in the box on the slide.

In lab we use a common emitter stage with emitter feedback which also has high input resistance and also small signal voltage gain of ~ 10 V/V.

LEVEL SHIFTING WITH HIGH INPUT RESISTANCE

It would be nice to have zero volts out when we have zero volts in. We can achieve this by adding a level shifting stage.



VOLTAGE MIRROR

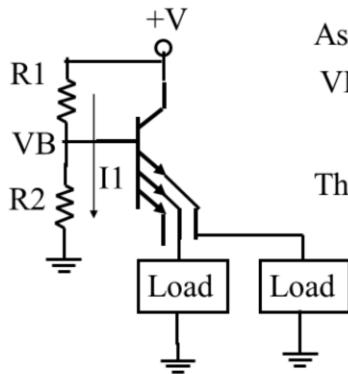
Assume IB is small compared to $I1$
The voltages across all loads are equal to Vz

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Some circuits use identical reference voltages and can use multiple emitter transistors.

VOLTAGE MIRROR

Assume I_b is small compared to I_1

$$VL = VB - 0.7$$

$$VB = V \left(\frac{R_2}{R_1 + R_2} \right)$$

$$\text{Therefore: } VL = V \left(\frac{R_2}{R_1 + R_2} \right) - 0.7$$

$$r_o = \frac{r_\pi + R_1 / R_2}{(\beta + 1)}$$

Note: small

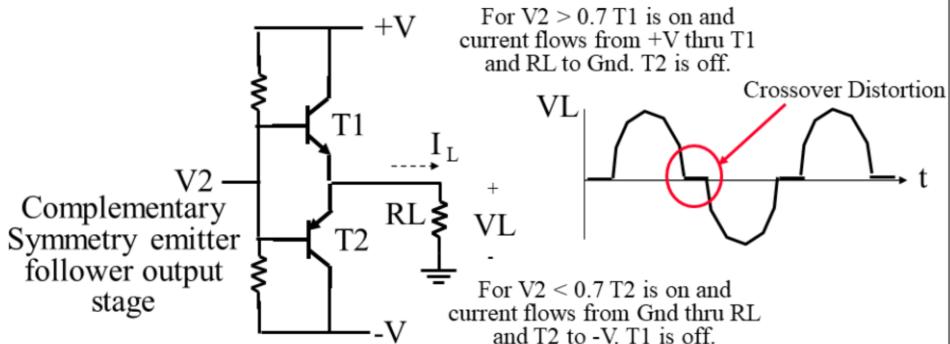
The voltages across all loads are equal to VL



Voltages other than the zener voltage shown on the previous page can be created with this circuit.

OUTPUT STAGES

An output stage is needed to provide the capability of sourcing or sinking “large” currents to the load

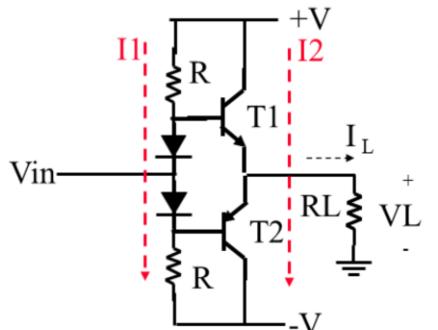


With no signal in the transistors T1 and T2 are biased in an off state. This is called a class B amplifier.

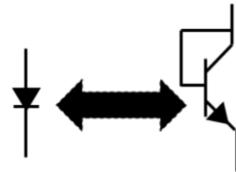
The output stage is common collector, so voltage gain of approximately one. However it can provide large current to the load, RL . $V2$ should be close to zero volts when there is no signal if the level shifting stage is working correctly. When a signal makes $V2$ increase more than 0.7 volts the transistor T1 turns on and allows current to flow from +V through RL to ground. When a signal makes $V2$ go negative more than 0.7 volts, T2 is turned on and allows current to flow from ground through RL to the -V supply. No current flows when $V2$ is between -0.7 and +0.7 thus the output wave form has crossover distortion as shown. The amount of current that flows depends on the value of RL . If RL was zero (wiring error) the current would be infinite (for a short time until the transistor burns up).

OUTPUT STAGES

To eliminate the crossover distortion we can bias the transistors T1 and T2 so that they are just ready to conduct (ie $V_{be} \sim 0.65$)



Note: D1 and D2 are probably transistors identical to T1 and T2 with Base and Collector shorted. Thus $I_1 = I_2$ and is called the idle current. $I_1 = (2 V - 1.4)/2R$



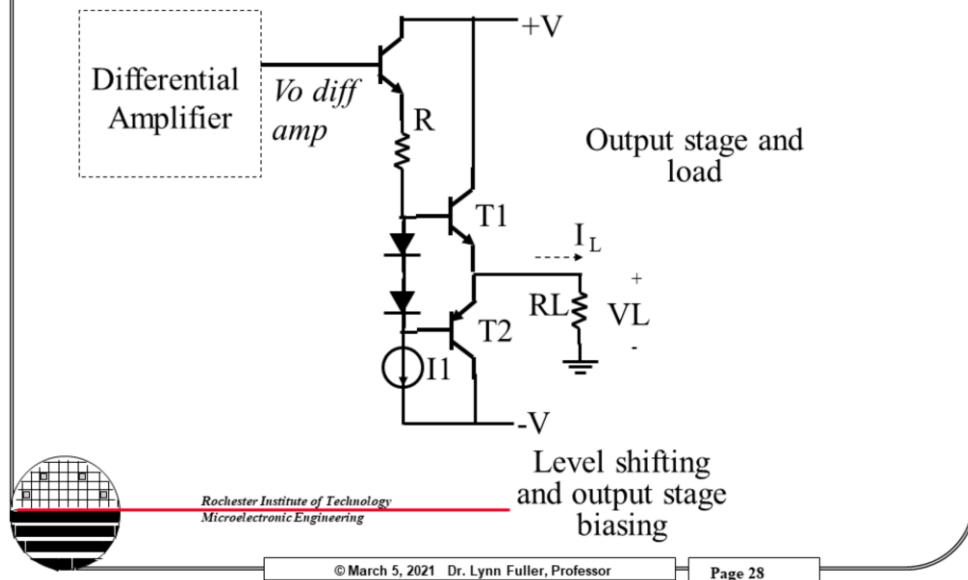
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To eliminate the crossover distortion we can bias the transistors T1 and T2 so that they are just ready to conduct (ie $V_{be} \sim 0.65$). A good way to do that is to insert a couple of diodes or transistors with base connected to collector to give a small idle current so that the voltage on the base of the transistors T1 and T2 are ± 0.65 Volts.... Just ready to conduct. The idle current depends on R or can be set other ways such as with a current source.

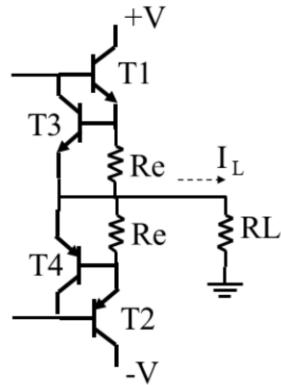
OUTPUT STAGES



This circuit shows a common collector (high R_{in} , gain of 1 V/V) level shifting stage with crossover distortion elimination (using two diodes) and Idle current set by I_1 . I_1 times R sets the level shifting voltage needed to make V_L equal to zero when the input signal to the differential amplifier (not shown) is zero. The DC value of $V_{o\ diff\ amp}$ is found from the DC analysis of the differential amplifier.

OUTPUT STAGE WITH CURRENT LIMITING

When T1 is on IL flows from +V thru T1, Re and RL to Gnd. If RL accidentally went to zero IL would only go to $0.7/Re$ because at that value of IL T3 would turn on which would remove the base drive from T1 thus IL would be limited to $0.7/Re$. Similar for T2.



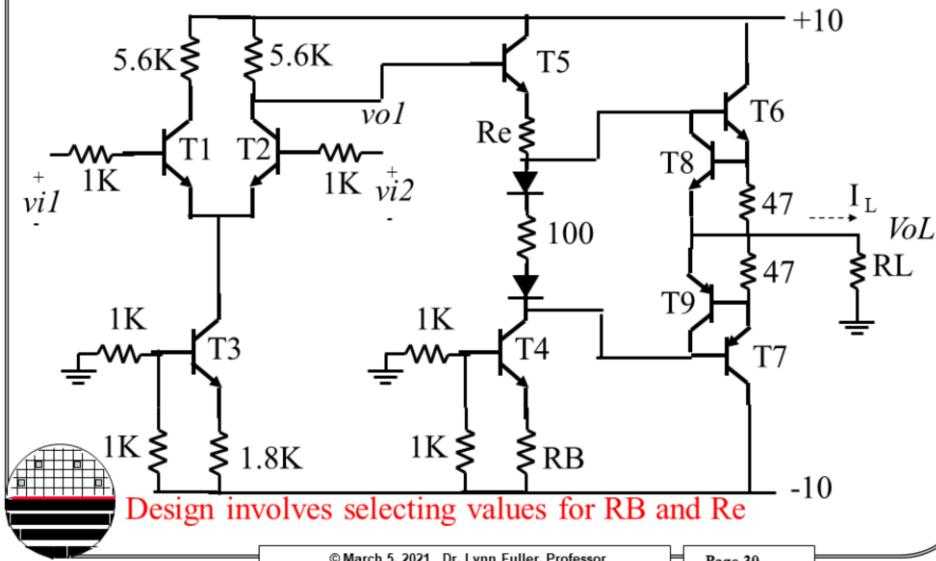
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Most op amps will have current limiting of some type to prevent burn out if the output terminal is wired to ground by mistake. The resistors Re and T3 and T4 limit the current. I max is $0.7/Re$.

SIMPLE OPERATIONAL AMPLIFIER

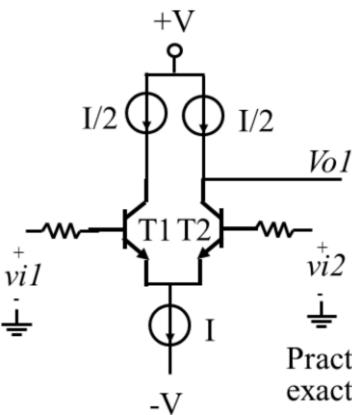


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This is a schematic of a direct coupled (no coupling capacitors) amplifier with three stages. The differential amplifier with current source. The common collector level shifting, crossover elimination and its current source, and common collector output stage with current limiting. The overall voltage gain is approximately the product of the single sided differential amplifier, the common collector level shifting stage (gain ~1) and common collector output stage (gain ~1) there might be some voltage division from the Rout and Rin between stages, and between Rs and Rin of the diff amp and between Rout and RL at the output that would reduce the overall gain some. However the 2nd and 3rd stages are common collector so Rin should be large and Rout small. So it is correct to neglect the voltage division. To get the approximate gain but expect the gain to be lower.

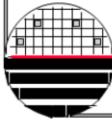
ACTIVE LOADS



Replacing some of the resistors with current sources requires less space and enables higher differential voltage gain and lower common mode gain because r_o replaces RC in the collector.

$$r_o = V_A/I_C \text{ and can be even higher}$$

Practically: $I/2$ sources can not be made exactly correct. (see next page)



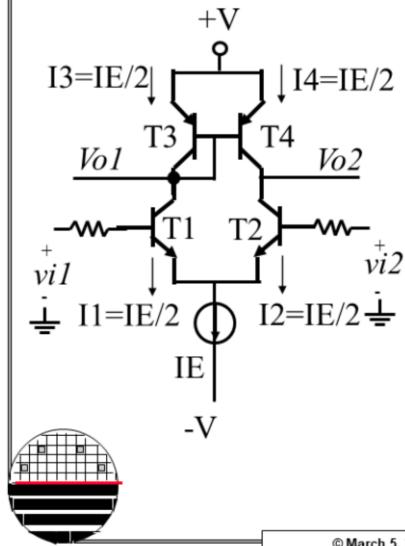
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We get much higher gain when we use active loads instead of resistors in the differential amplifier. Active loads are current sources or mirrors instead of resistors. We can set the desired DC operating point and in AC equivalent circuit the current sources are open leaving the r_{ee} of the current source which can be large. Since the single sided voltage gain is $\frac{1}{2} g_m R_C$ and R_C now becomes r_{ee} of the active load we can achieve voltage gains of 1,000 V/V instead of 100's V/V. The next five pages we do hand calculations for a differential amplifier with active loads.

ACTIVE LOADS – CURRENT MIRROR



DC Analysis:

1. IE is constant current.
2. $I_3 = I_4 = IE/2$
3. $V_{o1} = V - 0.7$
actually $V_{o1} = V - KT/q \ln(I_3/IS)$
4. $V_{o2} = V - V_{EB3} - V_{BC4}$
 $V_{o2} = V - KT/q \ln(I_3/IS) - V_{BC4}$

When $V_{in1} = V_{in2} = \text{zero}$ and $I_3 = I_4 = IE/2$
we have everything balanced and
 $V_{BC3} = V_{BC4} = 0$ thus $V_{o2} = V - 0.7$
equal to V_{o1}

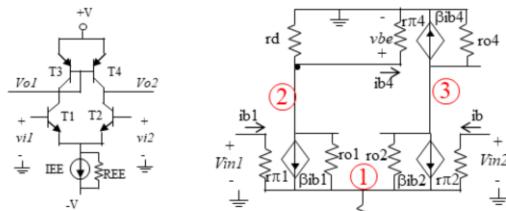
5. When $V_{in1} > V_{in2}$ then $I_1 > I_2$ and
 V_{o2} rises toward $+V$
Note: p-p signal swing is about 1 volt

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As always we start with the DC analysis to determine the transistor collector currents. Once we know IC we find gm, r_π and r_o for each transistor. The peak to peak signal swing is only 1 volt, however we only want to take microvolt signals and amplify them by 1000 to get millivolt signals.

SMALL SIGNAL ANALYSIS OF DIFF AMP WITH ACTIVE LOAD



Let V_1, V_2 and V_3 be node voltages
at node 1,2 and 3, summing currents KCL

at node1

$$(\beta+1)(V_{in1}-V_1)/r_{\pi 1} + (V_2-V_1)/r_{o1} + (V_3-V_1)/r_{o2} + (\beta+1)(V_{in2}-V_1)/r_{\pi 2} - V_1/REE = 0$$

at node2

$$V_2/r_d + V_2/r_{\pi 4} + (V_2-V_1)/r_{o1} + \beta(V_{in1}-V_1)/r_{\pi 1} = 0$$

at node3

$$\beta V_2/r_{\pi 4} + V_3/r_{o4} + (V_3-V_1)/r_{o2} + \beta(V_{in2}-V_1)/r_{\pi 2} = 0$$



This figure shows the ac equivalent circuit for the differential amplifier. I choose nodal analysis to find the node voltages at node 1, 2 and 3. The equations at each node come from Kirchhoff's current law, KCL, at node 1, 2 and 3.

I expect you to know how to do this from your Circuits I class.

SMALL SIGNAL ANALYSIS OF DIFF AMP WITH ACTIVE LOAD

Rearranging:

$$\text{at 1} \quad \underbrace{[-1/\text{RE}\text{E}-(\beta+1)/\text{r}\pi 1-1/\text{r}\text{o}1-1/\text{r}\text{o}2-(\beta+1)/\text{r}\pi 2]\text{V}1}_{\text{a1}} + [1/\text{r}\text{o}1]\text{V}2 + [1/\text{r}\text{o}2]\text{V}3 = \text{RHS}$$

$\text{RHS} = -\text{V}\text{i}\text{n}2(\beta+1)/\text{r}\pi 2 - \text{V}\text{i}\text{n}1(\beta+1)/\text{r}\pi 1$

$$\text{at 2} \quad \underbrace{[-1/\text{r}\text{o}1-\beta/\text{r}\pi 1]\text{V}1}_{\text{a2}} + \underbrace{[1/\text{r}\text{d}+1/\text{r}\pi 4+1/\text{r}\text{o}1]\text{V}2}_{\text{a3}} + 0 \text{ V}3 = -\beta \text{V}\text{i}\text{n}1/\text{r}\pi 1$$

$$\text{at 3} \quad \underbrace{[-\beta/\text{r}\pi 2-1/\text{r}\text{o}2]\text{V}1}_{\text{a4}} + \underbrace{\beta/\text{r}\pi 4\text{V}2}_{\text{a5}} + \underbrace{[1/\text{r}\text{o}4+1/\text{r}\text{o}2]\text{V}3}_{\text{a5}} = -\beta \text{V}\text{i}\text{n}2/\text{r}\pi 2$$



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SMALL SIGNAL ANALYSIS OF DIFF AMP WITH ACTIVE LOAD

Using Cramer's rule and determinants

$$V_3 = \frac{\begin{vmatrix} a_1 & 1/r_{o1} & [-V_{in2}(\beta+1)/r_{\pi2} - V_{in1}(\beta+1)/r_{\pi1}] \\ a_2 & a_3 & -\beta V_{in1}/r_{\pi1} \\ a_4 & \beta/r_{\pi4} & -\beta V_{in2}/r_{\pi2} \end{vmatrix}}{\begin{vmatrix} a_1 & 1/r_{o1} & 1/r_{o3} \\ a_2 & a_3 & 0 \\ a_4 & \beta/r_{\pi4} & a_5 \end{vmatrix}}$$



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SMALL SIGNAL ANALYSIS OF DIFF AMP WITH ACTIVE LOAD

Example: let $r_{o1} = r_{o2} = r_{o4} = 50K$ $gm = \text{Beta}/r\pi$
 $r_{\pi 1} = r_{\pi 2} = r_{\pi 4} = 2K$
 $\beta = 100$, $r_d = 20$, REE = infinite

- a) If $V_{in1} = 1/2$ volt and $V_{in2} = -1/2$ volt

Find $V_3 = 1246$

Therefore $A_{vd} = 1246$

Simple Hand Calculation:

$$A_{vd} = \frac{1}{2} \text{Beta } R_c / r\pi = 1250$$

$$= \frac{1}{2} 100 \cdot 50K / 2K = 1250$$

or

$$A_{vd} = \frac{1}{2} gm R_c = 1250$$

- b) If $V_{in1} = 1$ volt and $V_{in2} = 1$ volt

Find $V_3 = 0.00005108$

Therefore $A_{vc} = 0.00005108$

$$c) CMMR = 1246 / 0.00005108 = 2.44e7$$



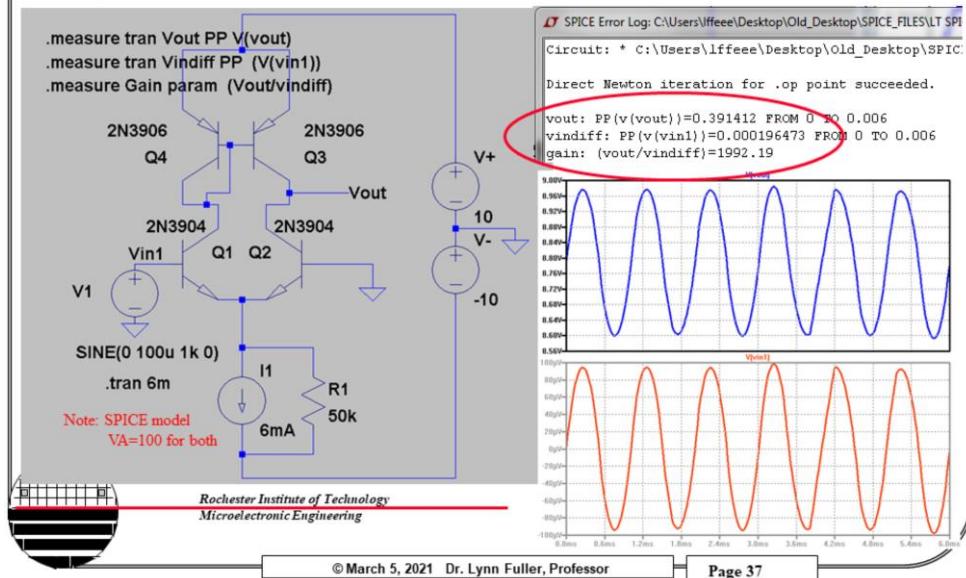
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For differential gain we let $V_{in1} = +1/2$ volt and $V_{in2} = -1/2$ volt. We calculate the voltage at node 3 (the output voltage) and divide by the differential input voltage of 1 volt to get the single sided differential voltage gain. The result from nodal analysis and from simple hand calculation equations, $\frac{1}{2} gm RC$ where RC is the r_o of the transistor T4 agree.

LTSPICE SIMULATION



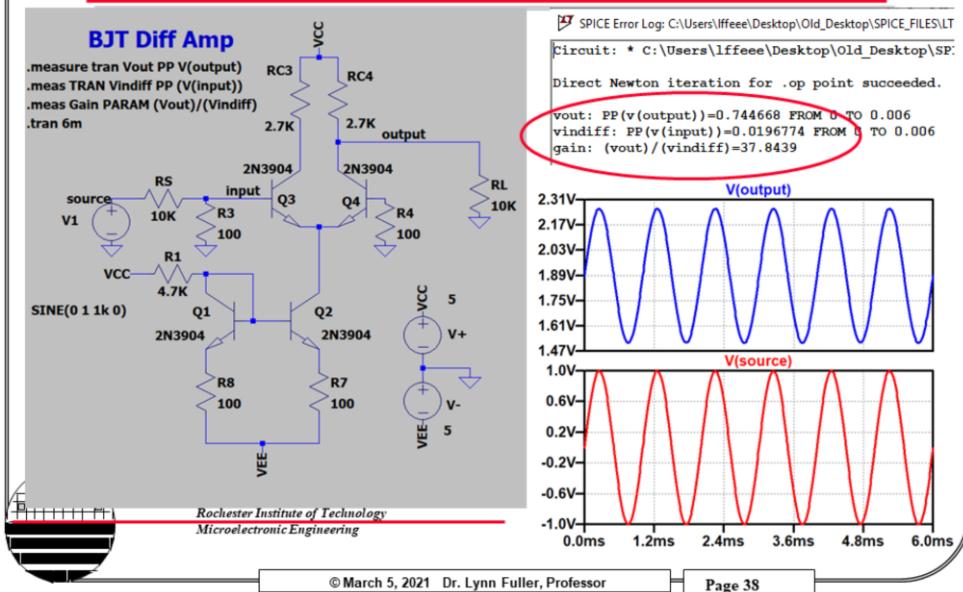
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SPICE analysis for the differential amplifier with active load gives a voltage gain of 1992 V/V.

In LTSPICE with the measurement commands shown on the schematic the input and output peak-to-peak values and gain are shown in the SPICE error log.

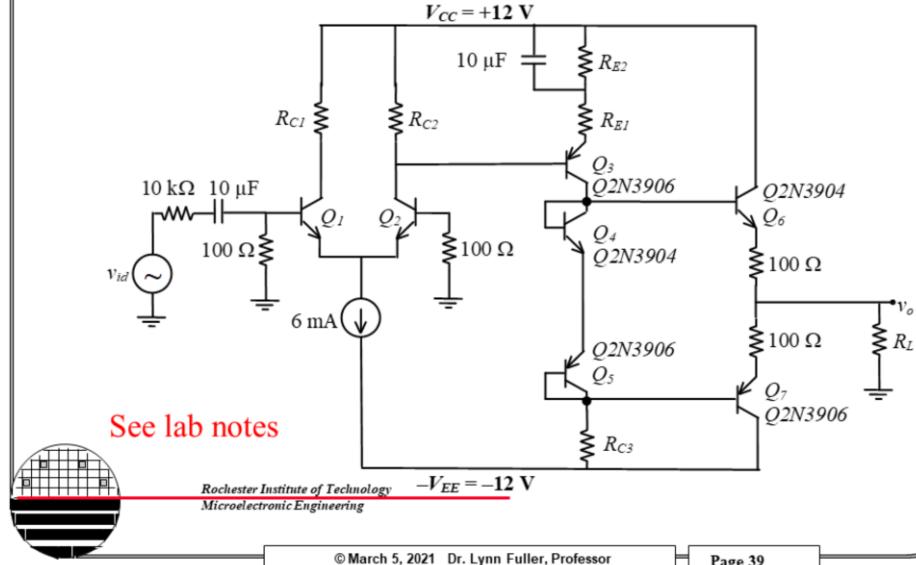
LTSPICE SIMULATION



SPICE analysis for the differential amplifier with active load gives a voltage gain of 1992 V/V but with resistors in the collector the gain is less than 100 V/V

In LTSPICE with the measurement commands shown on the schematic the input and output peak-to-peak values and gain are shown in the SPICE error log.

EXAMPLE FROM LAB



This is another example of a direct coupled BJT amplifier. It has three stages. The first stage is a differential amplifier with a voltage divider to make V_{in} 100 times smaller than the source V_S voltage. The differential amplifier has a single sided differential voltage gain of approximately 80 V/V. The second stage is a PNP common emitter stage with emitter feedback to reduce the gain of that stage to $\sim R_C3/R_E1$. The second stage also provides level shifting and crossover distortion elimination. The third stage is a common collector stage with 100 ohm resistors to limit the current in case the output is accidentally connected to ground. The overall total single sided differential voltage gain is the product of the gains for each of the three stages. $A_{vss} \text{ total} = v_{out}/v_{in} = 80 \times 10 \times 1 = \sim 800 \text{ V/V}$.

TWO TRANSISTOR DC COUPLED AMPLIFIERS

CC-CE

Common Collector – Common Emitter

CC-CC

Common Collector - Common Collector

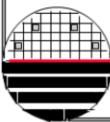
Darlington

CE-CB

Common Emitter – Common Base

or (Cascode)

There are other transistor configurations used instead of single transistor amplifiers. We will look briefly at these in the next few pages.

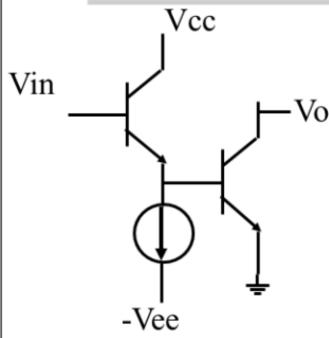


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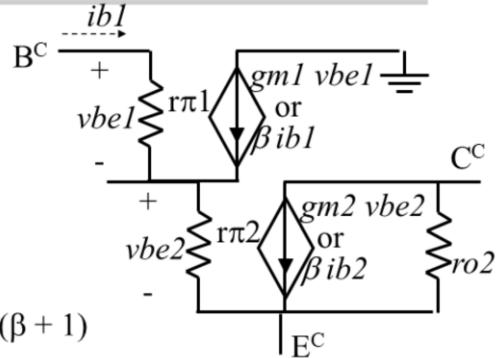
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CC-CE AND CC-CC CONFIGURATION



$$\beta^C = \beta (\beta + 1)$$



$$r\pi^C = \text{combined CC-CE input resistance} = r\pi l + (\beta + 1) r\pi 2$$

$$ro^C = ro2$$

$$gm^C = \left(\frac{gm2}{1 + \frac{r\pi l}{(\beta+1)r\pi 2}} \right)$$

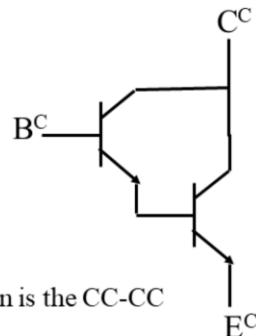
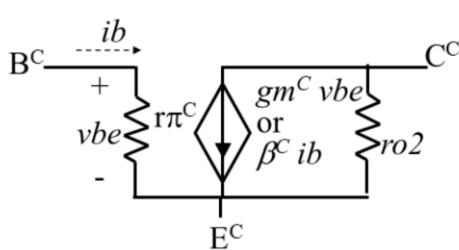


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The CC-CE connects two transistors as shown. The CC gives high input impedance and the direct coupled CE gives voltage gain. If this combination is used for the two input transistors in a differential amplifier we can expect higher input impedance and similar voltage gains as discussed in the first pages of this document.

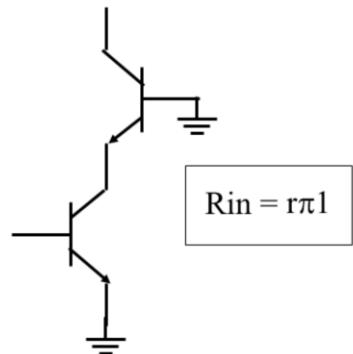
DARLINGTON CONFIGURATION



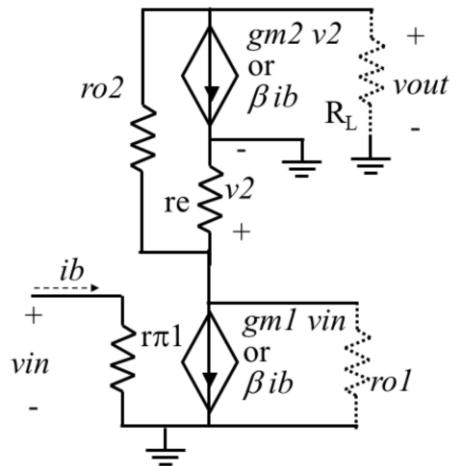
1. The darlington, when used in the CC configuration is the CC-CC configuration already discussed.
2. In the common emitter configuration the darlington is similar to the CC-CE configuration except that the collector of Q1 does not go to the supply, but rather it goes to the output. This reduces the output resistance and increases the input capacitance. Thus the CC-CE is preferred over the darlington.

The Darlington configuration gives high current gain of Beta times (Beta + 1).

CE-CB CASCODE CONFIGURATION



Note: r_o1 is in parallel with r_e so we can neglect r_o1



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The common emitter - common base configuration gives higher voltage gain, higher frequency operation, bandwidth, and higher output resistance, r_o .

CE-CB CASCODE CONFIGURATION

Note: if the load is a current source then R_L is infinite and $gm_2 v_2$ flows in r_o2 only.

$$\text{Thus } v_2 = (gm_1 V_{in} + gm_2 v_2) re$$

$$\text{So } (1 - gm_2 re) v_2 = gm_1 re V_{in} \text{ which gives us } v_2/V_{in}$$

$$\text{and } V_{out} = - gm_2 v_2 r_o2 - v_2 \\ \text{or } V_{out} = - (gm_2 r_o2 + 1) v_2 \quad \text{neglect}$$

$$Av = V_{out}/V_{in} = V_{out}/v_2 \times v_2/v_{in} = - (gm_2 r_o2 + 1) \frac{gm_1 re}{(1 - gm_2 re)}$$

$$\text{But } \alpha = I_c/I_e = gm_2 v_2 / (v_2/re) = gm_2 re$$

$$\text{And } \alpha / (1 - \alpha) = \beta$$

Thus

$$Av = gm_2 r_o2 \beta$$



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CE-CB CASCODE CONFIGURATION

R_o^c is found by “killing” the input source and calculating v_{test}/i_{test} applied to the output.

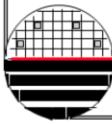
$$I_{test} = gm2 v2 - v2/re$$

$$V_{test} = - (v2/re2 ro2 + v2)$$

$$Ro = v_{test}/i_{test} = \frac{-((ro2/re2) + 1)}{ro1(gm2 - 1/re2)} = \frac{-(ro2 + re2)}{(gm2re2 - 1)}$$

neglect

$$= \frac{(ro2)}{(1-gm2re2)} = ro2 \beta = Ro$$



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CE-CB CASCODE CONFIGURATION

Summary: $R_{in} = r_{\pi} l$
 $R_{out} = r_o 2 \beta$
 $A_v = g_m^2 r_o 2 \beta$
(no miller capacitance) giving high bandwidth

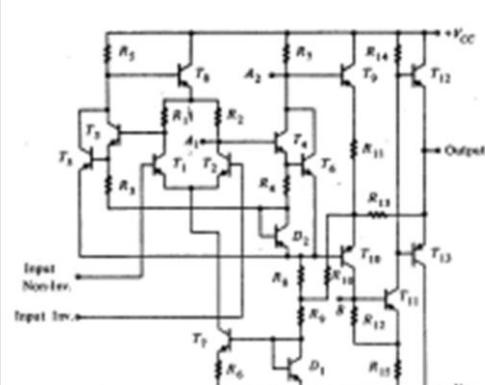


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709 OPERATIONAL AMPLIFIER



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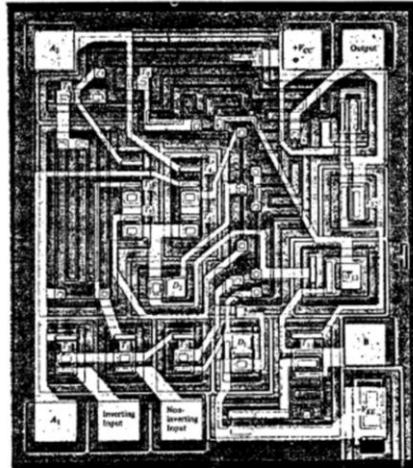


Figure 5.21 Circuit layout for the 709 operational amplifier. (Photo: Fairchild.)

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This circuit is a 709 Operational Amplifier. We should be able to recognize some of the sub circuits. T1 and T2 is a differential amplifier. The output is taken on both outputs and go into a second differential amplifier that uses Darlington transistors. The output of the second differential amplifier is take single sided at A2 to T9 which is a common emitter stage and level shifting stage. The output transistors T12 and T13 is NPN/PNP push-pull common collector stage. We also recognize current source T7 and diode D2.

741 OPERATIONAL AMPLIFIER

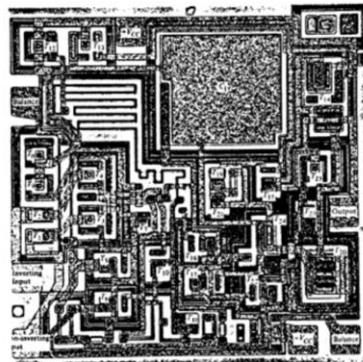
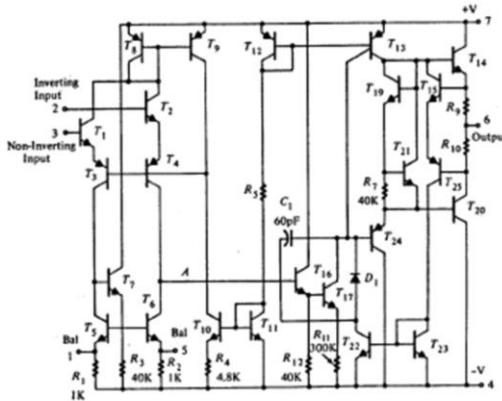


Figure 5.23 Photomicrograph of the 741 operational amplifier. Die size: 56 mils square. (Photo: Fairchild.)



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This is the circuit schematic for the 741 op amp. The inputs go to common collector common base differential amplifier. There is a large compensation capacitor of 60pF and a large resistor visible in the layout. A simplified schematic is shown on the next page.

SIMPLIFIED 741 OP AMP SCHEMATIC

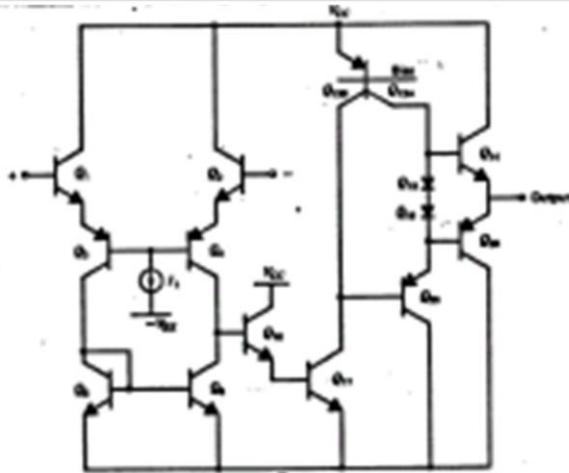


Fig. 6.14 Simplified, conceptual schematic diagram of the 741 amplifier.

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The first stage is CC-CB differential amplifier with active load. The output is taken single sided for its high input resistance followed by a common emitter gain stage with an active load with split collector acting as a current source for the level shifting and crossover distortion elimination stage that drives the NPN/PNP common collector push-pull output stage.

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1. Sedra and Smith,
2. Device Electronics for Integrated Circuits, 2nd Edition, Kamins and Muller, John Wiley and Sons, 1986.
3. The Bipolar Junction Transistor, 2nd Edition, Gerald Neudeck, Addison-Wesley, 1989.
4. Analog Integrated Circuits, Gray and Meyers



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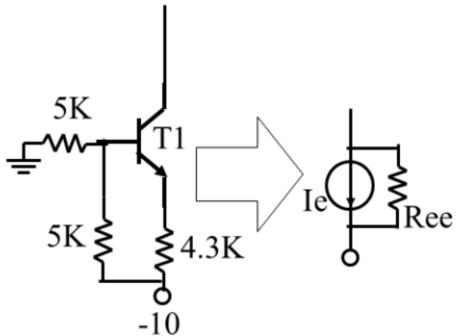
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HOMEWORK – BIPOLEAR IC DESIGN

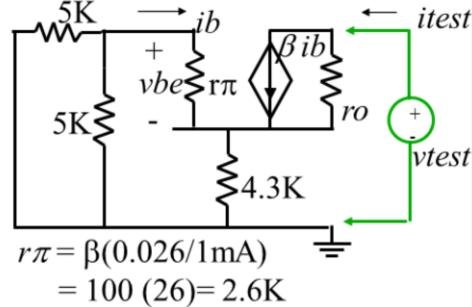
1. Derive the exact value of R_{ee} for the current source on page 15.
2. Design a $100 \mu A$ current source. See page 17.
3. For the simple op amp shown on page 30
 - a. let $v_{in1} = v_{in2} = \text{zero}$. Select values for R_C and R_B such that $V_{out} = \text{zero}$.
 - b. What is the maximum load current before current limiting?
 - c. Calculate the small signal differential voltage gain.
4. Do a SPICE analysis of the simple op amp on page 30. Show DC V_{out} vs V_{in} and Voltage Gain. **Answer: Gain ~128**
5. Do a SPICE analysis of the differential amplifier using active loads shown on page 37. Let $V=10\text{volts}$. Show DC V_{out} vs V_{in} and Gain. **Answer: Gain ~2000**

CURRENT SOURCE (HW Problem 1)

There are many types of current sources. Consider the following:



What is I_e ? (Ans: 1mA)



$R_{EE} = \infty$ if $r_o = \infty$ (not there)

R_{EE} is calculated by students in pro.1.

R_{EE} in this example is 4.68 Meg

if $\beta = 100$ and $r_o = 100\text{K}$



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HW PRO. 1 SOLUTION (CONT)

Let $r\pi = 2.6K$ and $r_o = 100K$, $\beta = 100$

$$R_x = 5K//5K + 2.6K = 5.1K$$

$$i_b = -I_{test} \cdot 4.3K / (R_x + 4.3K)$$

$$V_{test} = I_{test} \cdot (r\pi + 2.5K) // 4.3K + (I_{test} - \beta i_b) r_o$$

$$R_{ee} = V_{test}/I_{test} = (r\pi + 2.5K) // 4.3K + r_o - \beta r_o (4.3K / (R_x + 4.3K))$$

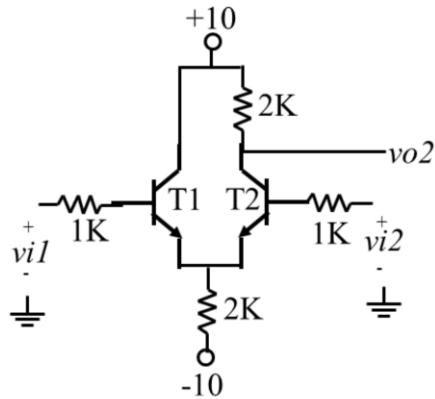
$$100 \quad 100K \quad 0.448 = 4.48 \text{ MEG}$$

$$\begin{aligned} R_{ee} &= 2.33K + 100K + 4.48 \text{ MEG} \\ &= 4.6 \text{ MEG} \end{aligned}$$



SOLUTION TO EXAMPLE ON PAGE 10

Analyze the following differential amplifier, $\beta=200$



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SOLUTION TO EXAMPLE ON PAGE 10

DC analysis: if $V_{in1} = V_{in2} = \text{zero}$, $I_{C1} = I_{C2}$ and $I_{B1}=I_{B2}$

$$\text{KVL: } I_{B1} 1\text{K} + 0.7 + 2(\beta+1)I_{B2} 2\text{K} - 10 = 0$$

$$I_{B1} = 9.3 / (1\text{K} + 2(200+1) 2\text{K}) = 11.6\mu\text{A}$$

$$I_{C1} = 200 I_{B1} = 2.32 \text{ mA}$$

$$V_{CE1} = 10 - I_{B1} 1\text{K} - 0.7 = 10.7$$

$$V_{CE2} = 10 - I_{C2} 2\text{K} - 0.7 = 6.06$$

$$r_\pi = \beta V_T / I_C = 200 (0.026\text{V})/2.32 \text{ mA} = 2.24\text{K}$$



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SOLUTION TO EXAMPLE ON PAGE 10**AC analysis:**

$$Av_{dss} = \frac{1}{2} gm R_c r\pi / (1K + r\pi) = \frac{1}{2} 0.089 2K 2.24K / 3.24K = 61.7$$

or

$$Av_{dss} = \frac{1}{2} \frac{\beta R_c}{(r\pi + 1K)} = \frac{1}{2} (200) 2K / (1K + 2.24K) = 61.7$$

$$\frac{V_{oss}}{V_{ic}} = \frac{-\beta R_c}{2Re(\beta+1) + (r\pi + 1K)} = -400K / (4K(201) + 3.24K) = 0.496$$

$$CMMR = 61.7 / .496 = 125$$



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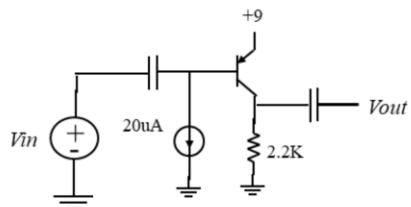
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Class Examples

Do the DC analysis of this circuit.

Find the small signal voltage gain V_{out}/V_{in} ,
Input resistance and output resistance.

Beta = 100
VA = infinite



Class Examples

Beta=100, VA = very large.

1.1 Do the DC analysis of this circuit with Vs=zero.
What is Vout (offset voltage)?

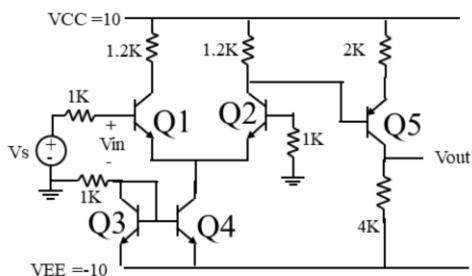
Answer: $V_{out} = -0.24 \text{ V}$

1.2. Calculate the voltage gain, Avmid.

Answer: $A_v = 214 \text{ V/V}$

1.3 What could be done to reduce the offset voltage
and increase the gain at the same time?

Answer: Increase 4K or Reduce 2K



Class Examples

1.1 State reasonable assumptions
 $V_A = \infty$ Beta=100

1.2 If V_{in} is zero calculate the RC value such that
 $V_{out} = 0$

Answer: $RC = 3.53K$

1.3 Calculate the voltage gain V_{out}/V_{in}

Answer: $A_V = 16400 \text{ V/V}$

