ECE 2300 - Lab 2 Report

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1 Introduction

The overall goal of this lab was to sucessfully decode a four bit input to an output number display on a seven section decoder. The lab was split into two sections, both involving breadboarding inputs to create a sucessful display. The first part allowed all inputs to be sent through a CMOS CD4511B 7 segment decoder, allowing us to test our initial breadboard setup, battery, and inputs. The second part allowed us to wire the decoders for inputs c, e, and g using only NAND gates and inverters.

The materials allowed to us in this lab consisted of a breadboard, two 72LS00 2-input NAND gate chips, one 72LS04 NOT gate, one 72LS10 3-input NAND gate, one 72LS20 4-input NAND gate, one CMOS CD4511B 7- segment decoder, one 74LS241 buffer, a resistor array, a 7-segment input display, along with a battery and a voltage regulator.

During our time in the lab, we were able to complete our design, achieving a fully functioning 7 segment display output on all digits 0 to 9. Although difficult to implement, we were able to take our pre-designed circuit and wire it correctly on the breadboard.

2 Design

The design of our logic circuit was based on the process of logic minimization through the use of Karnaugh maps. In order to create a minimized logic function for each segment of the 7-segment display, we created Karnaught maps for each of the outputs based on a truth table created from looking at the desired outputs. By our design specification, we were able to consider all inputs 10-15 to be "don't cares", simplifying our logic expressions.

3 Implementation and Testing

4 Conclusion

5 Work Distribution