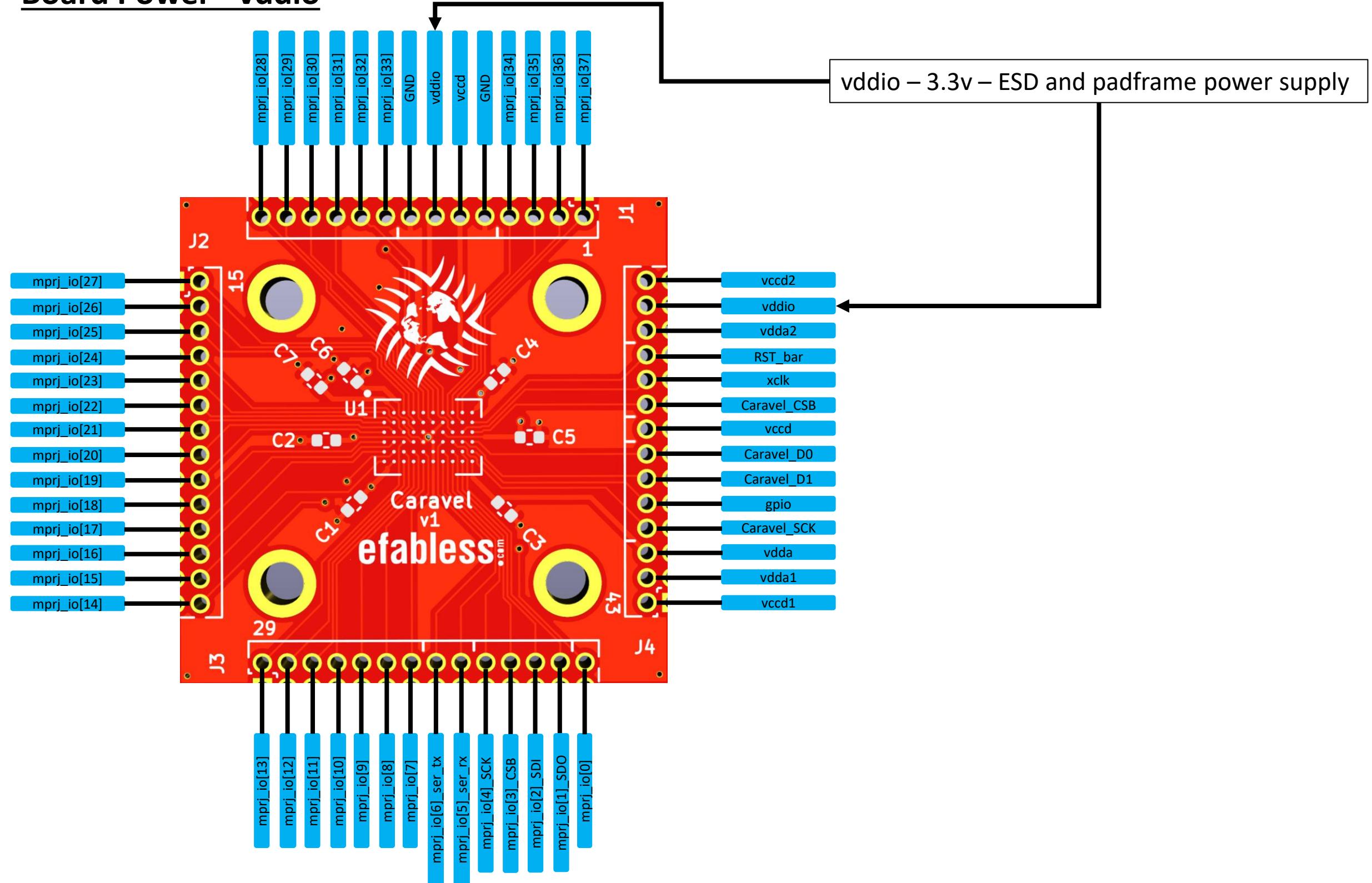
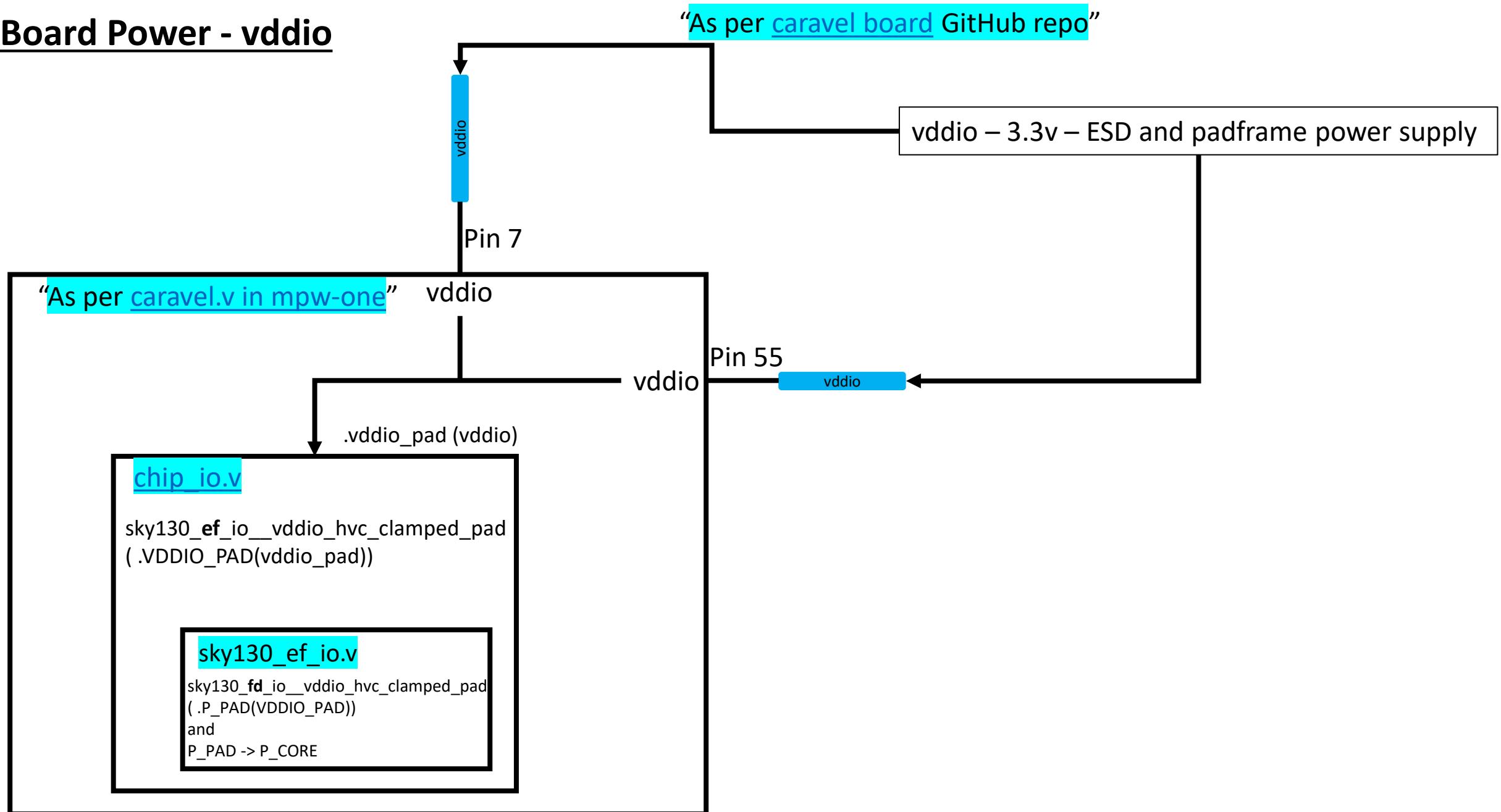


# Board Power

# Board Power - vddio

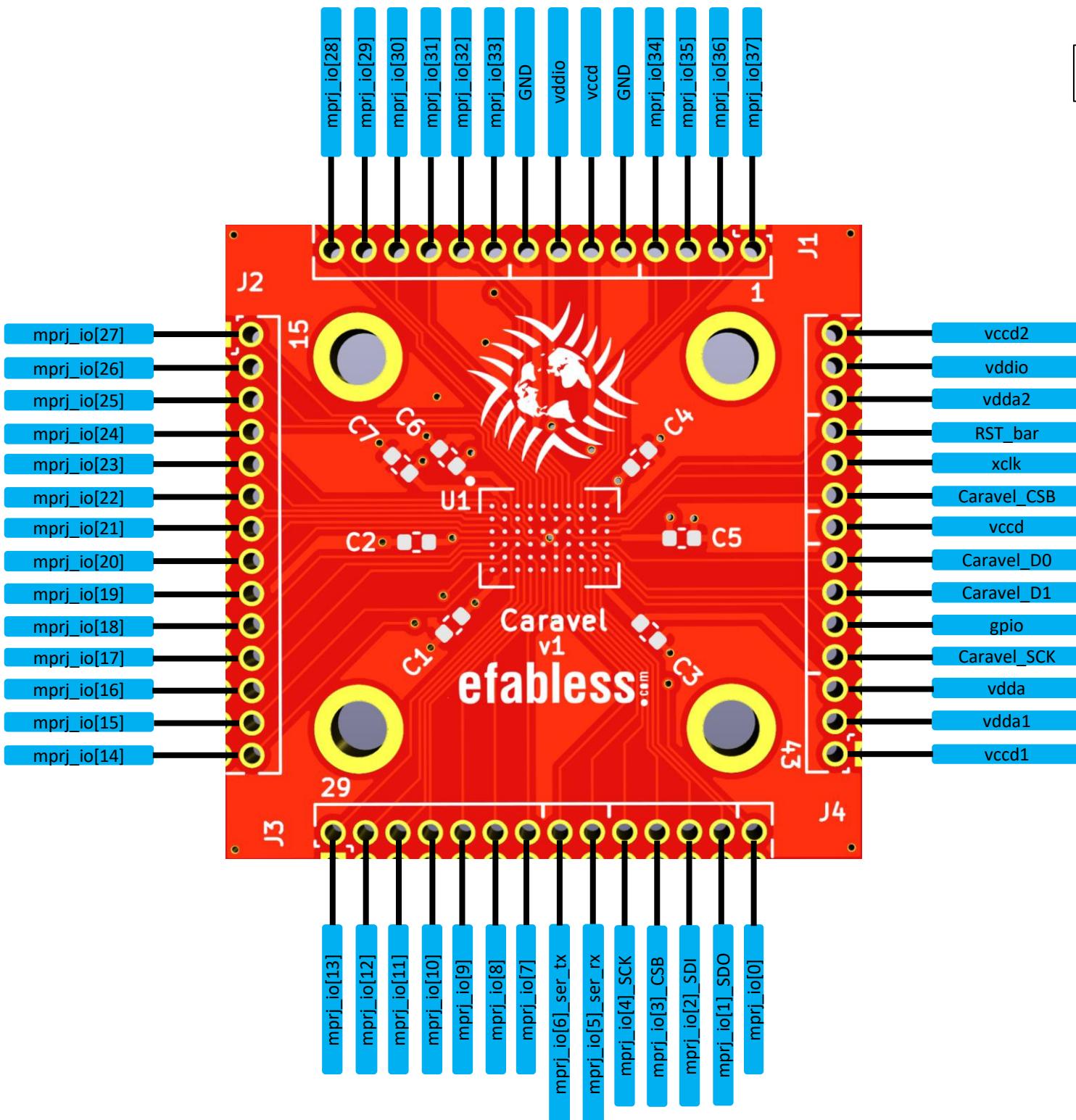


## Board Power - vddio



VDDIO trace down from board to package to chip pad frame to core

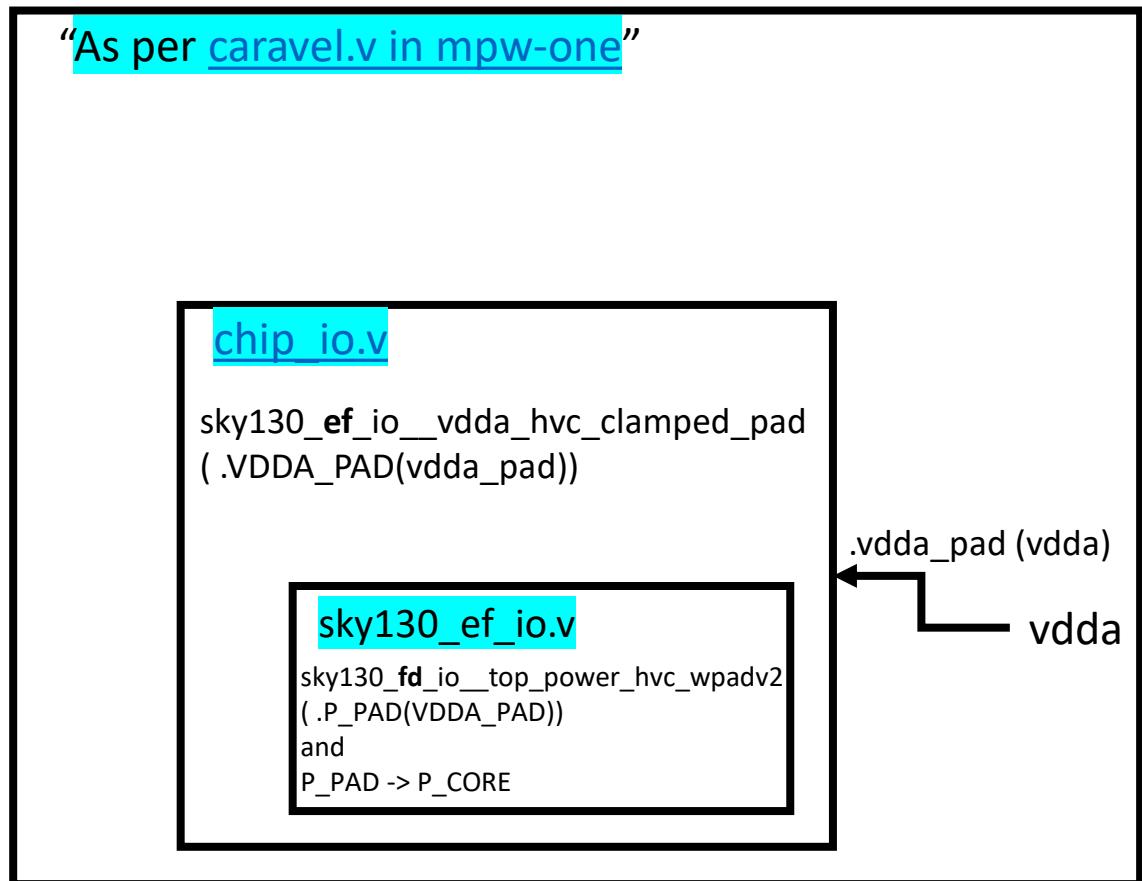
## Board Power - vdda



vdda – 3.3v – Management area power supply

## Board Power - vdda

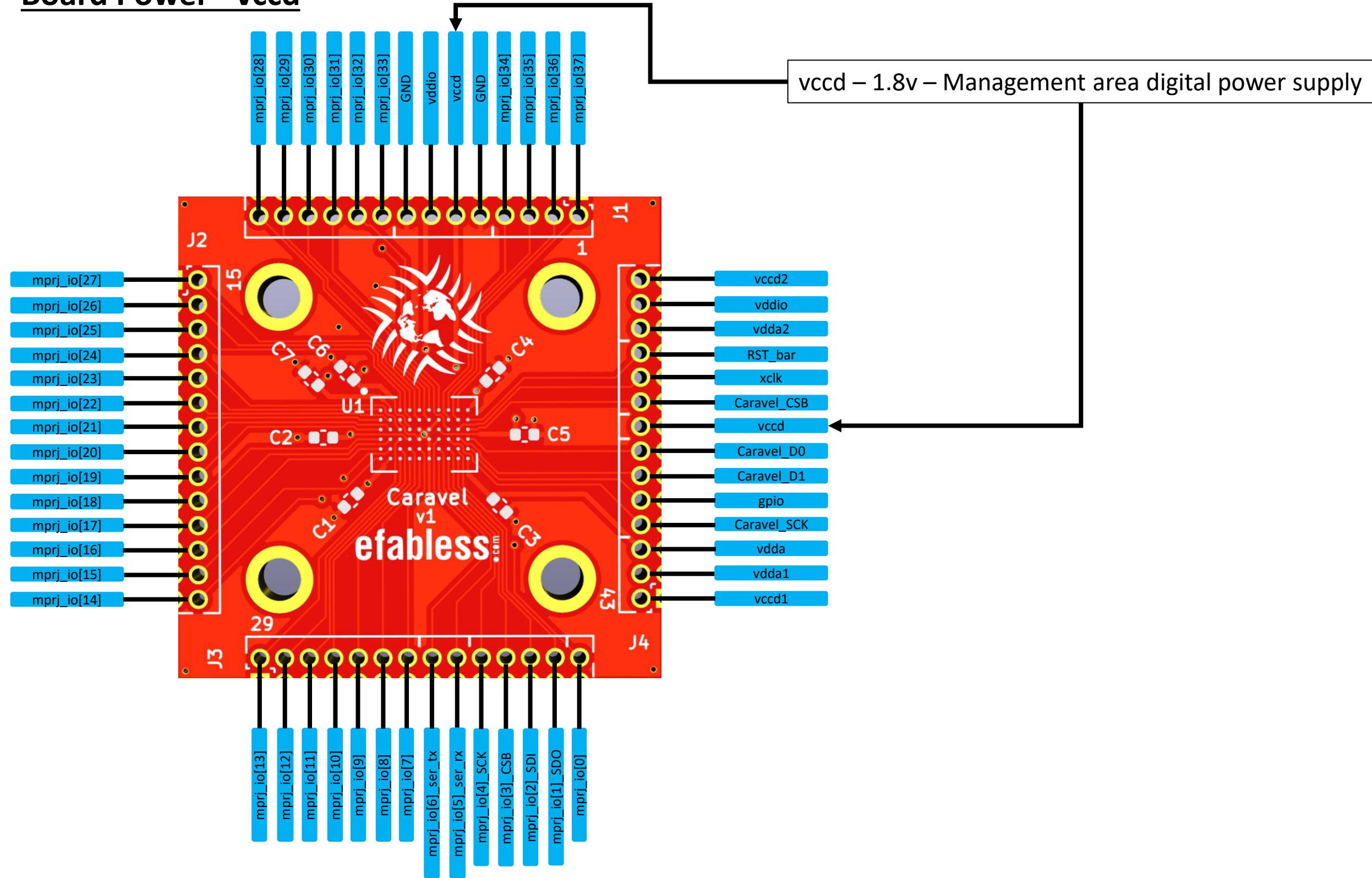
“As per [caravel board GitHub repo](#)”



vdda – 3.3v – Management area power supply

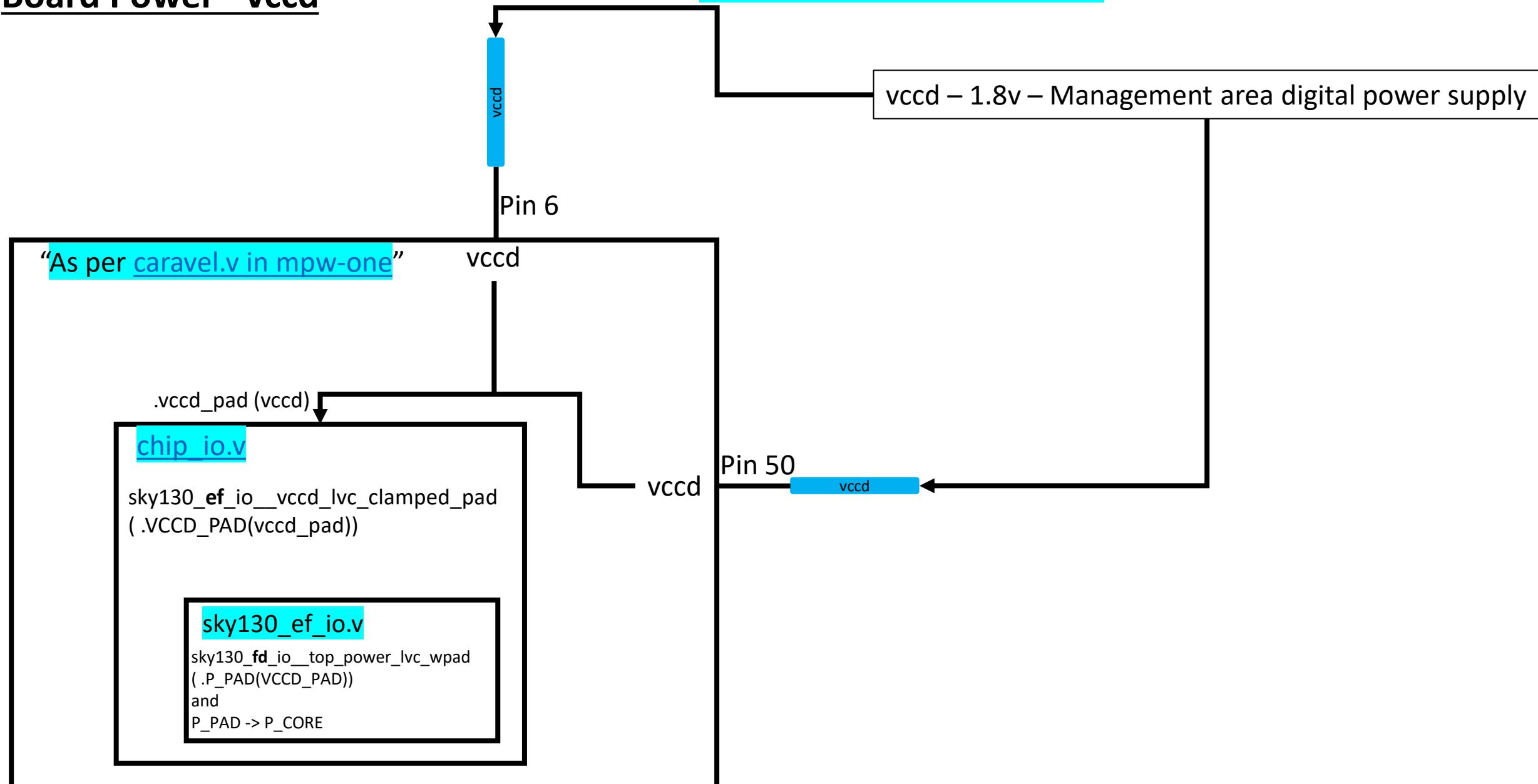
VDDA trace down from board to package to chip pad frame to core

## Board Power - vccd



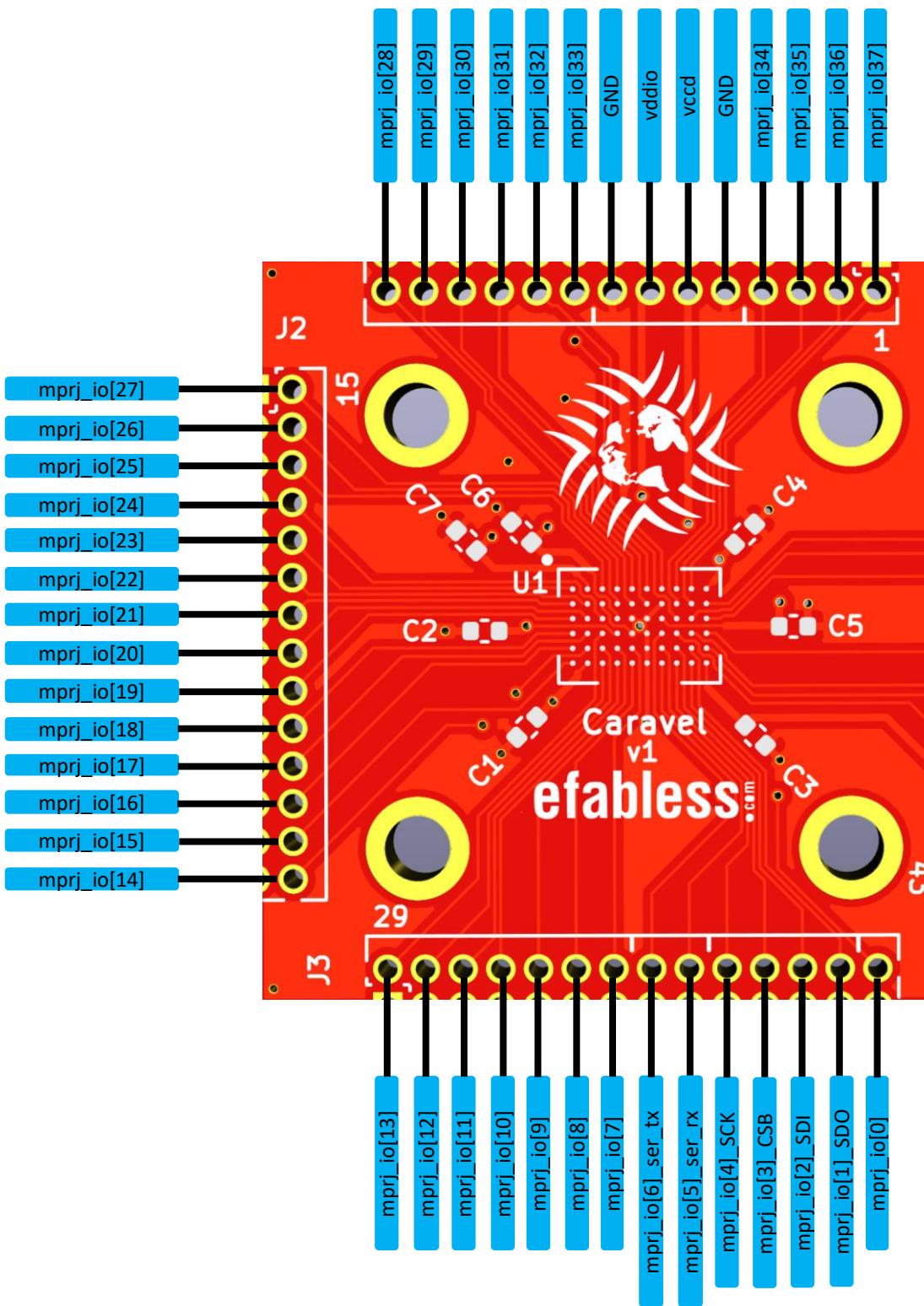
## Board Power - vccd

"As per [caravel board GitHub repo](#)"



VCCD trace down from board to package to chip pad frame to core

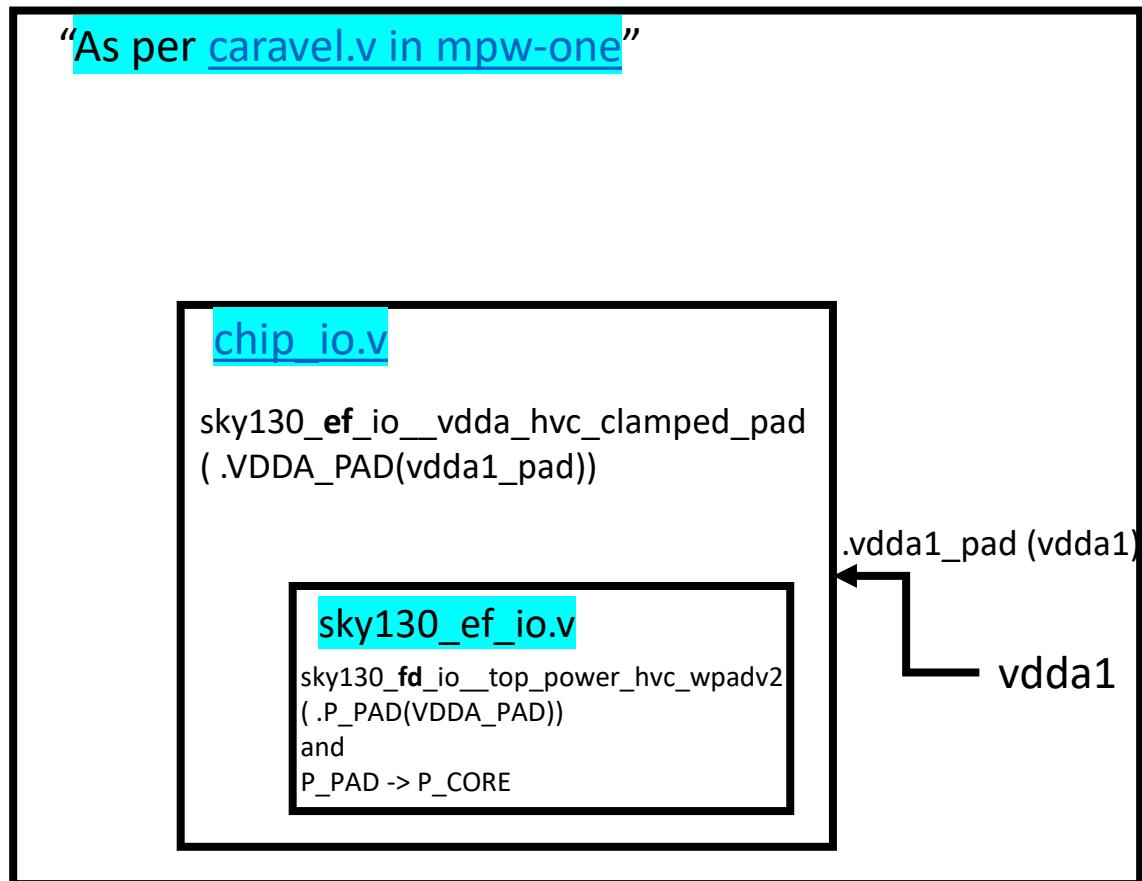
## Board Power – vdda1



vdda1 – 3.3v – User area 1 power supply

## Board Power – vdda1

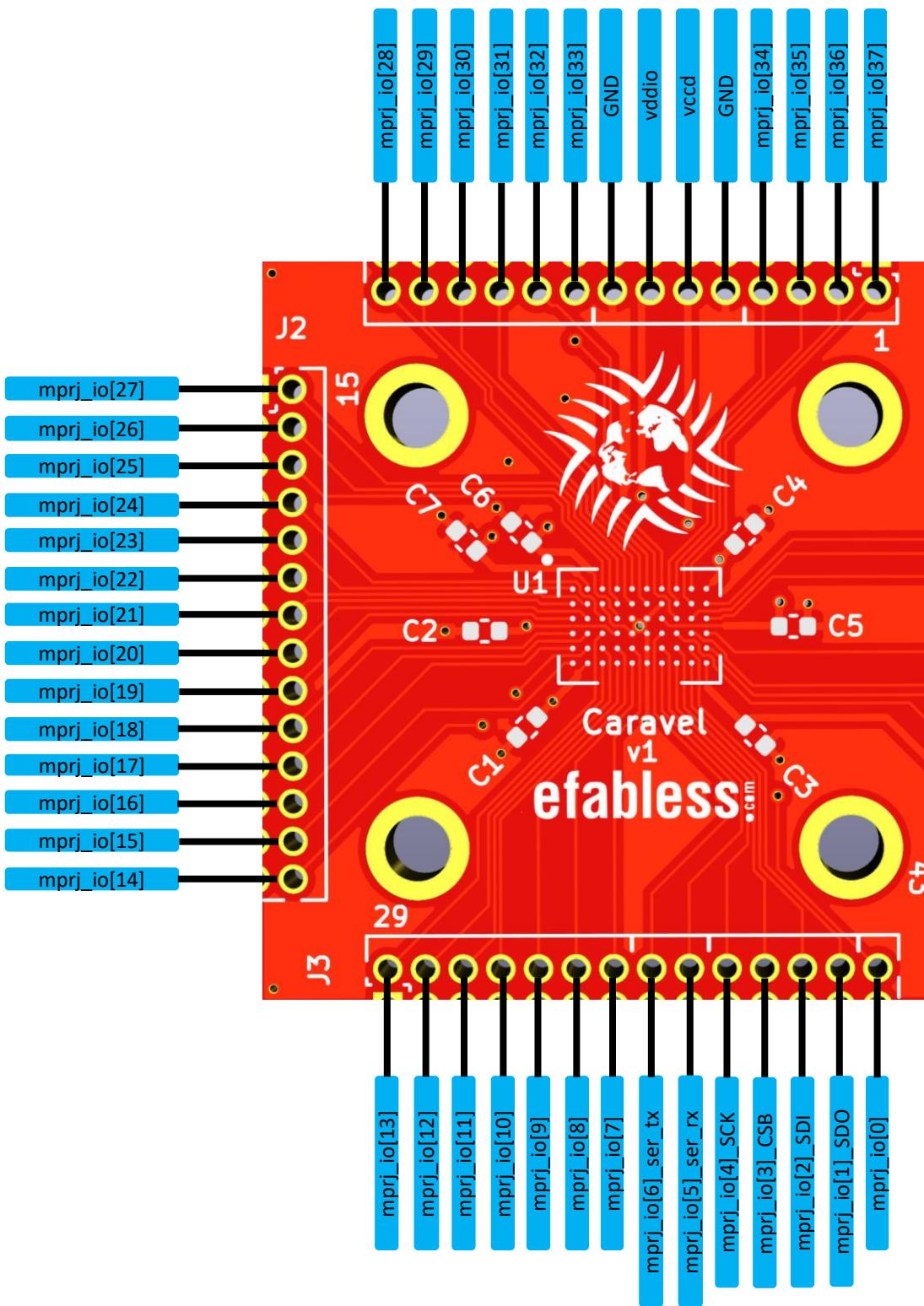
“As per [caravel board GitHub repo](#)”



vdda1 – 3.3v – User area 1 power supply

**VDDA1** trace down from board to package to chip pad frame to core

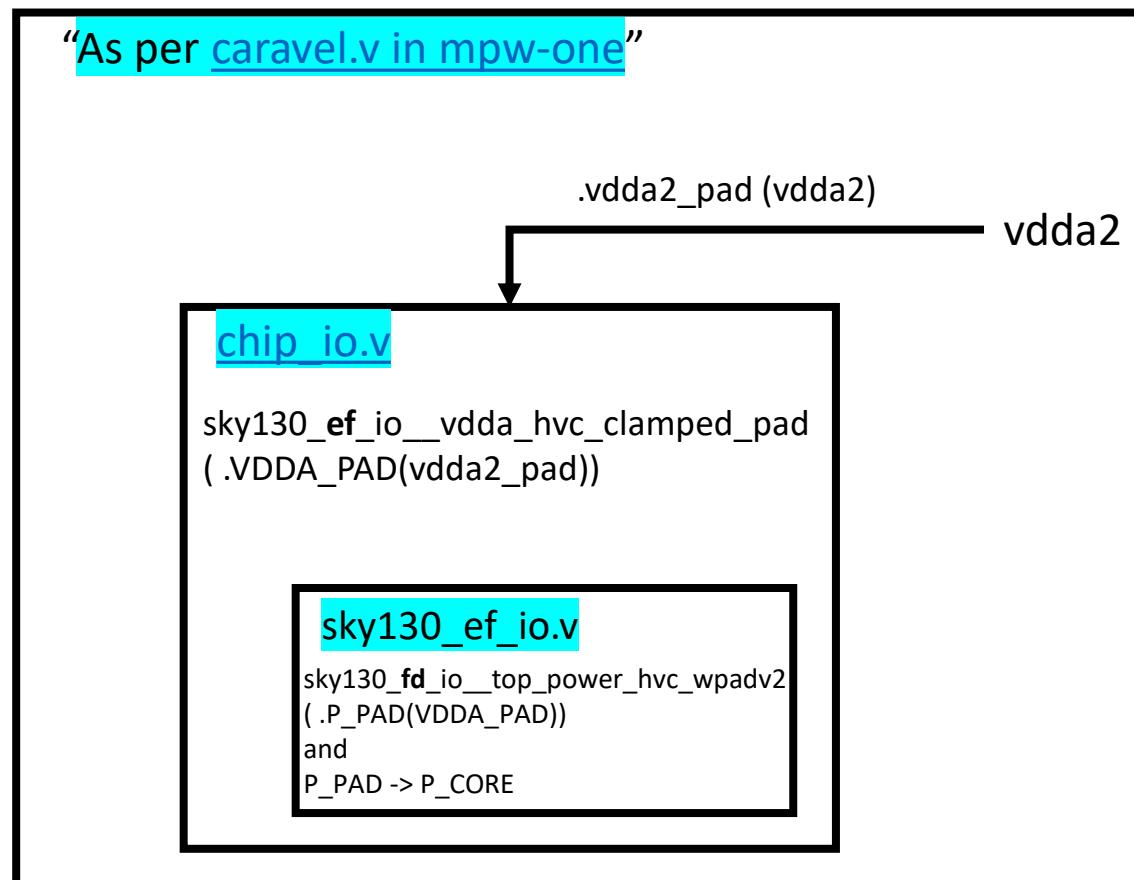
## Board Power – vdda2



vdda2 – 3.3v – User area 2 power supply

## Board Power – vdda2

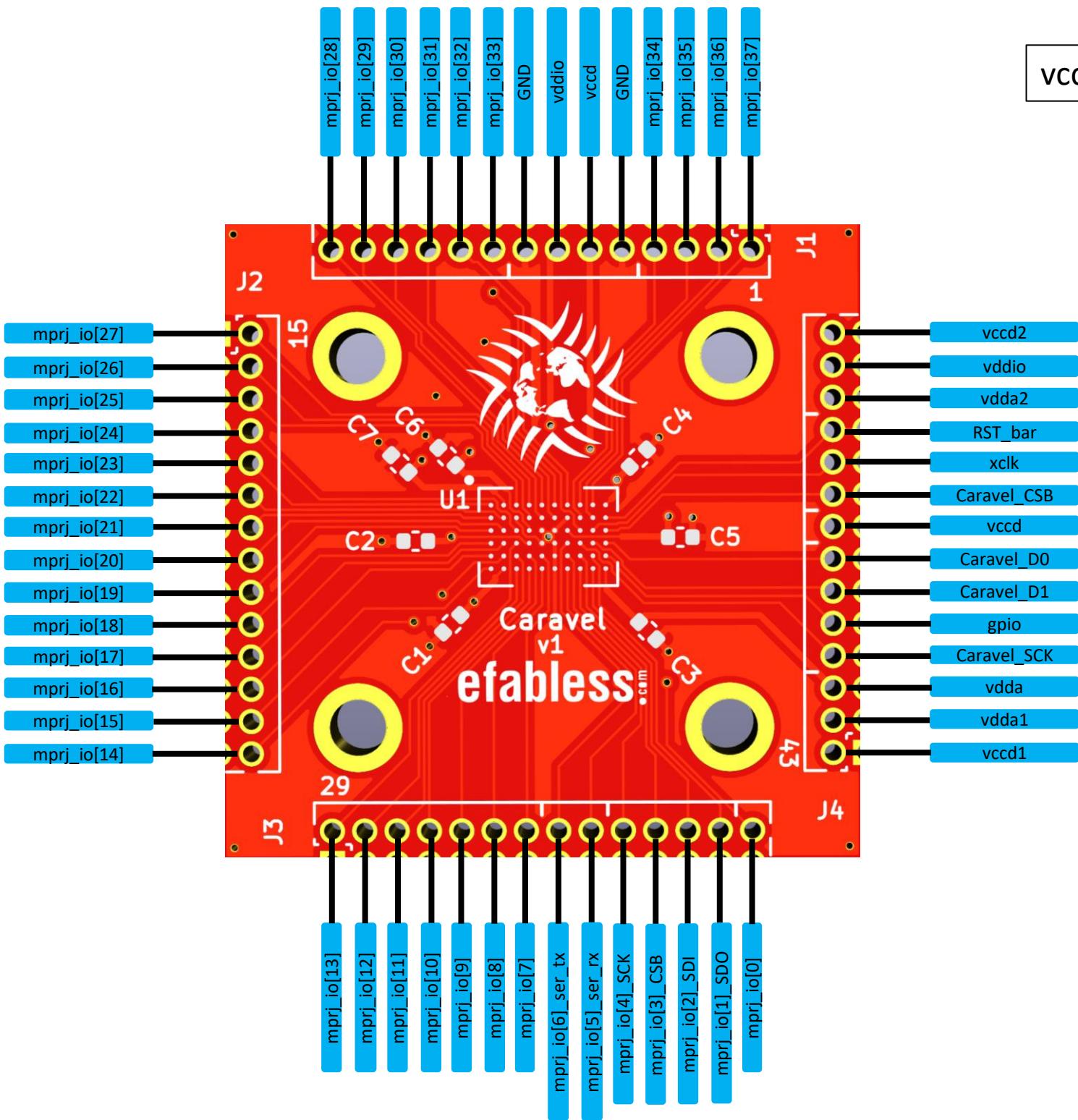
“As per [caravel board GitHub repo](#)”



vdda2 – 3.3v – User area 2 power supply

VDDA2 trace down from board to package to chip pad frame to core

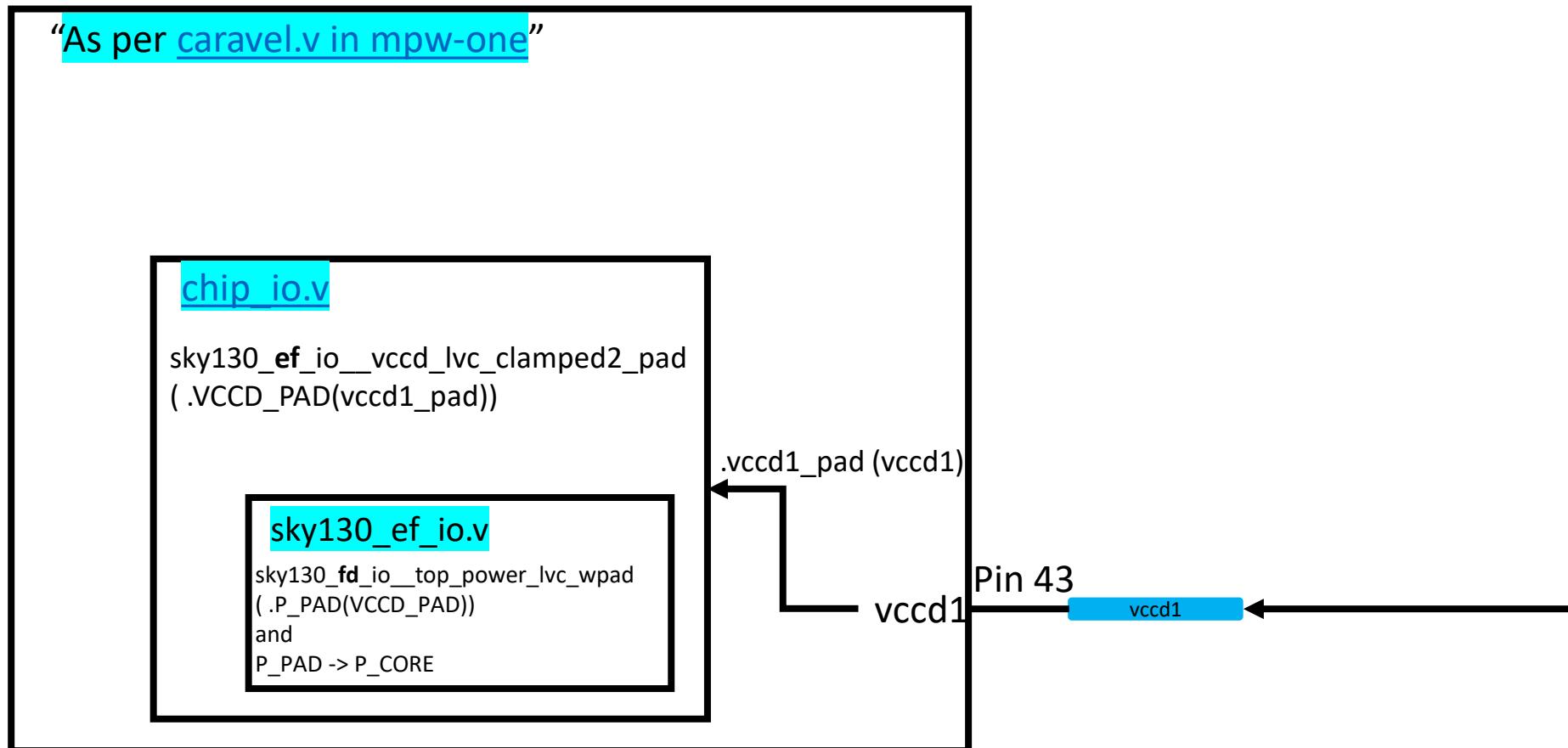
## Board Power – vccd1



vccd1 – 1.8v – User area 1 digital power supply

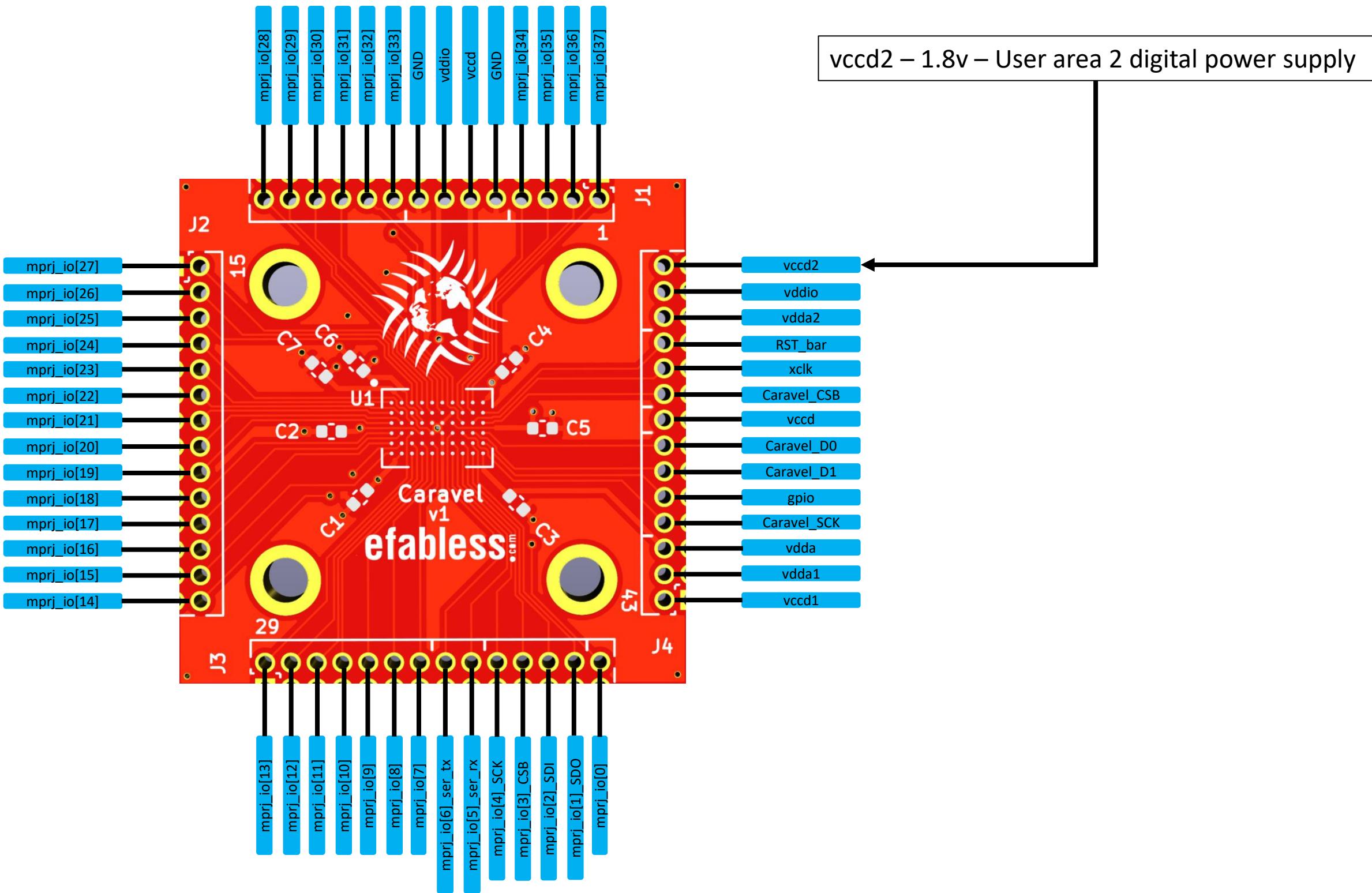
## Board Power – vccd1

“As per [caravel board GitHub repo](#)”



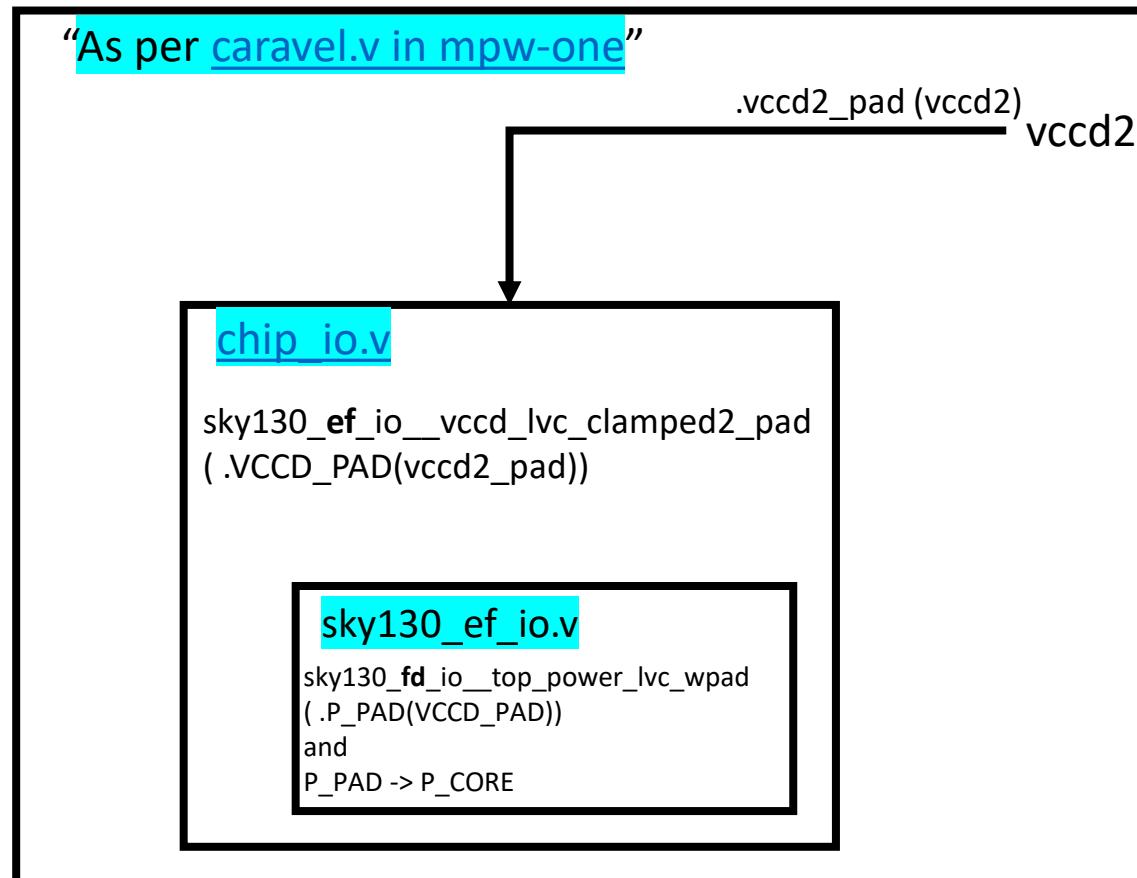
**VCCD1** trace down from board to package to chip pad frame to core

## Board Power – vccd2



## Board Power – vccd2

“As per [caravel board GitHub repo](#)”

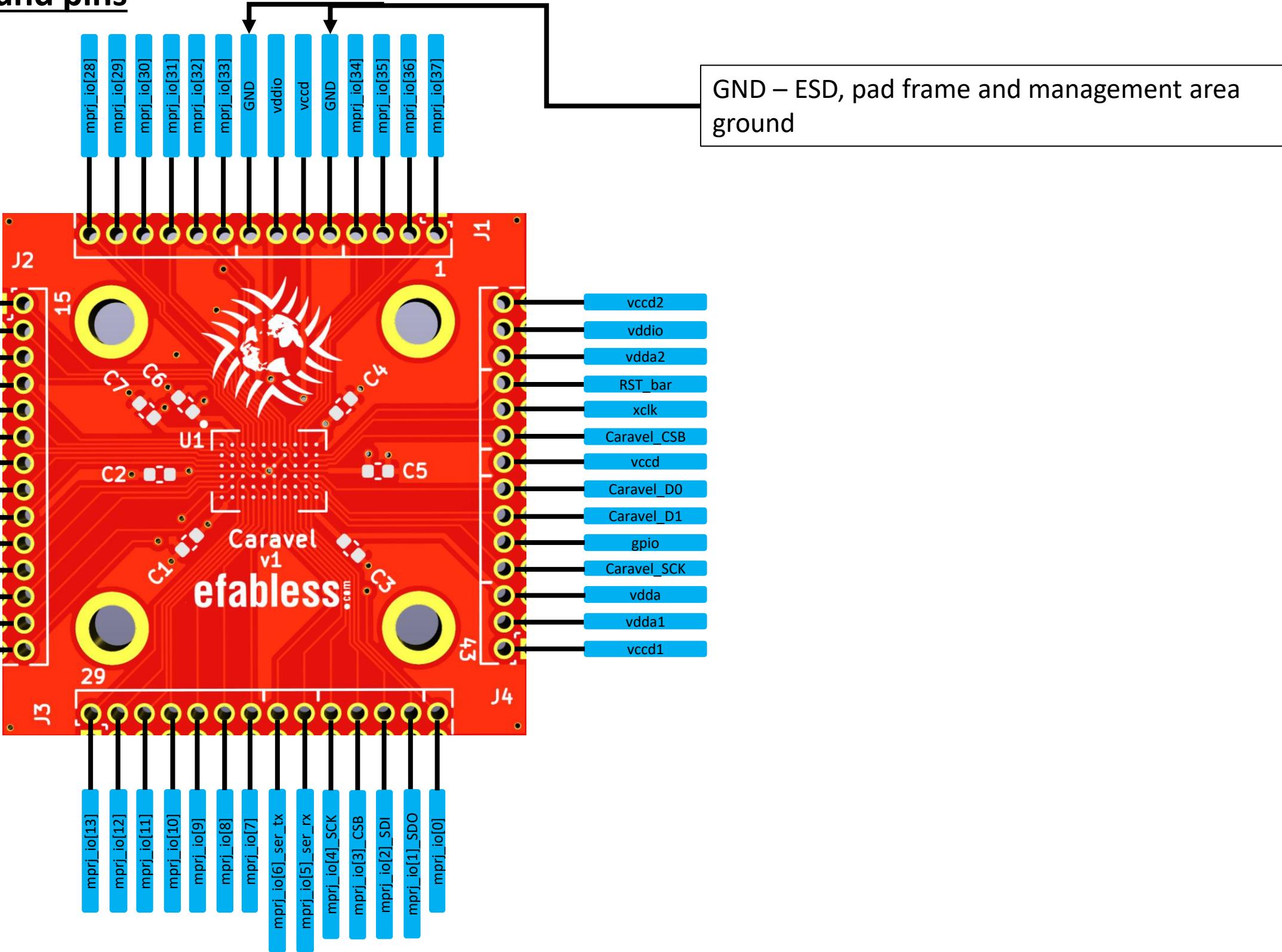


vccd2 – 1.8v – User area 2 digital power supply

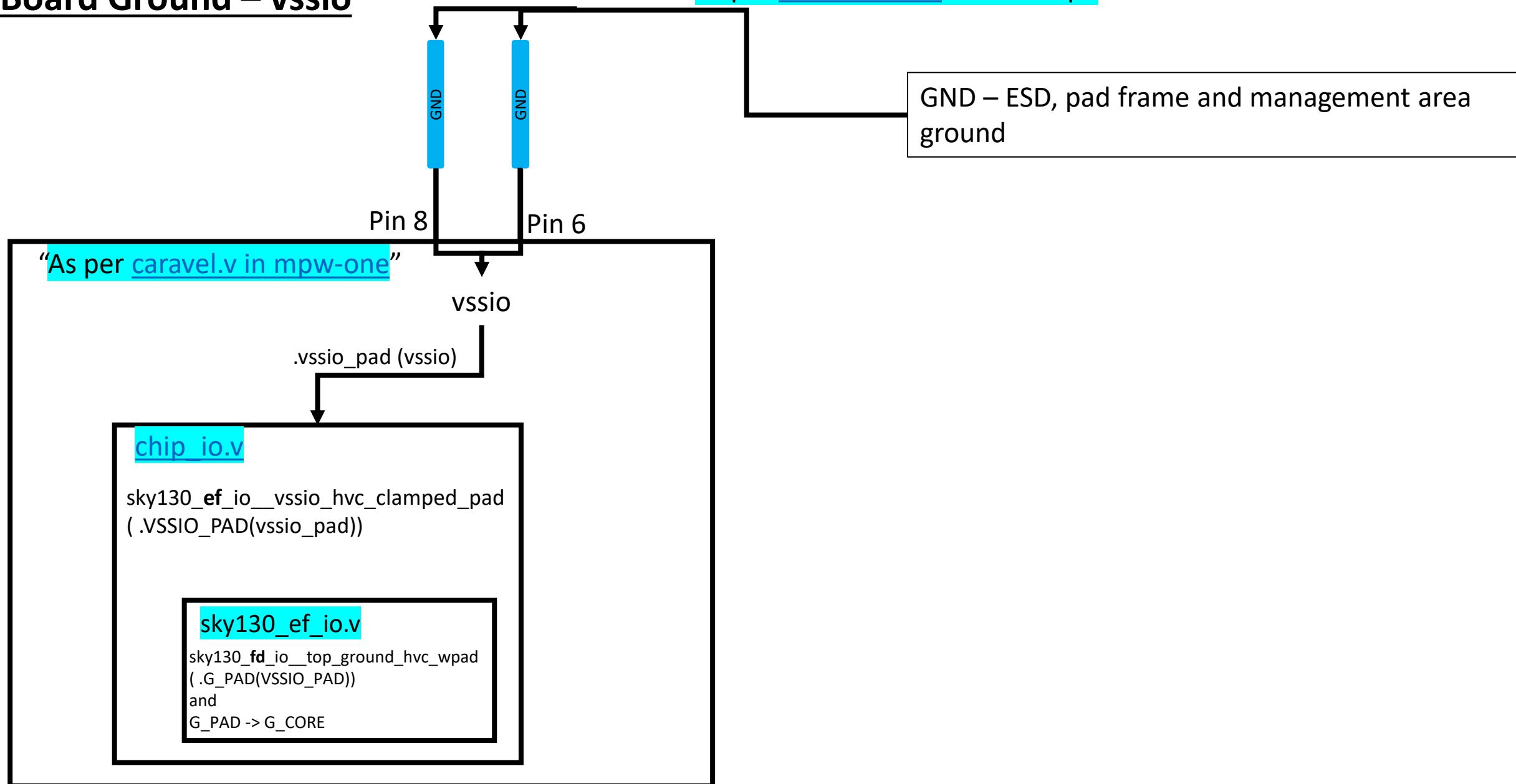
VCCD2 trace down from board to package to chip pad frame to core

**Board Ground**

## Board Ground pins

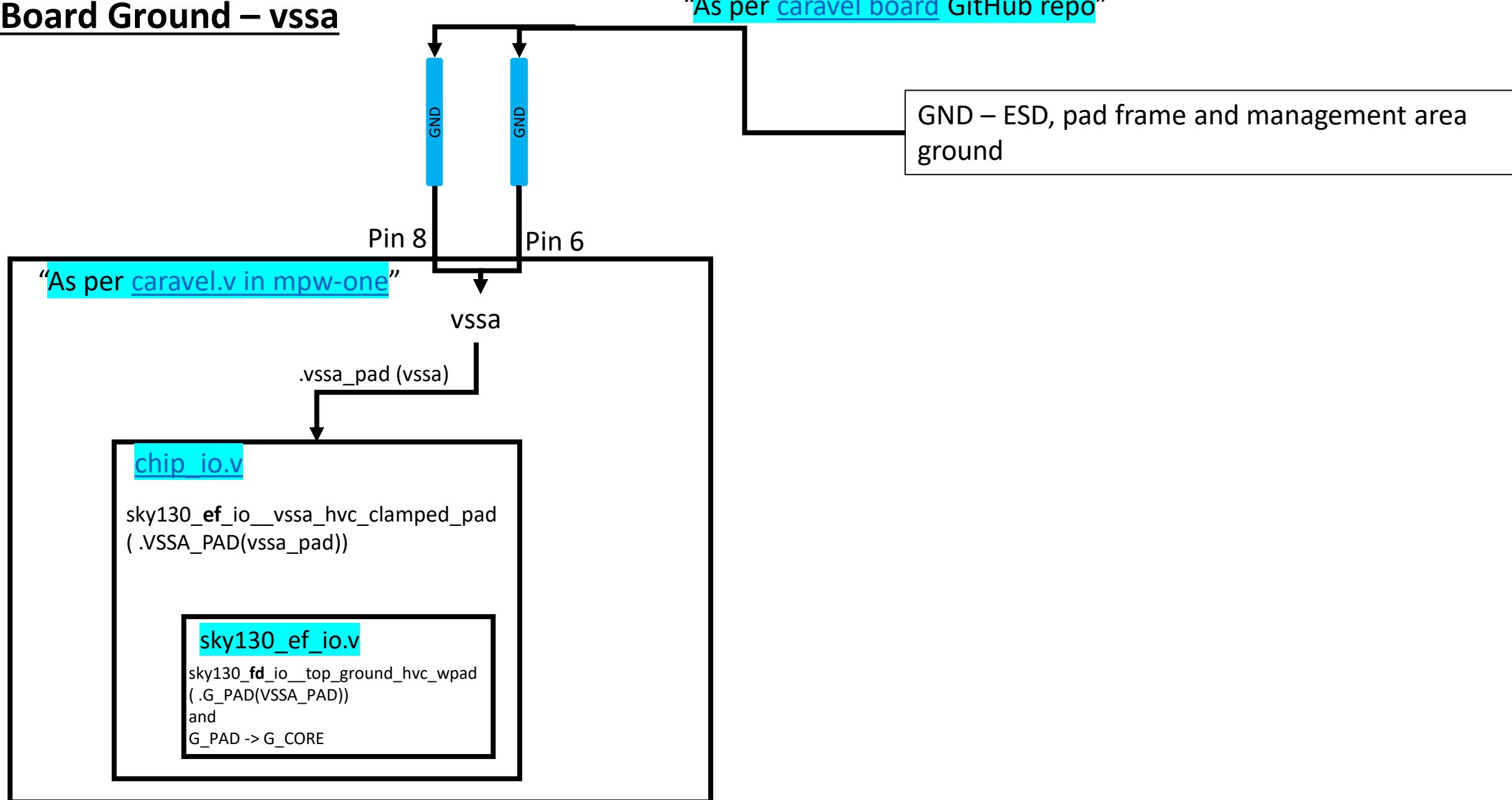


## Board Ground – vssio



**VSSIO** trace down from board to package to chip pad frame to core

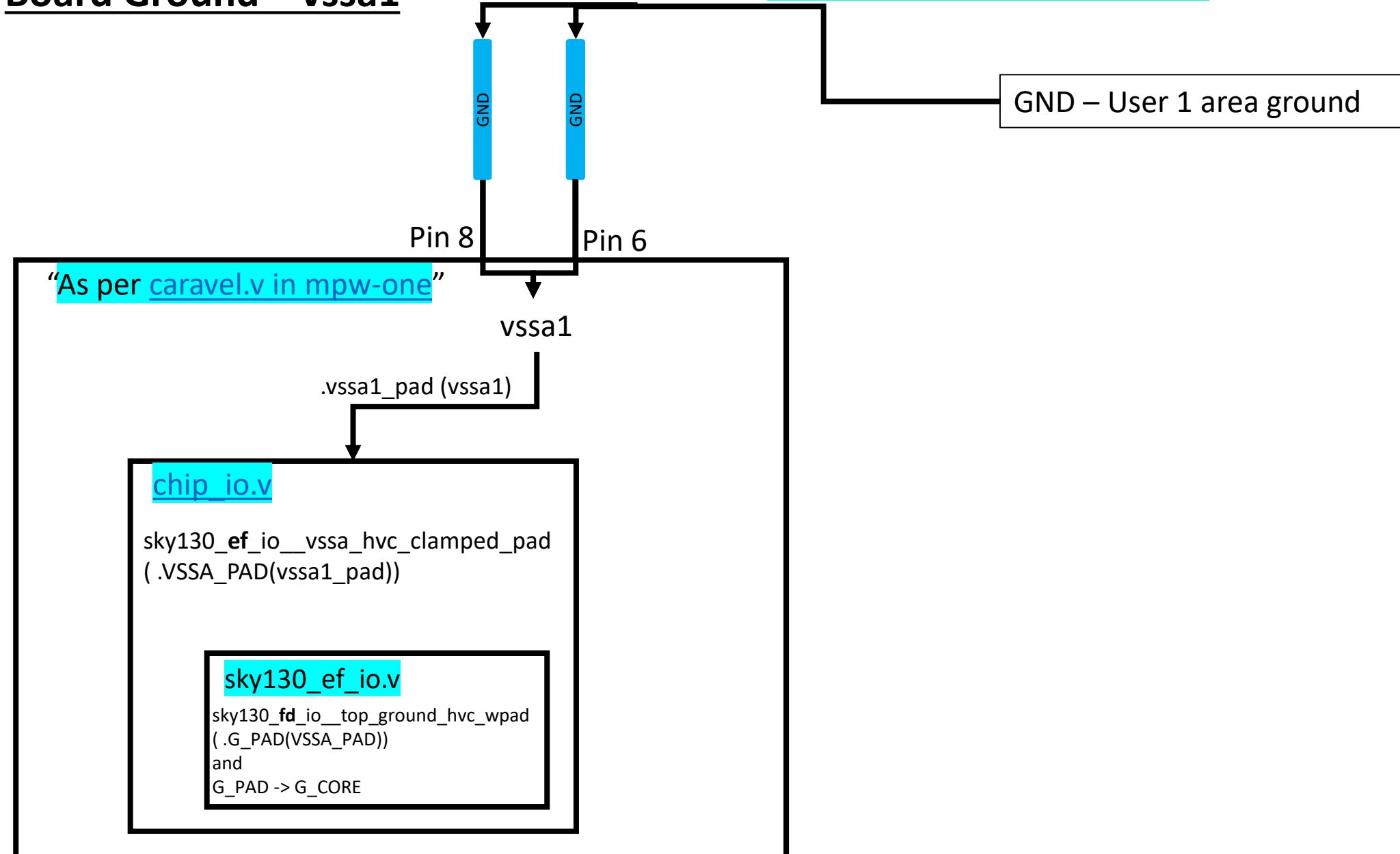
## Board Ground – vssa



VSSA trace down from board to package to chip pad frame to core

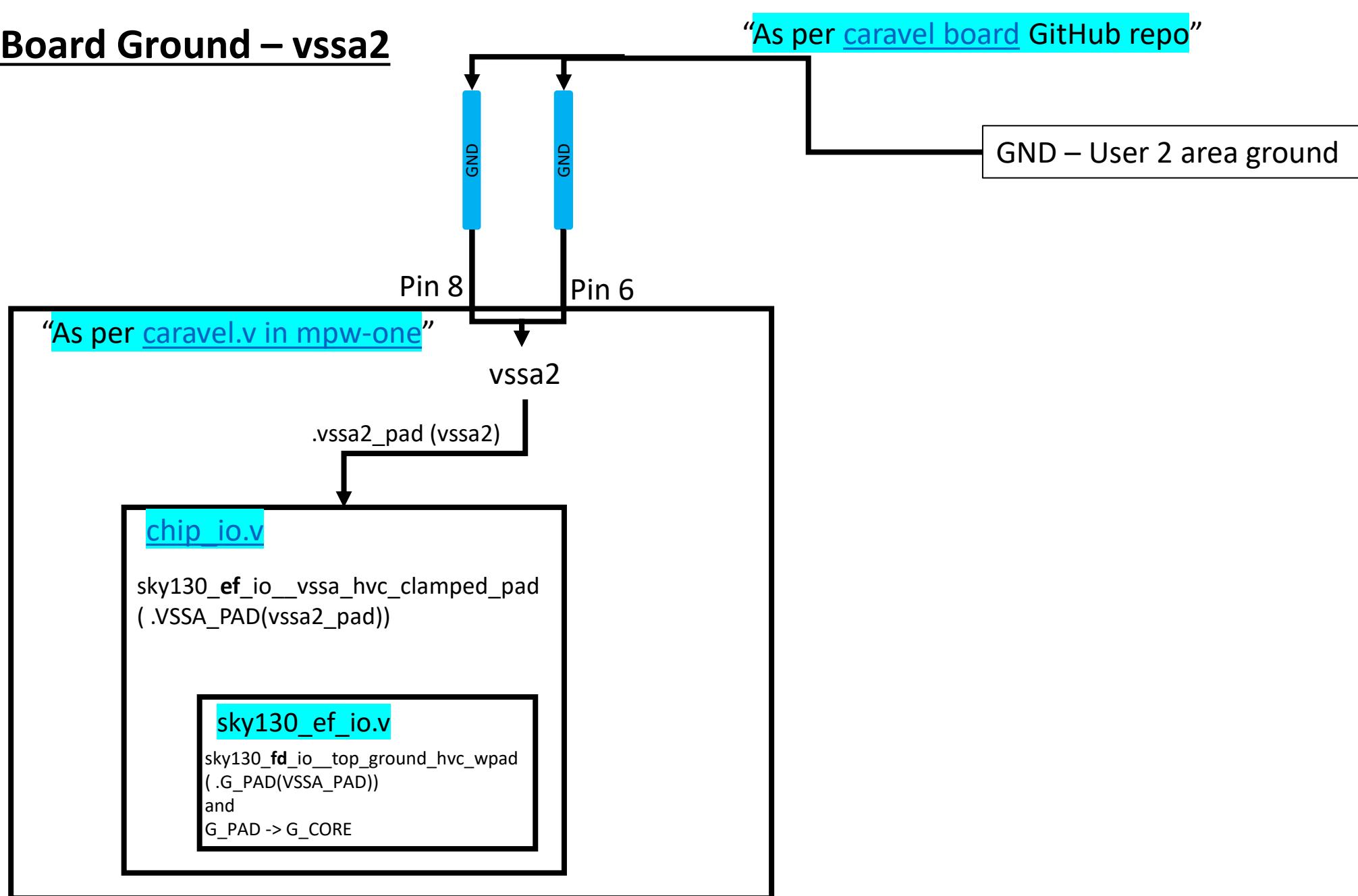
## Board Ground – vssa1

"As per [caravel board GitHub repo](#)"



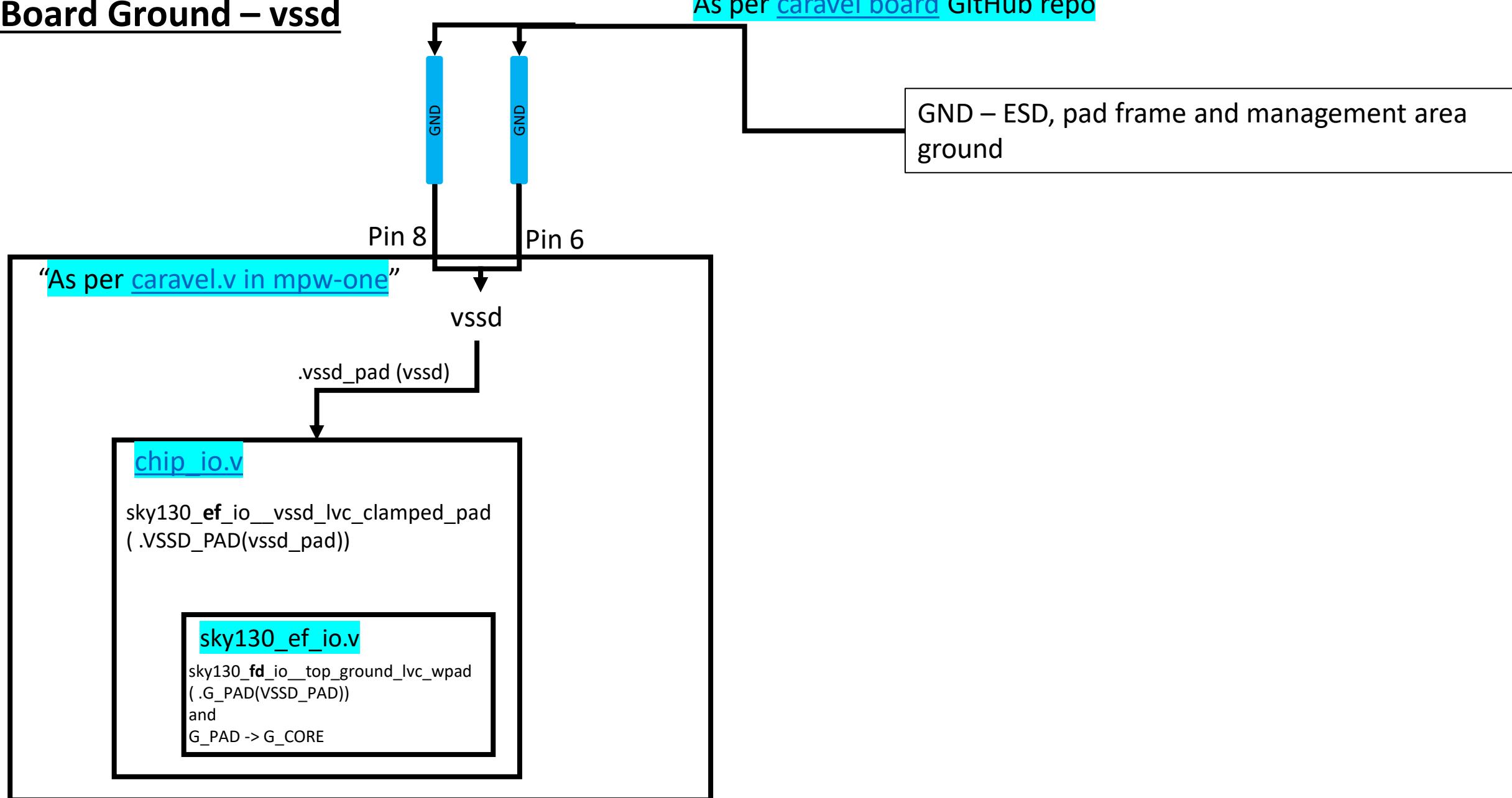
VSSA1 trace down from board to package to chip pad frame to core

## Board Ground – vssa2



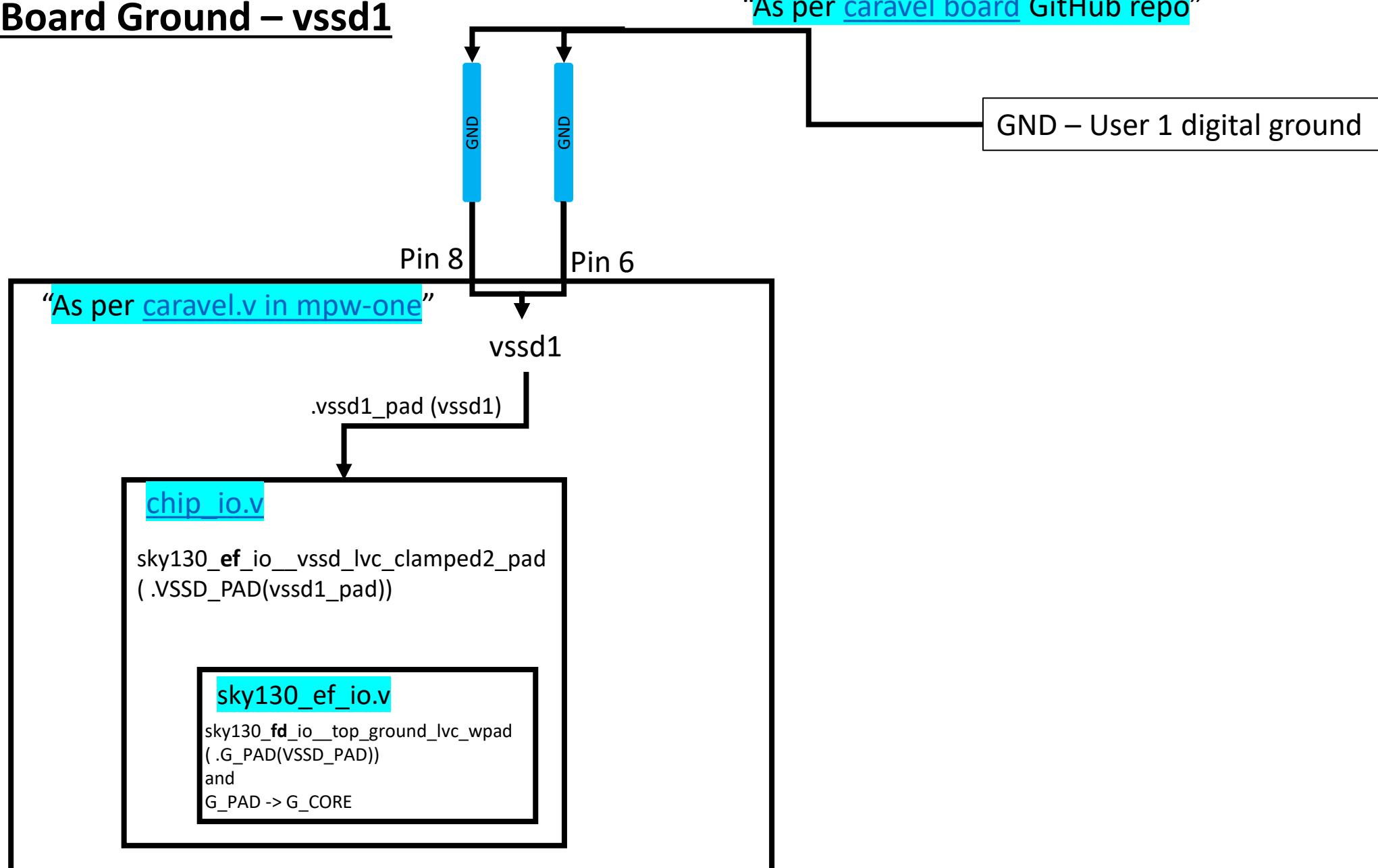
VSSA2 trace down from board to package to chip pad frame to core

## Board Ground – vssd



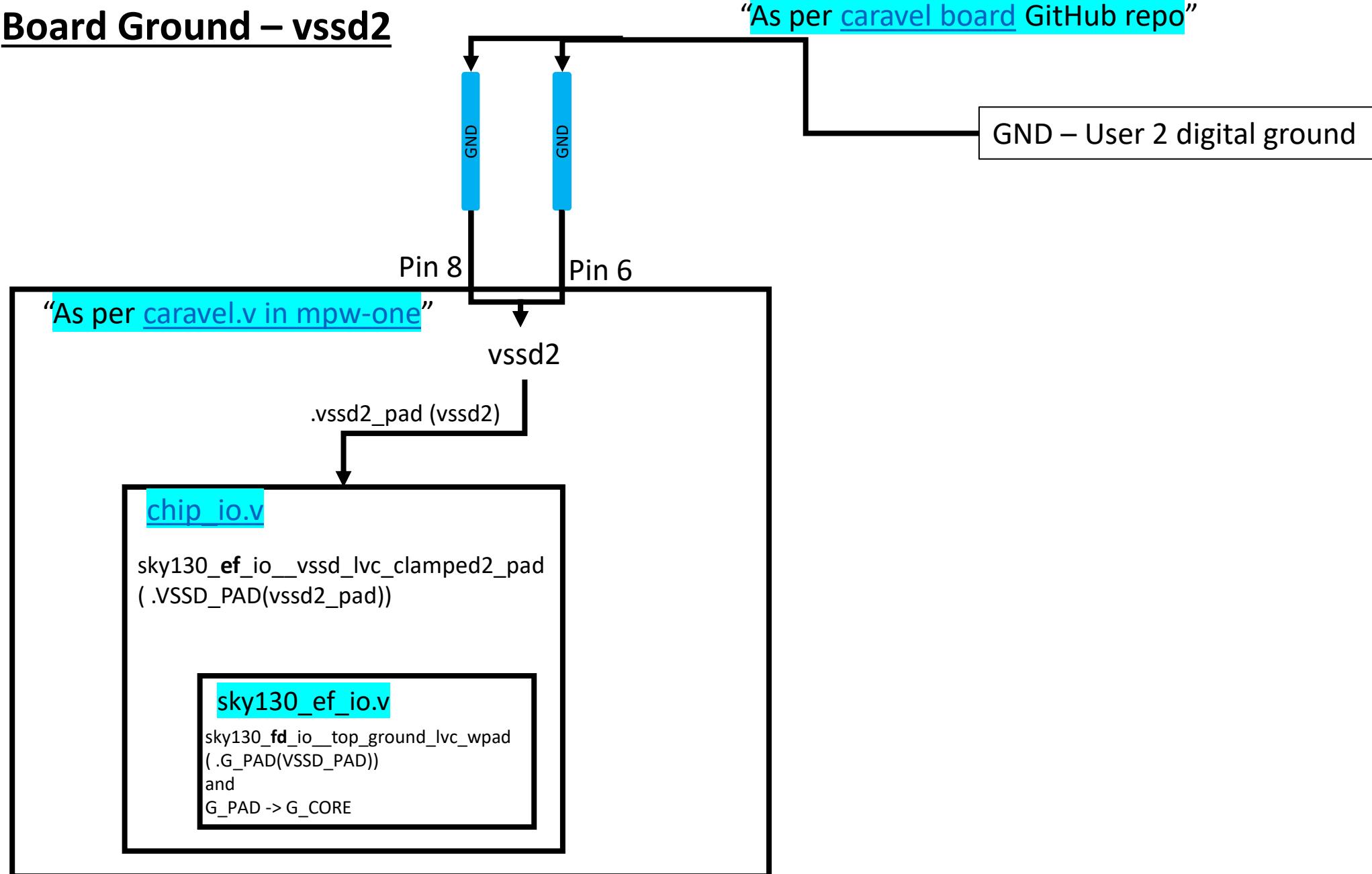
VSSD trace down from board to package to chip pad frame to core

## Board Ground – vssd1



VSSD1 trace down from board to package to chip pad frame to core

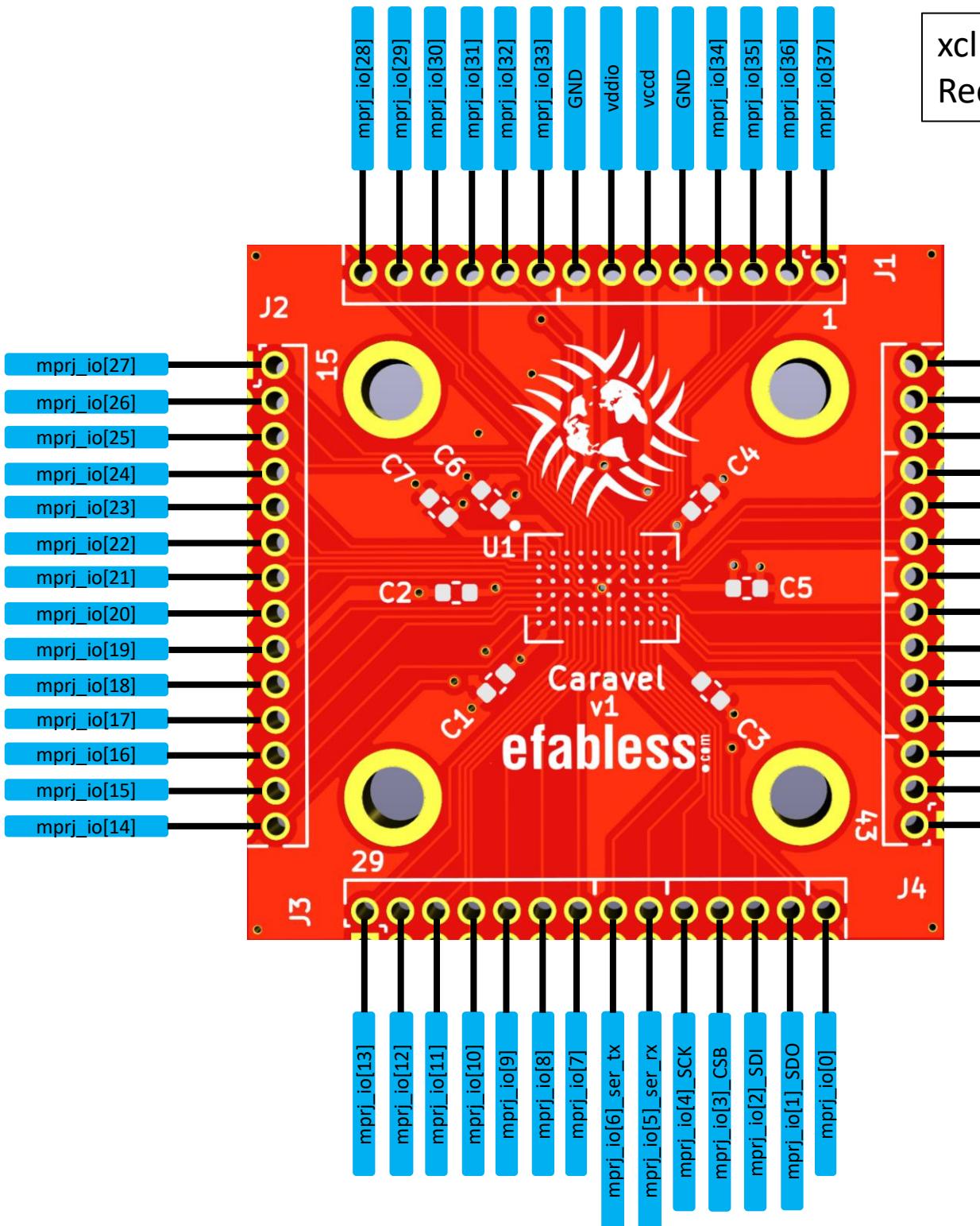
## Board Ground – vssd2



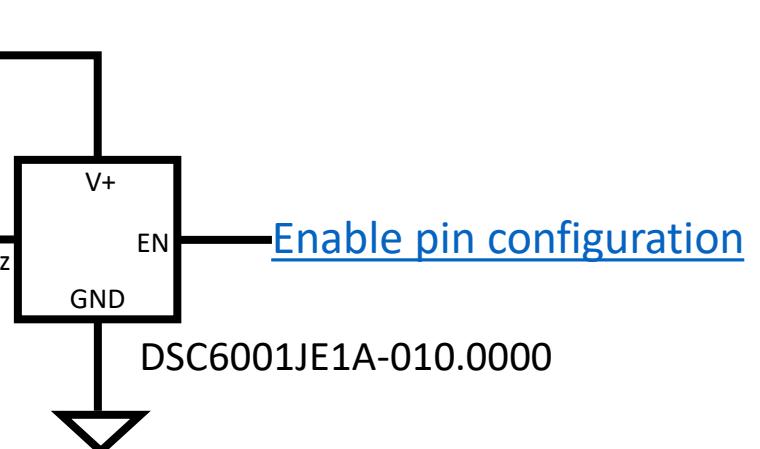
VSSD2 trace down from board to package to chip pad frame to core

# **Board Clock**

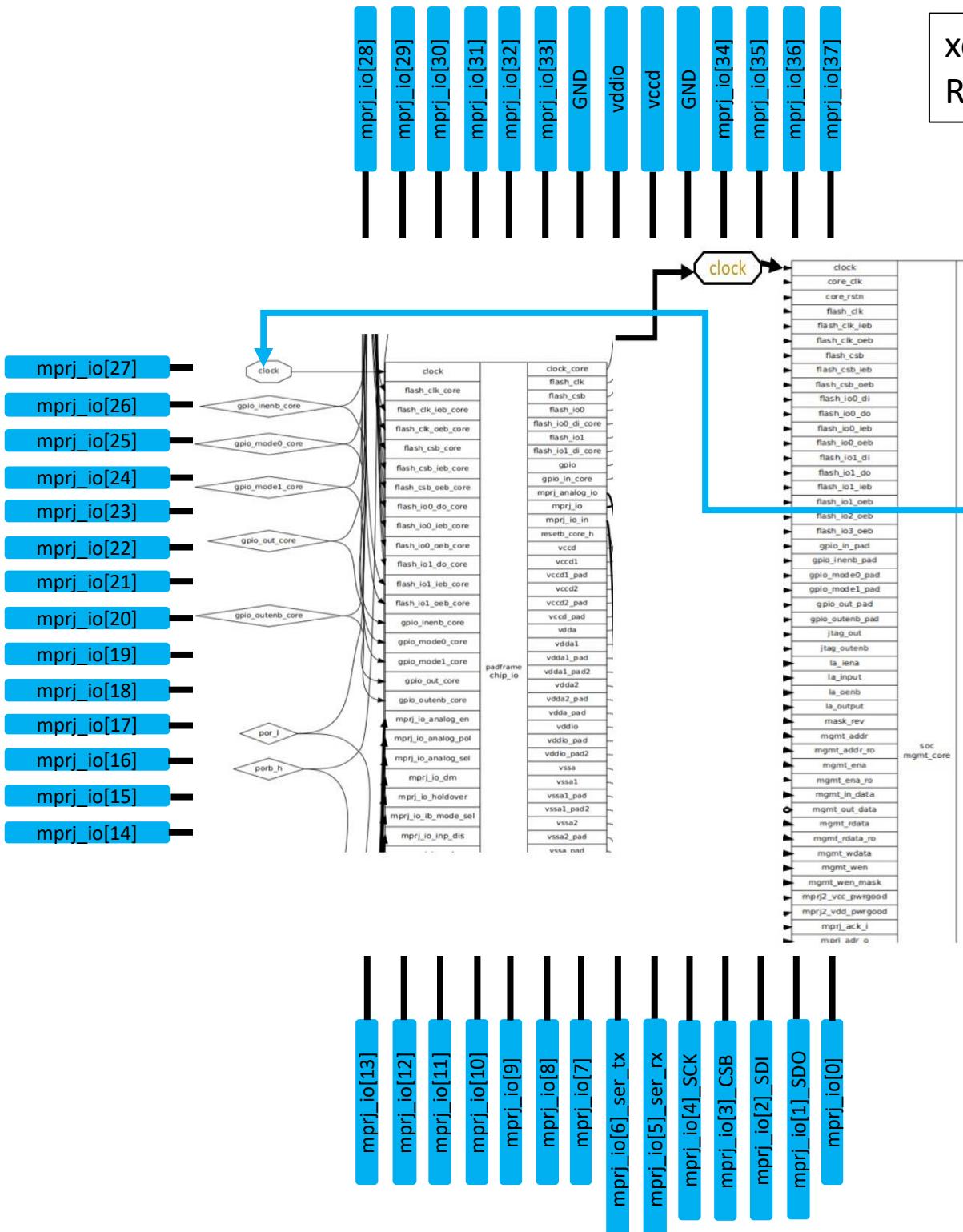
# Board Clock



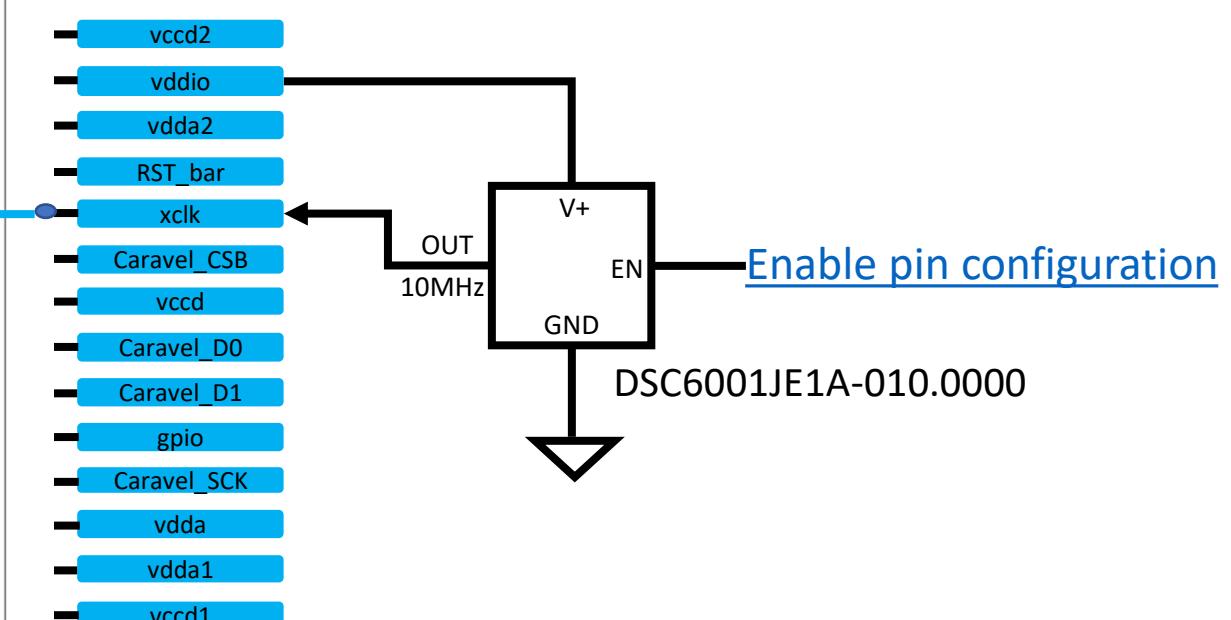
xclk – External CMOS 3.3V clock source, not a crystal  
Recommended Oscillator @10MHz – [DSC6001JE1A-010.0000](#)



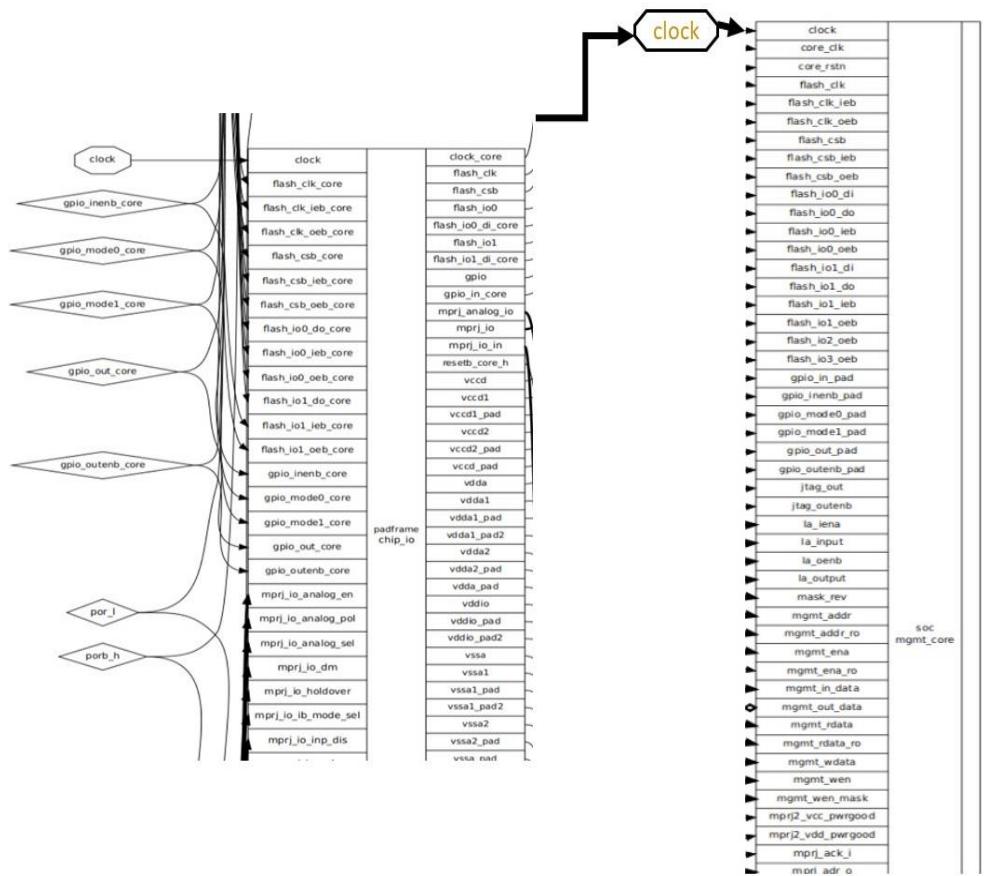
# Board Clock



xclk – External CMOS 3.3V clock source, not a crystal  
Recommended Oscillator @10MHz – **DSC6001JE1A-010.0000**



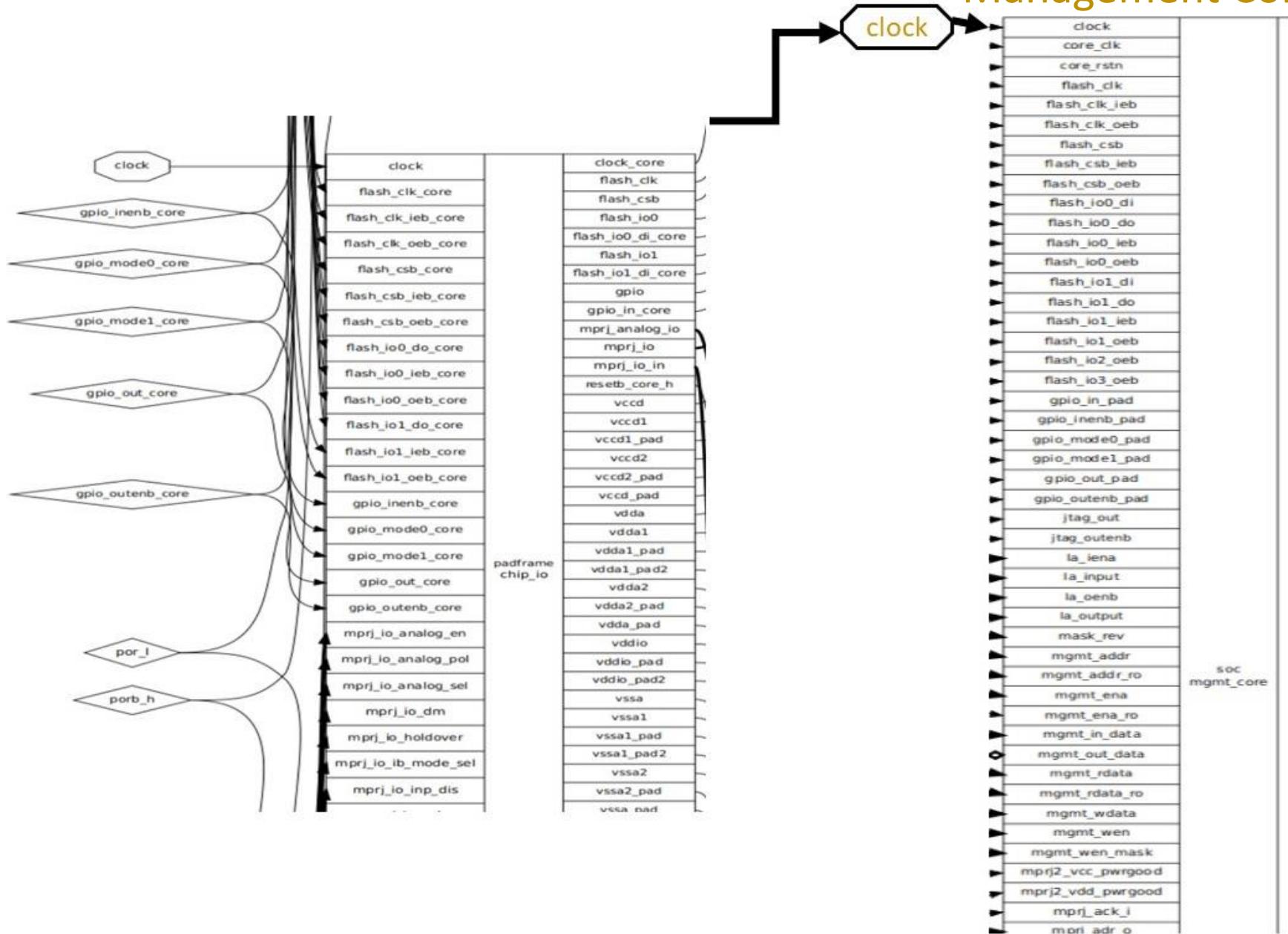
# Board Clock to Core Clock tracing



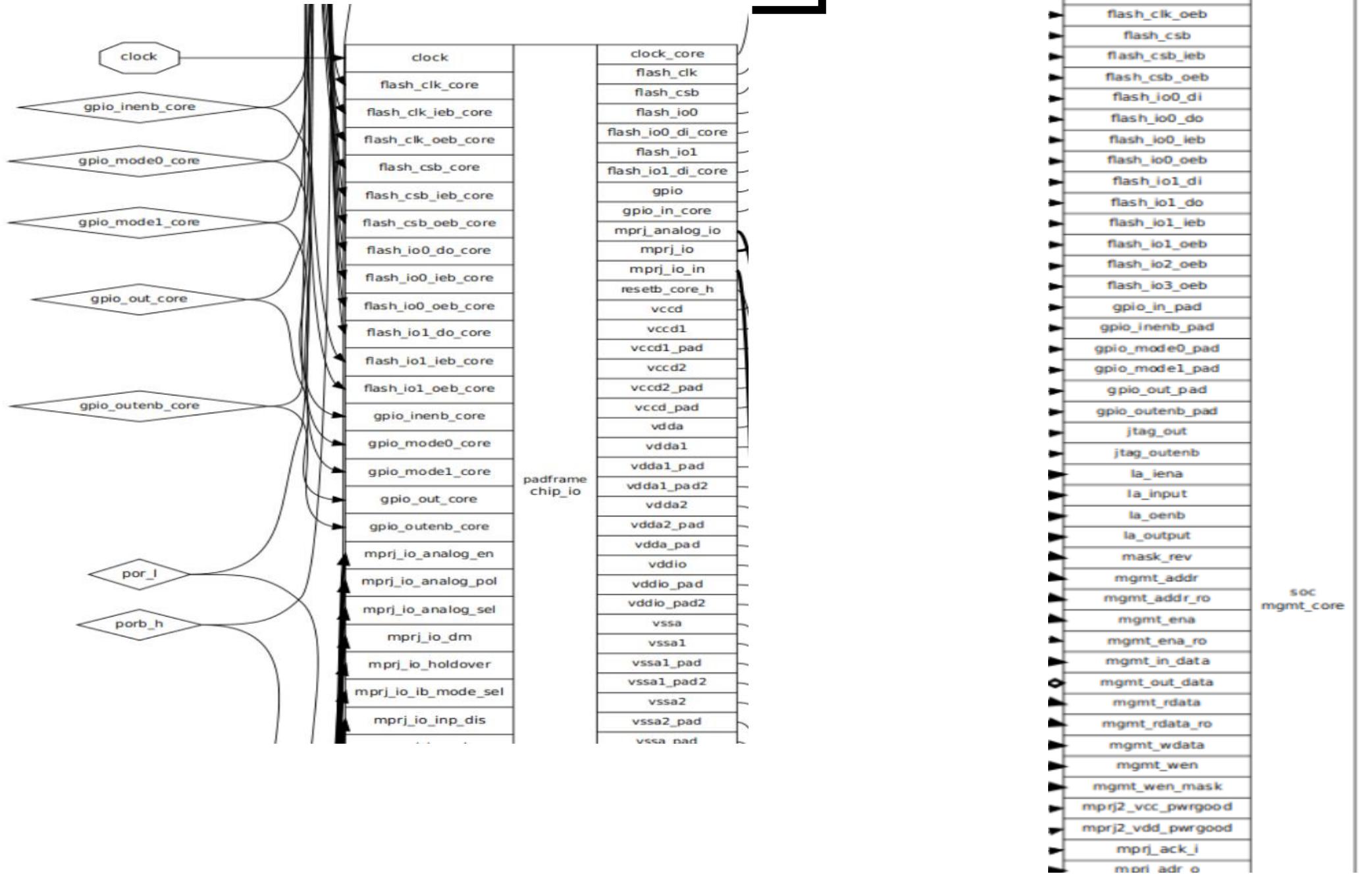
# Core Clock

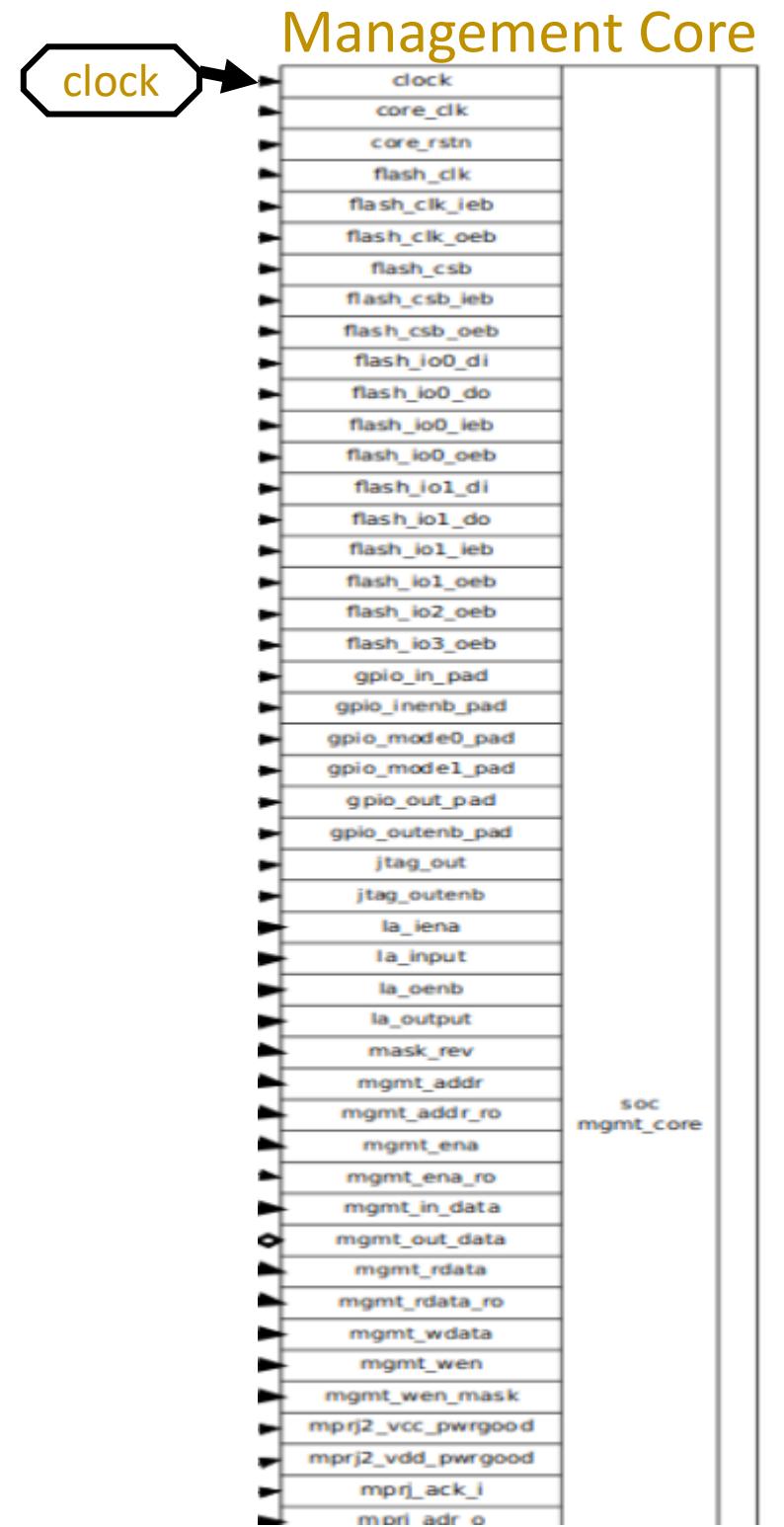
# Caravel Chip

## Management Core



# Core Clock

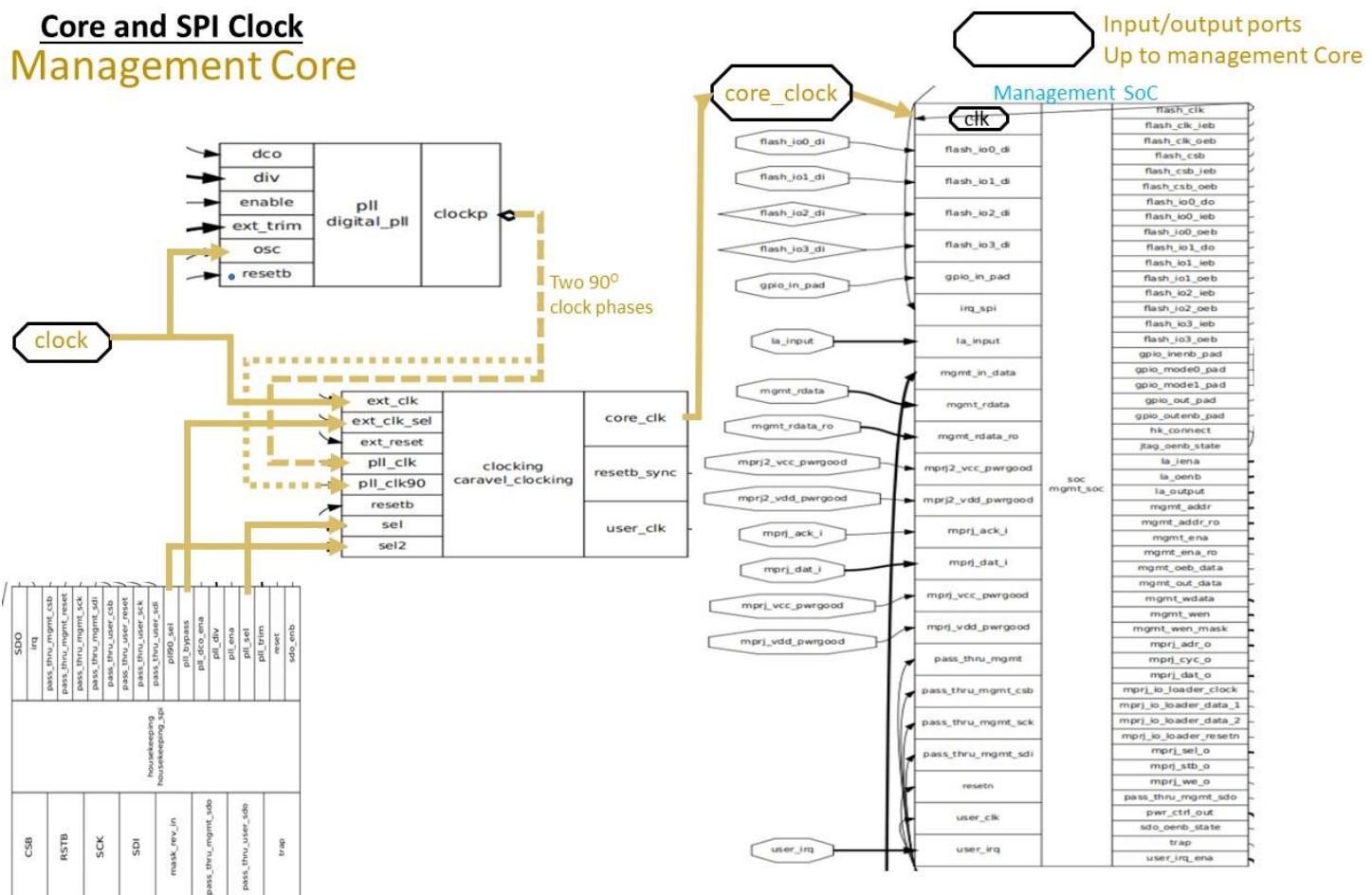




# Core Clock

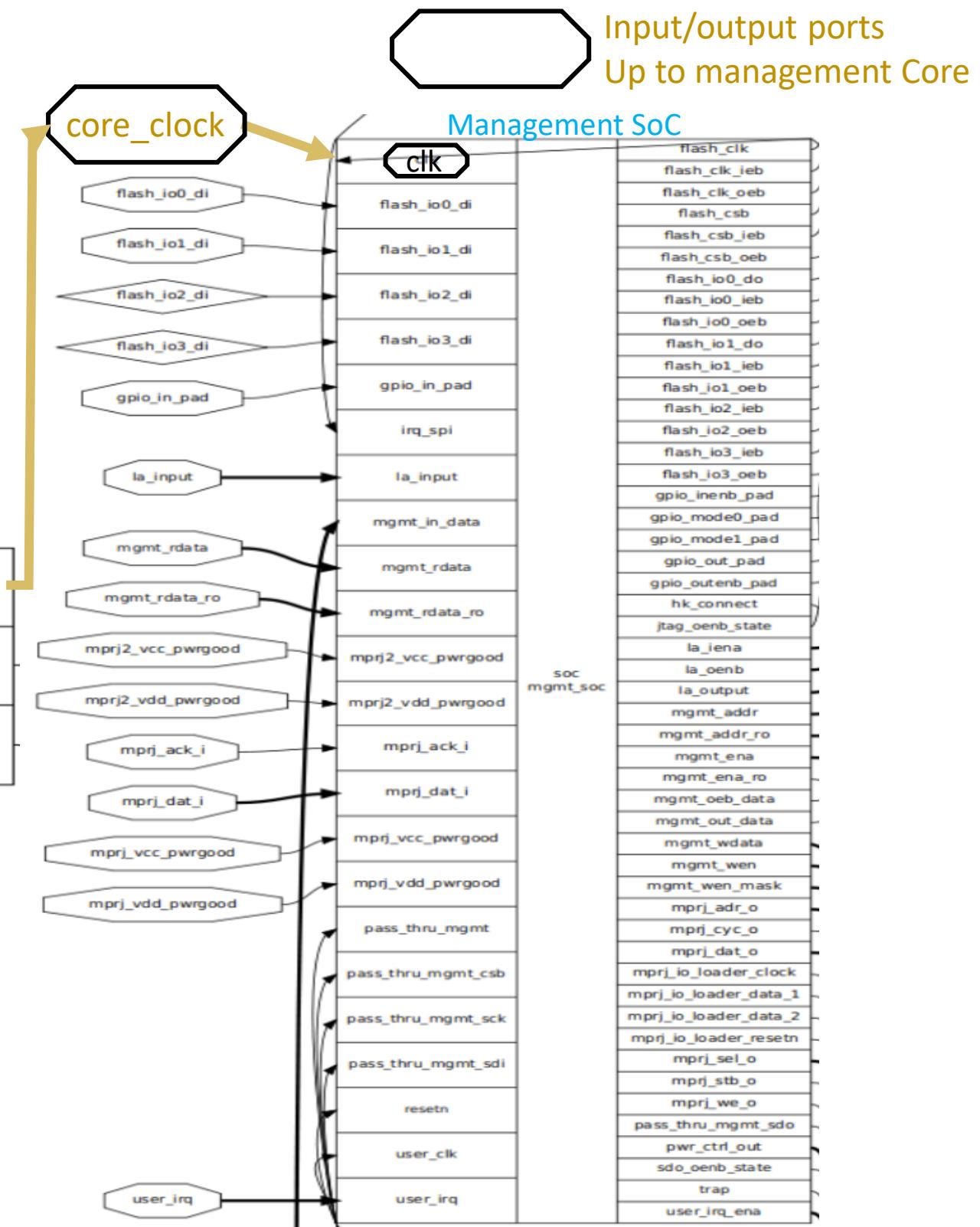
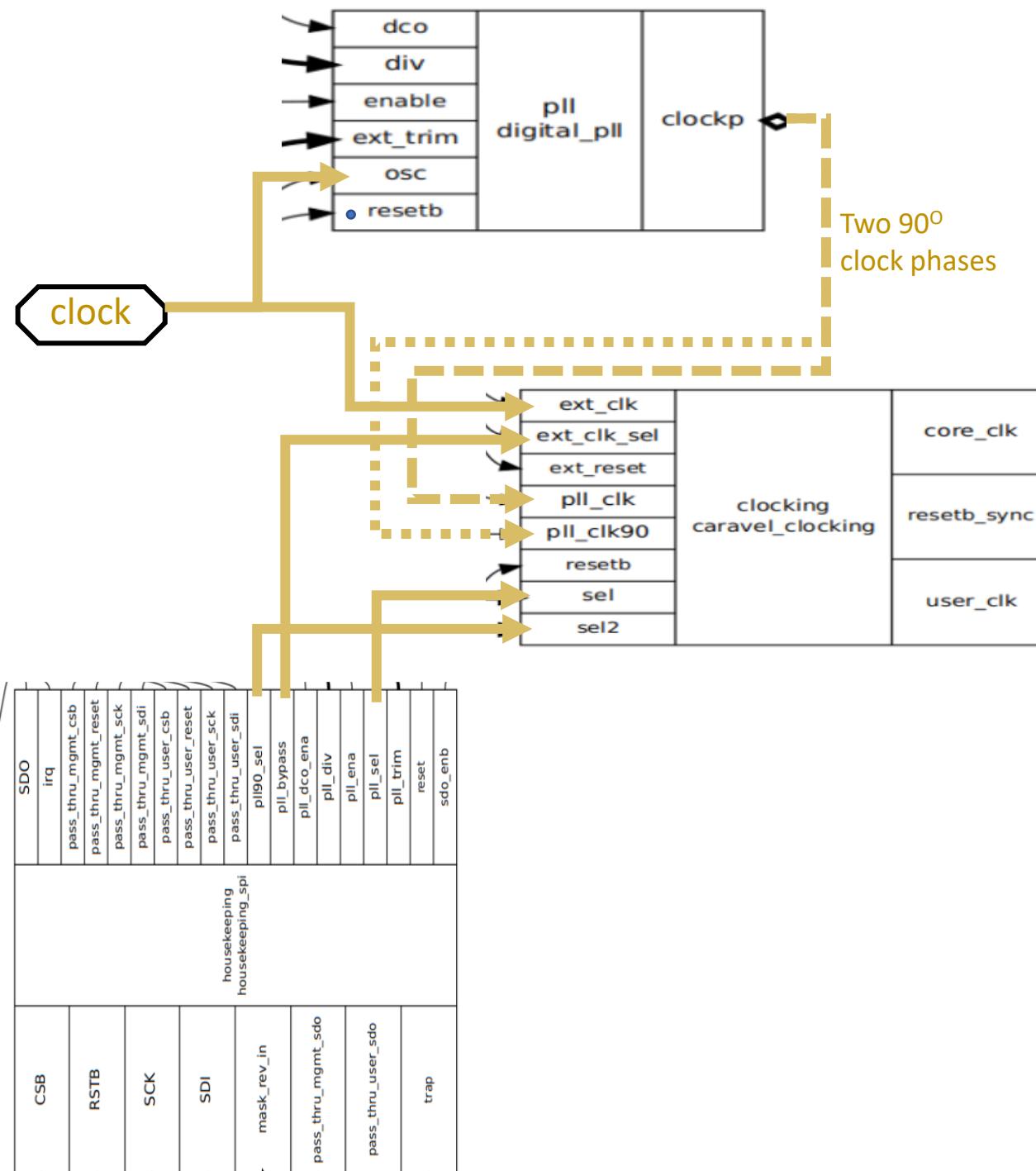
# Caravel Chip

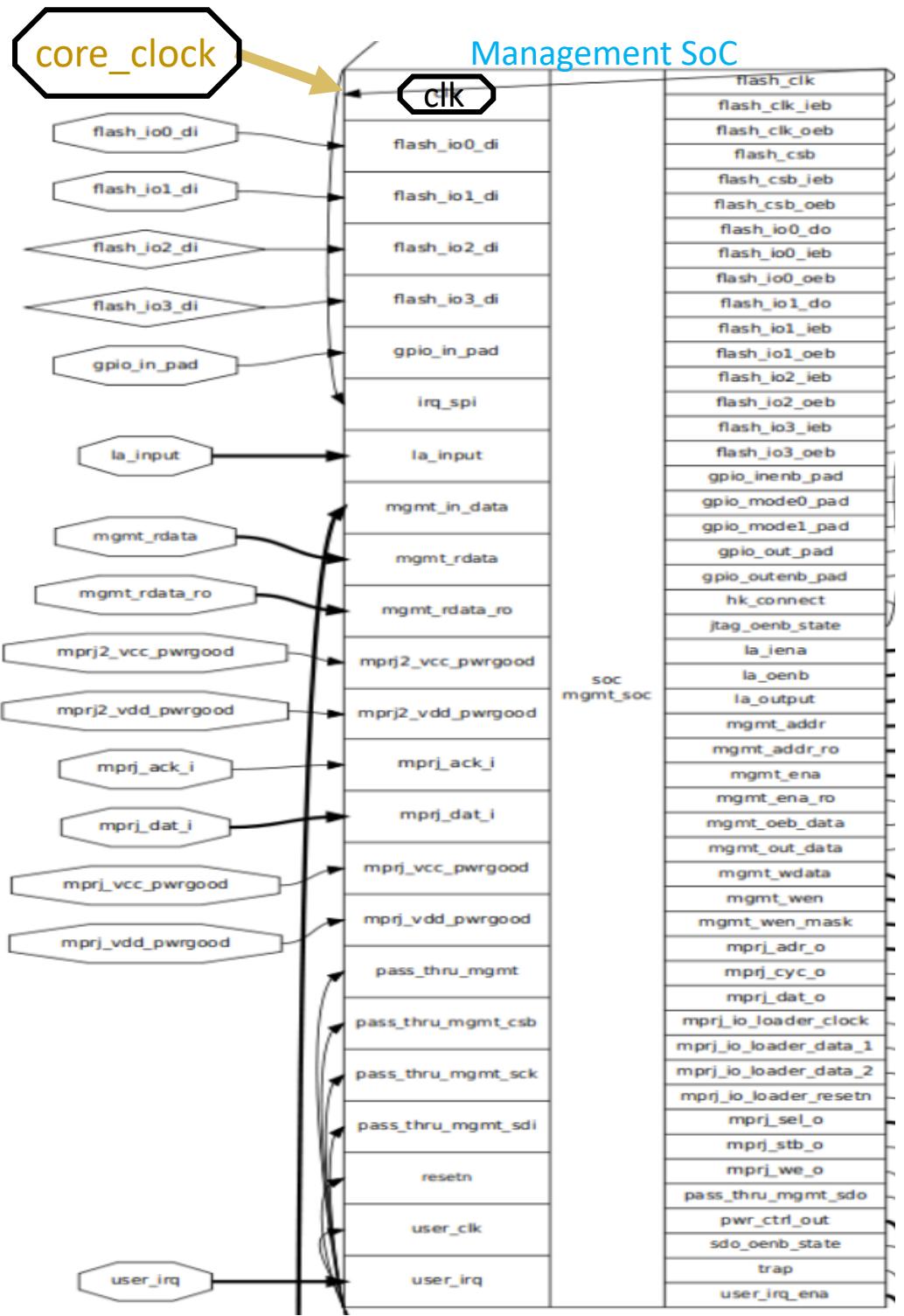
# Management Core



# Core Clock

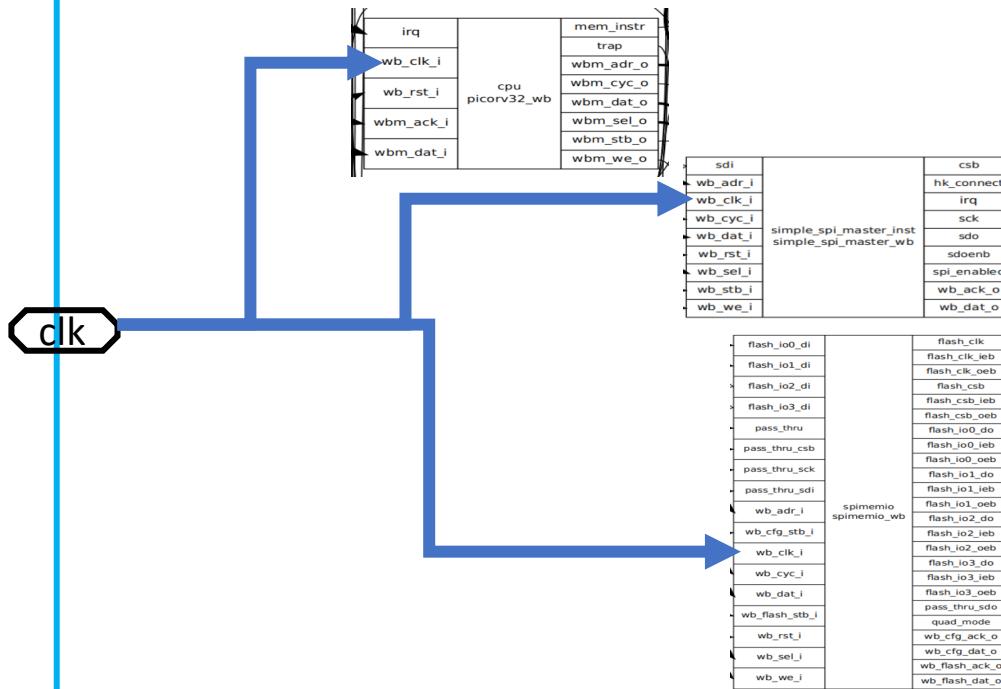
## Management Core





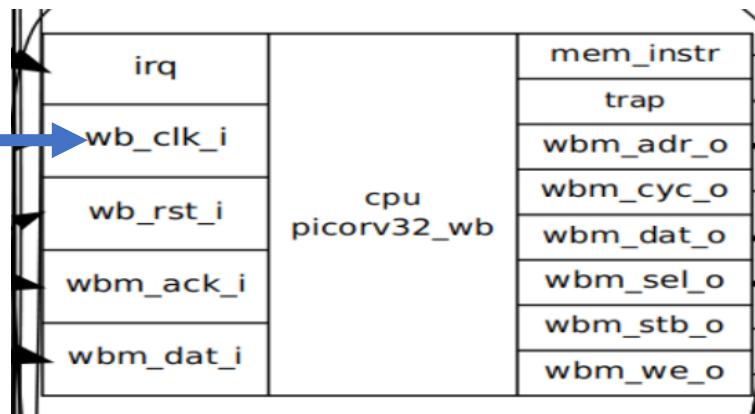
## Management Core

## Management SoC

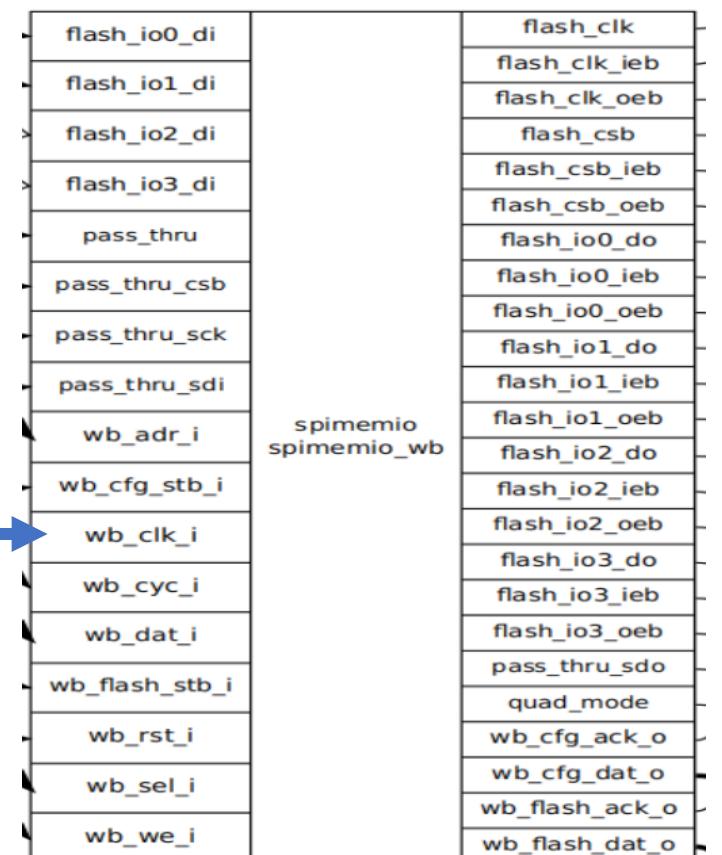


## Core Clock

## Management SoC



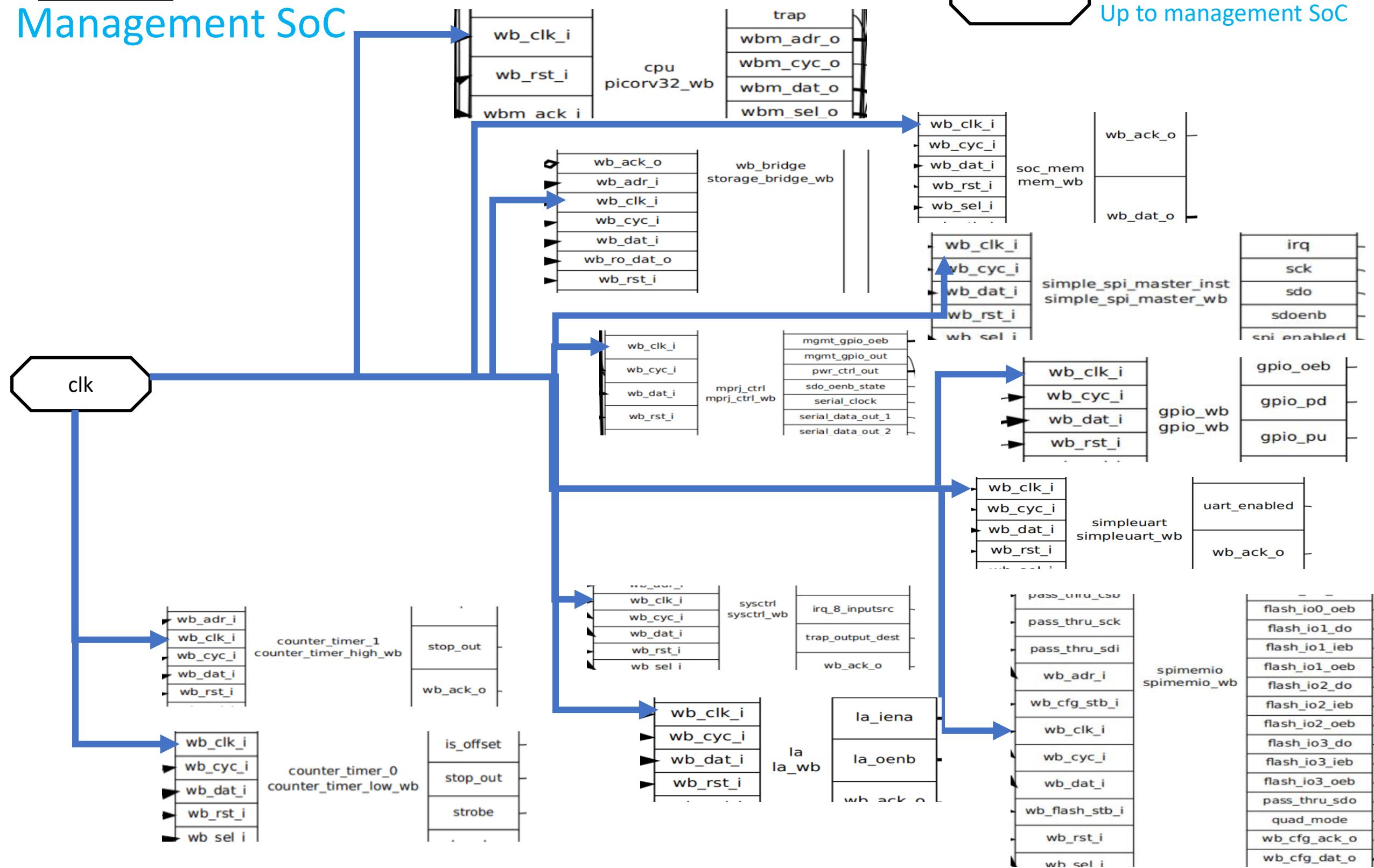
Input/output ports  
Up to management SoC



# Full Clock

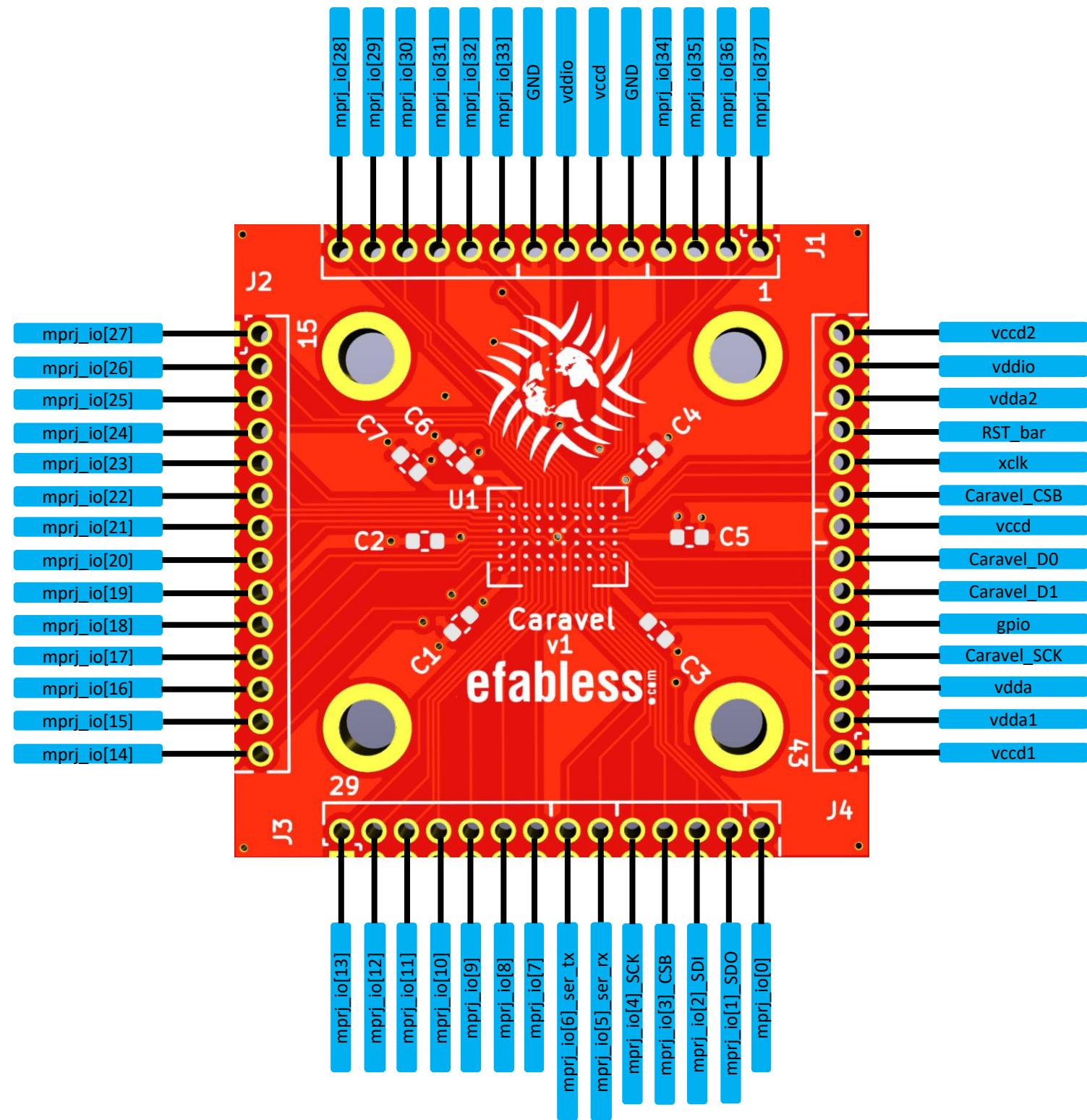
## Management SoC

Input/output ports  
Up to management SoC

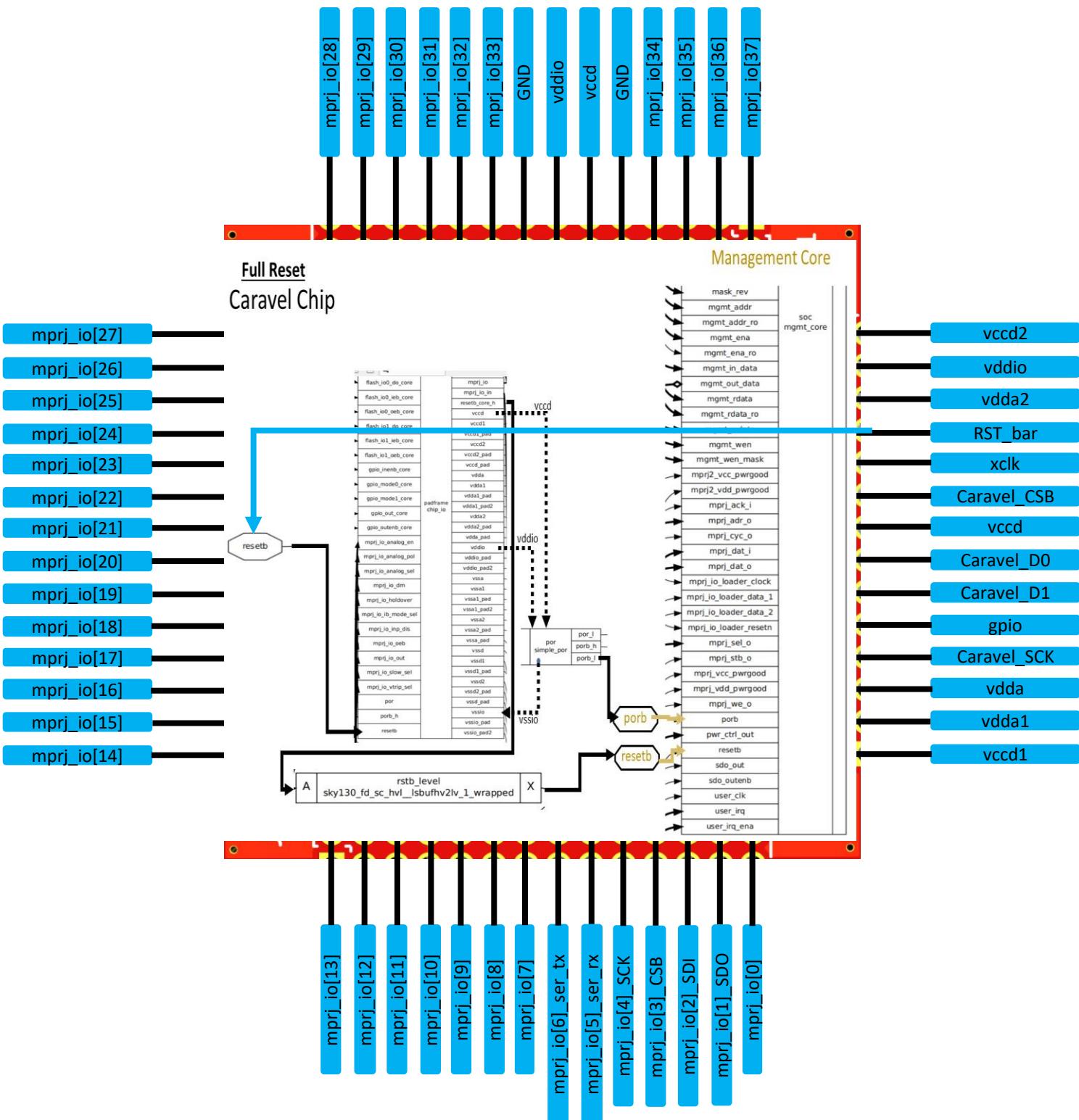


**Board Reset**

# Board Reset

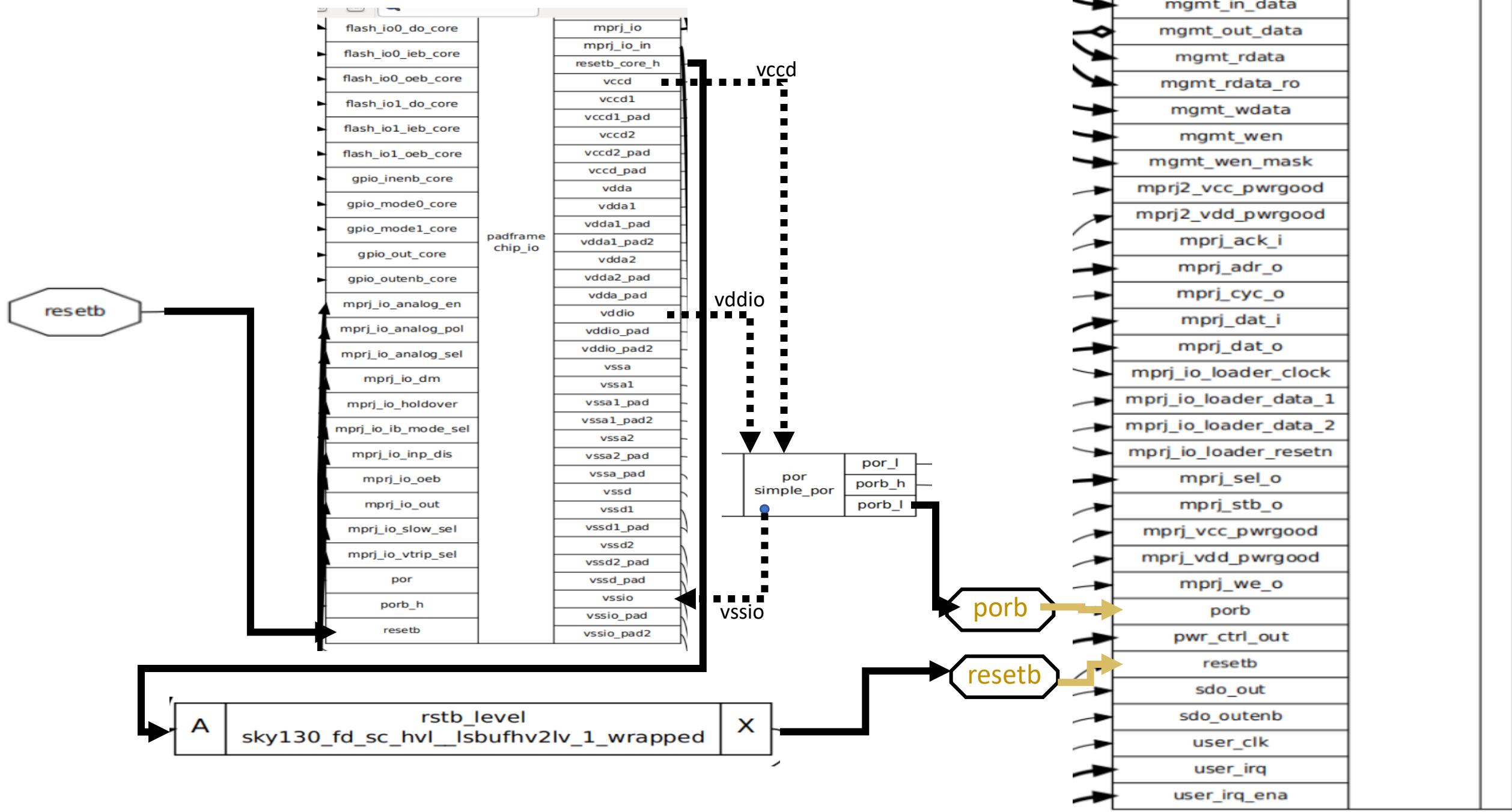


# Board Reset



Full Reset

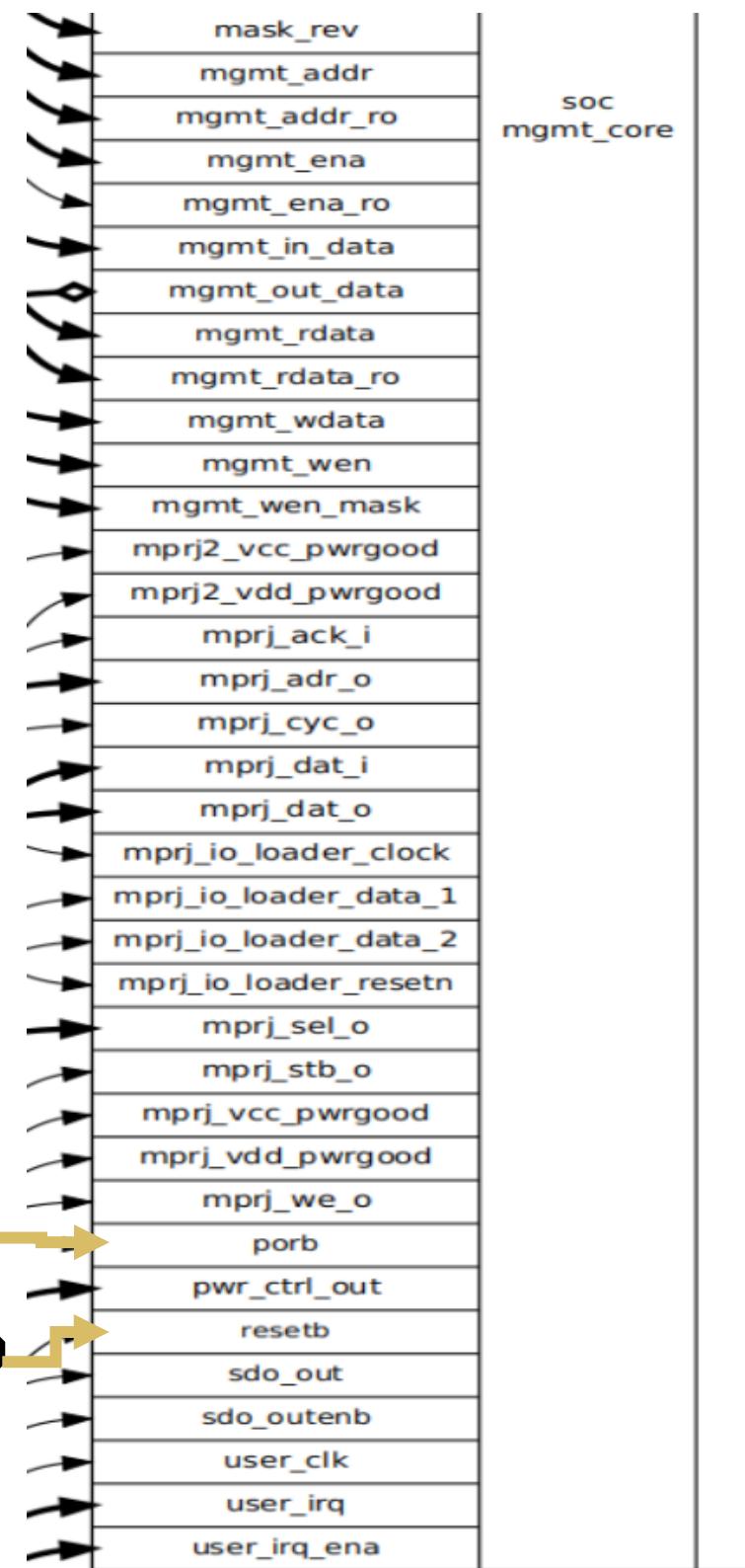
## Caravel Chip



# Management Core

Full Reset

Caravel Chip

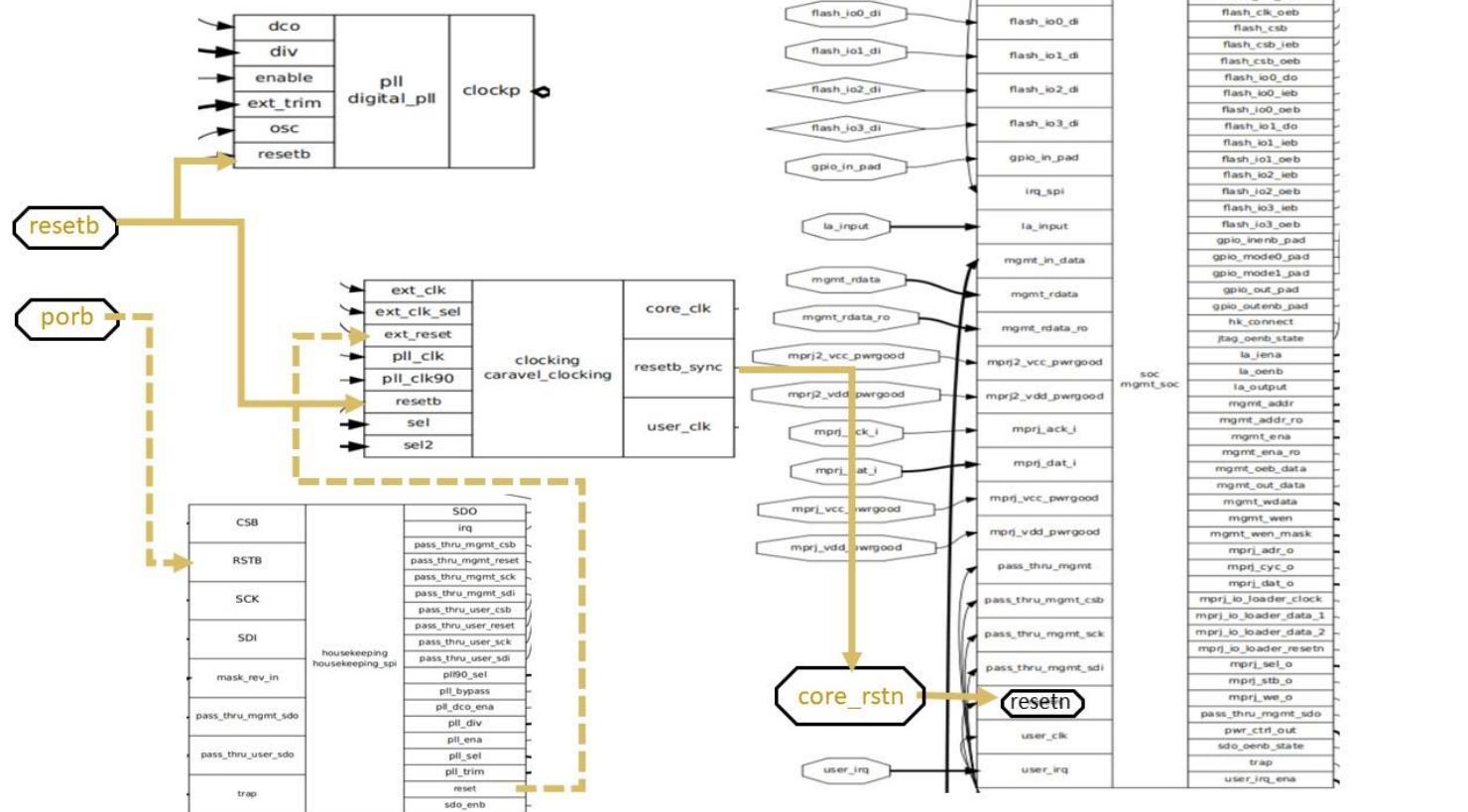


# Full Reset

# Caravel Chip

## Management Core

### Full Reset Management Core

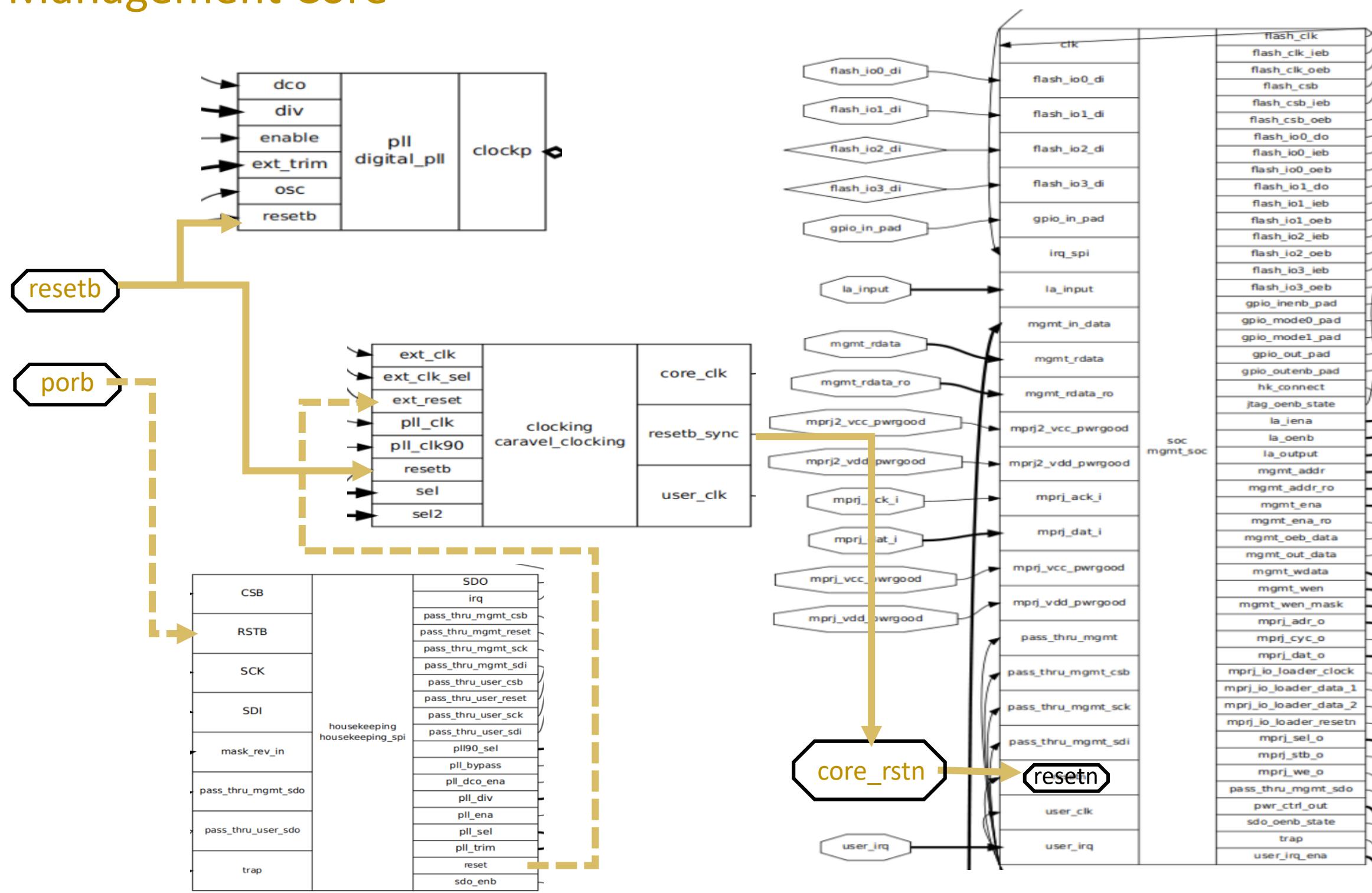


# Full Reset

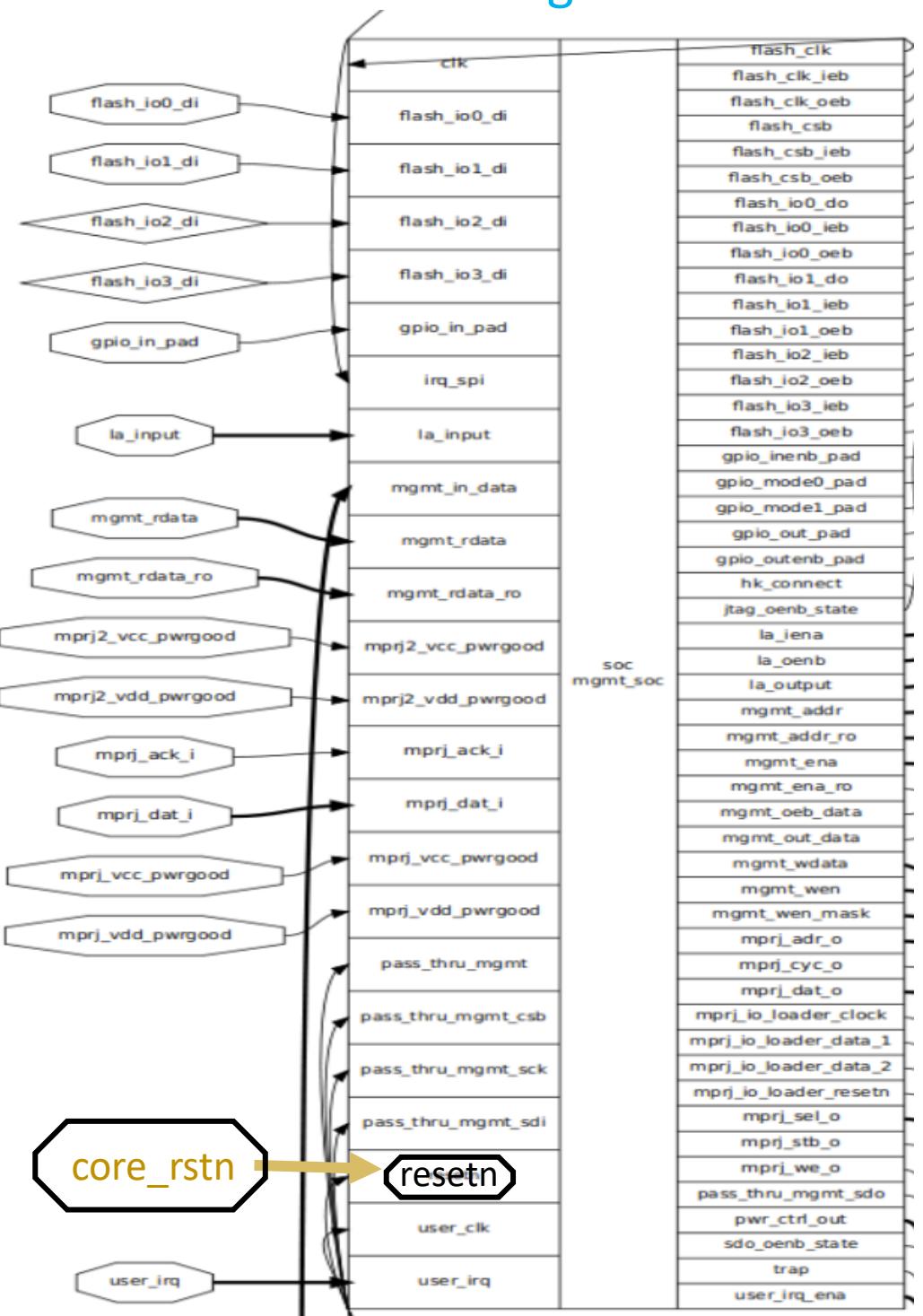
## Management Core

Input/output ports

Up to management Core



# Management SoC



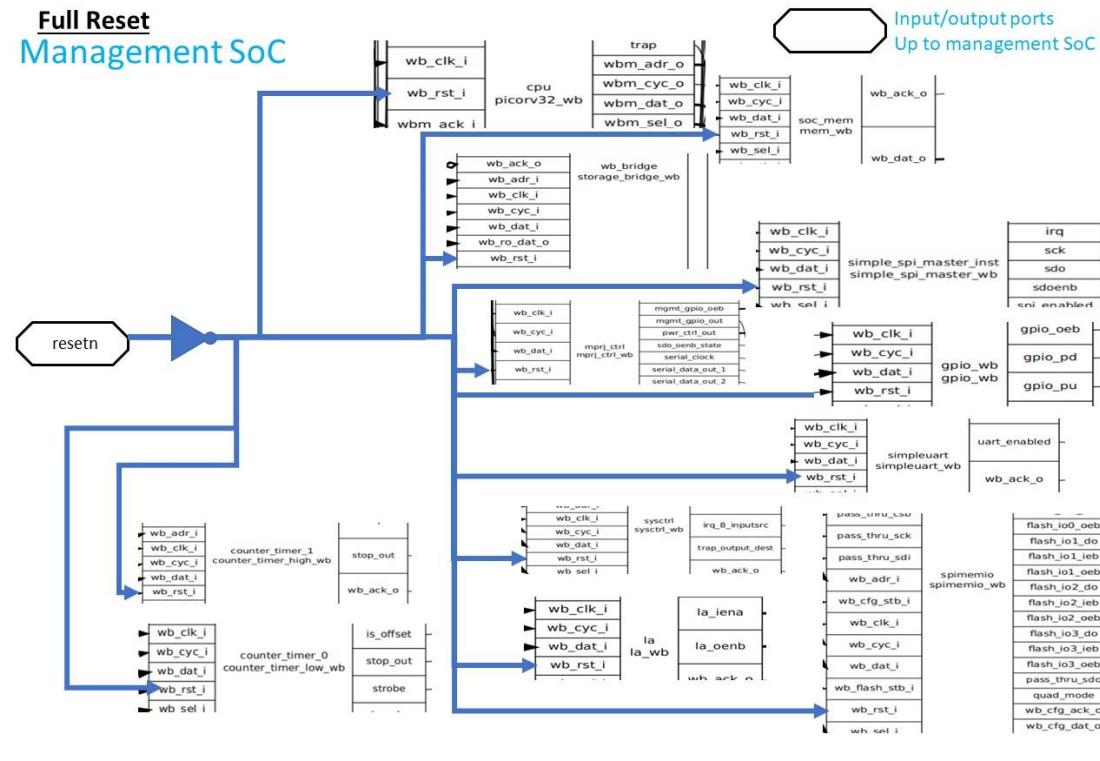
Full Reset

Management SoC

Caravel Chip

## Management Core

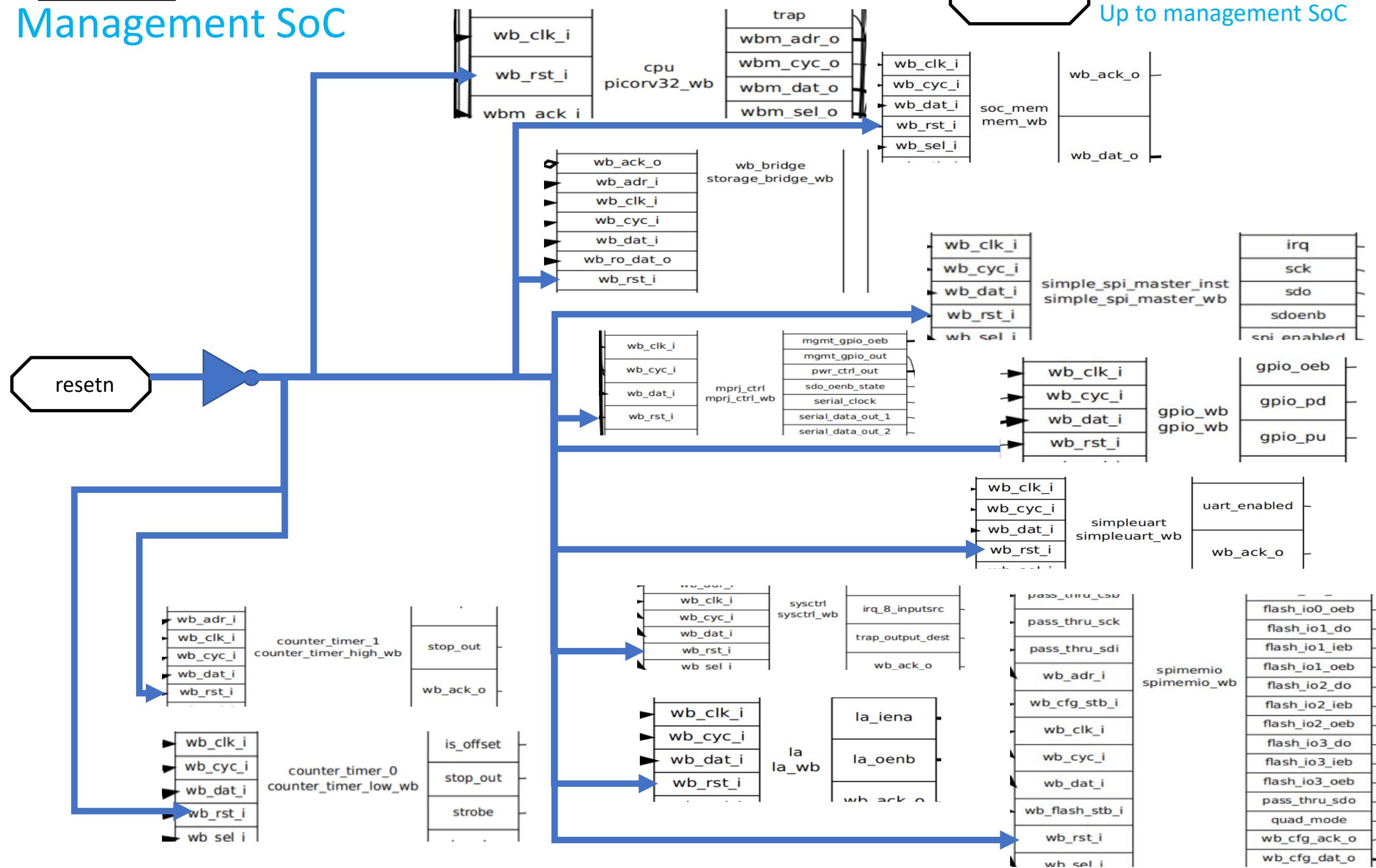
### Management SoC



# Full Reset

## Management SoC

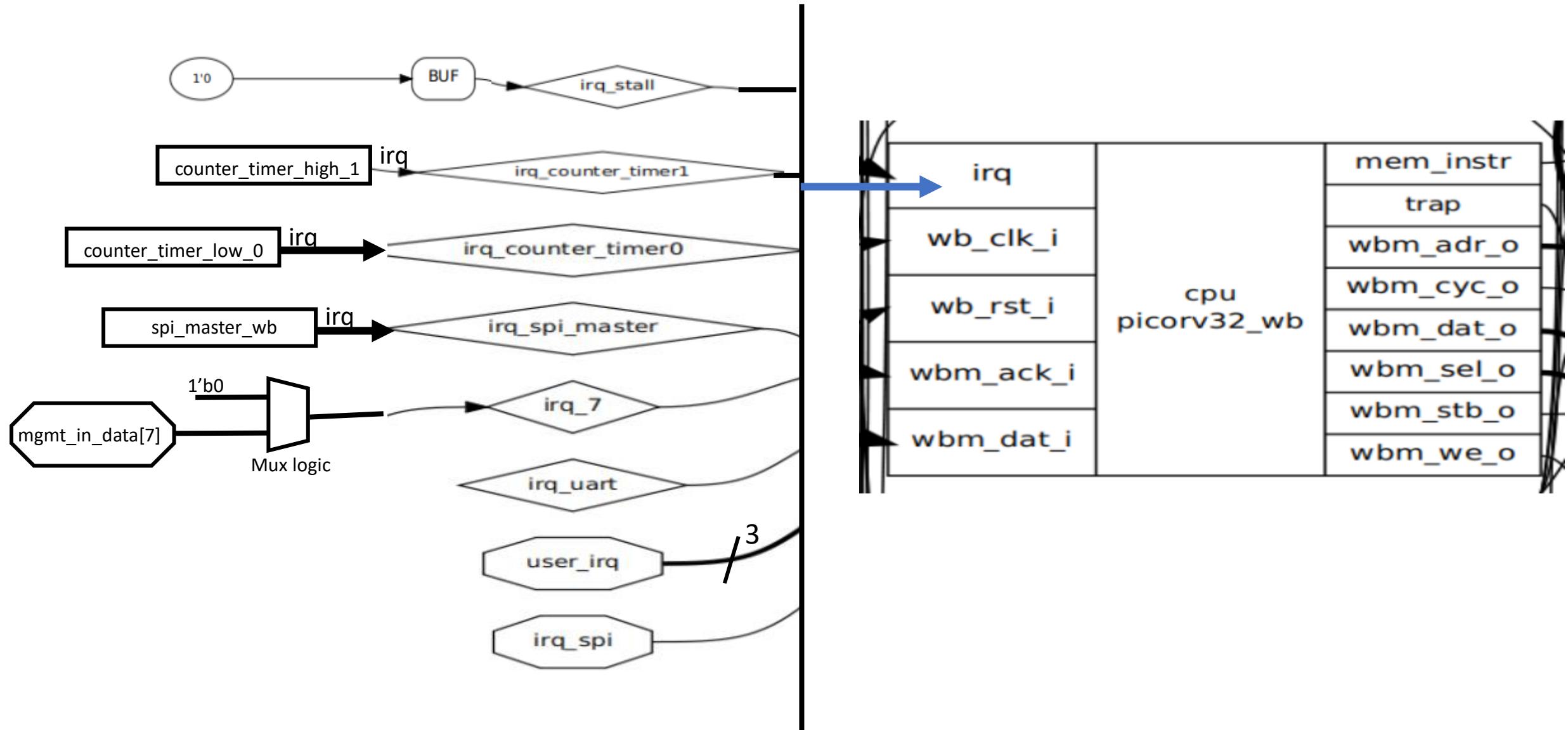
Input/output ports  
Up to management SoC



# IRQ connections

## Management SoC

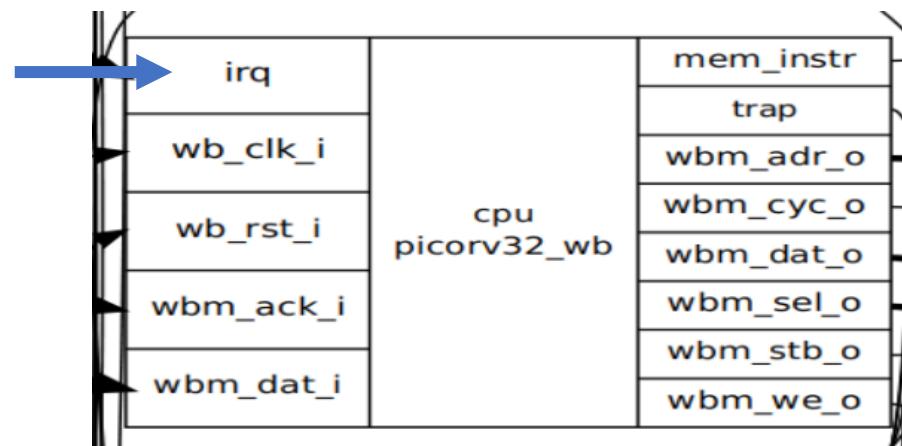
Input/output ports  
Up to management SoC



# Caravel Chip

Management Core

Management SoC

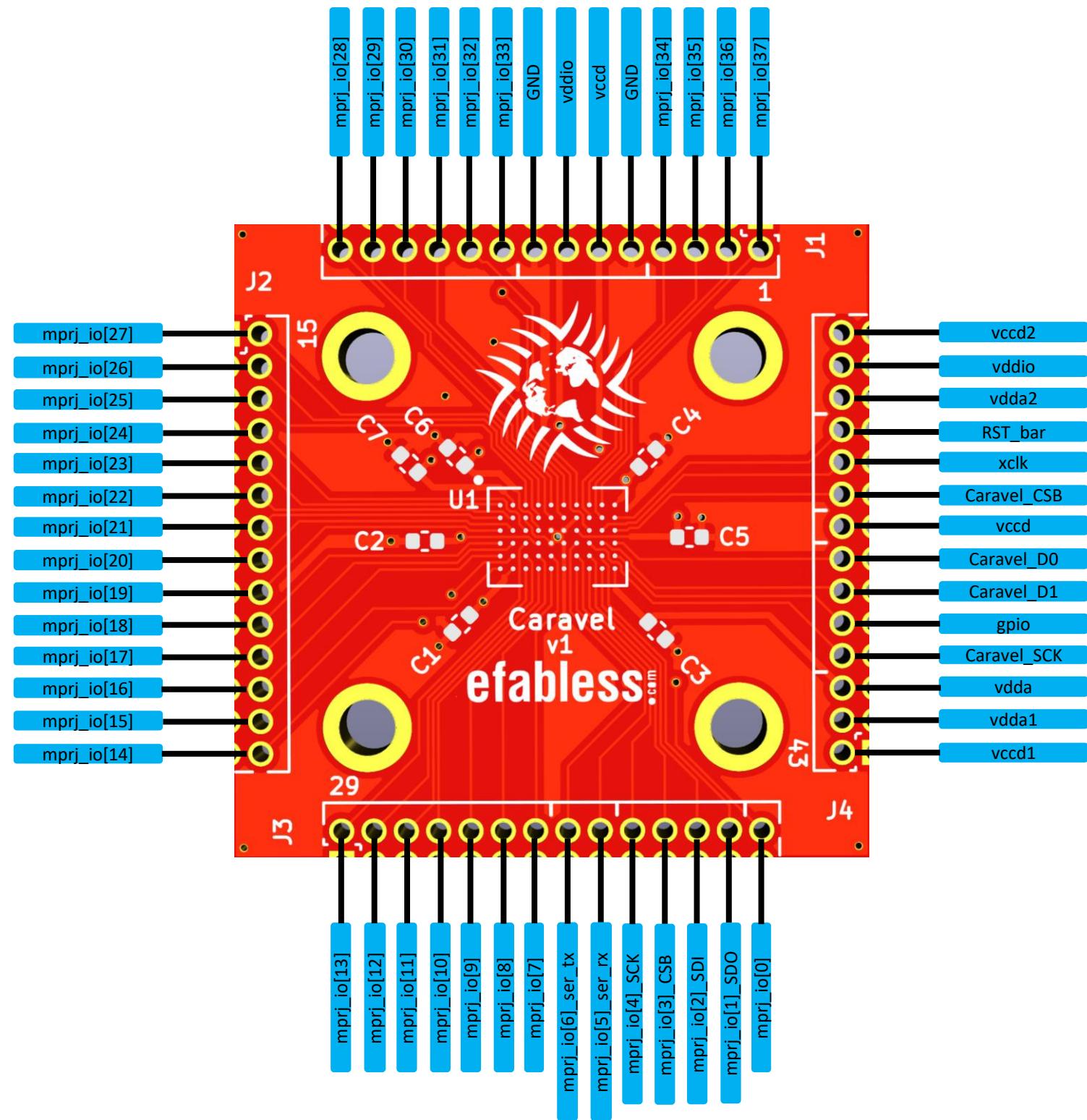


# Board Flash

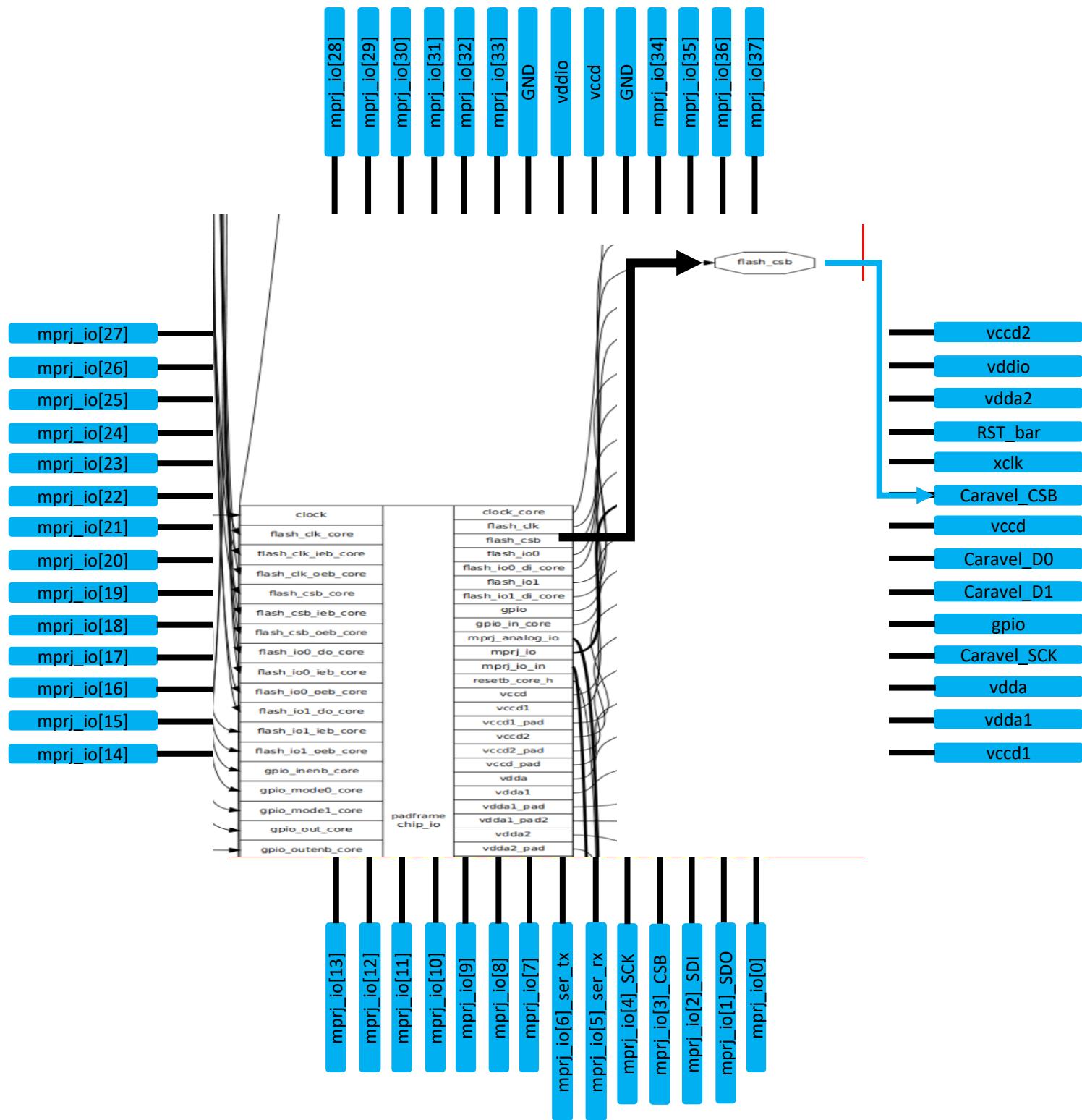
# 1. Flash CSB

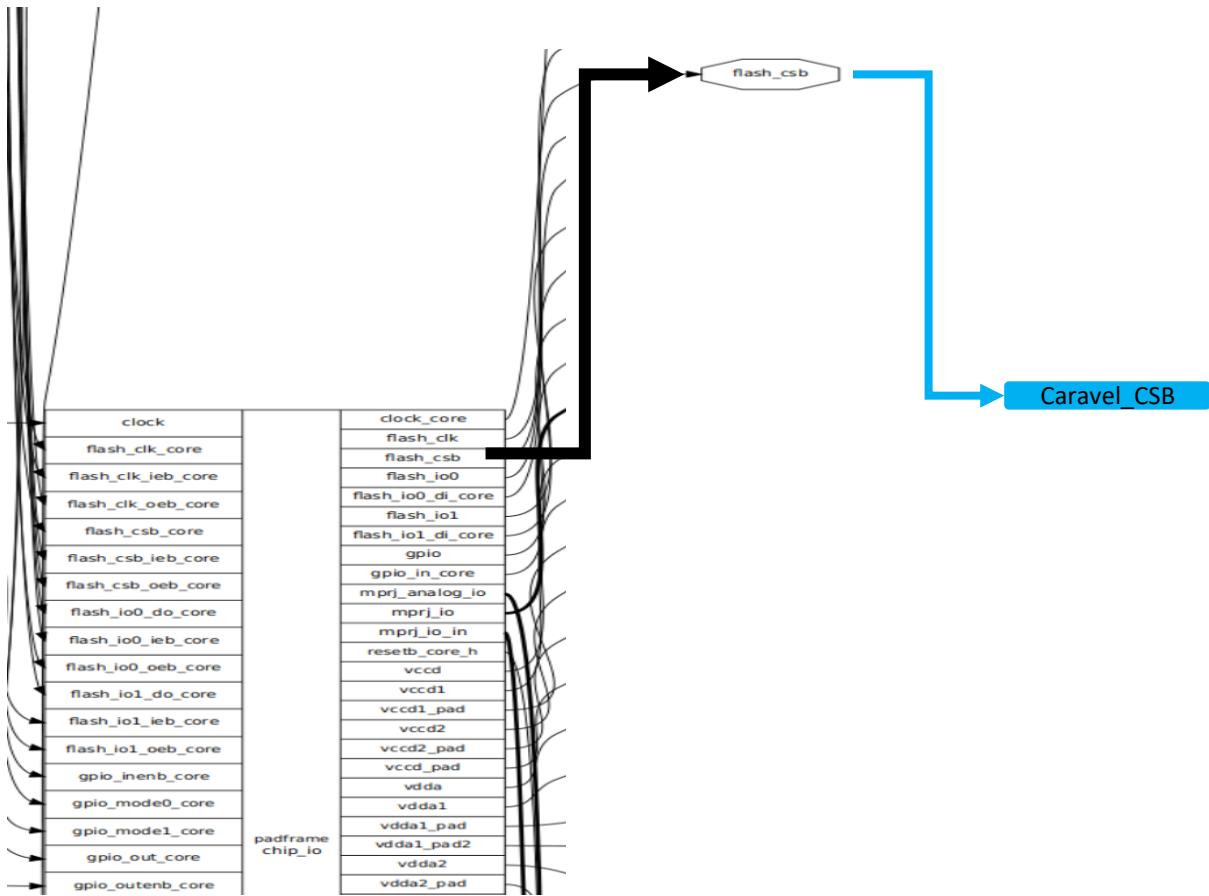
SPI flash controller chip select (sense inverted)

# Board Reset

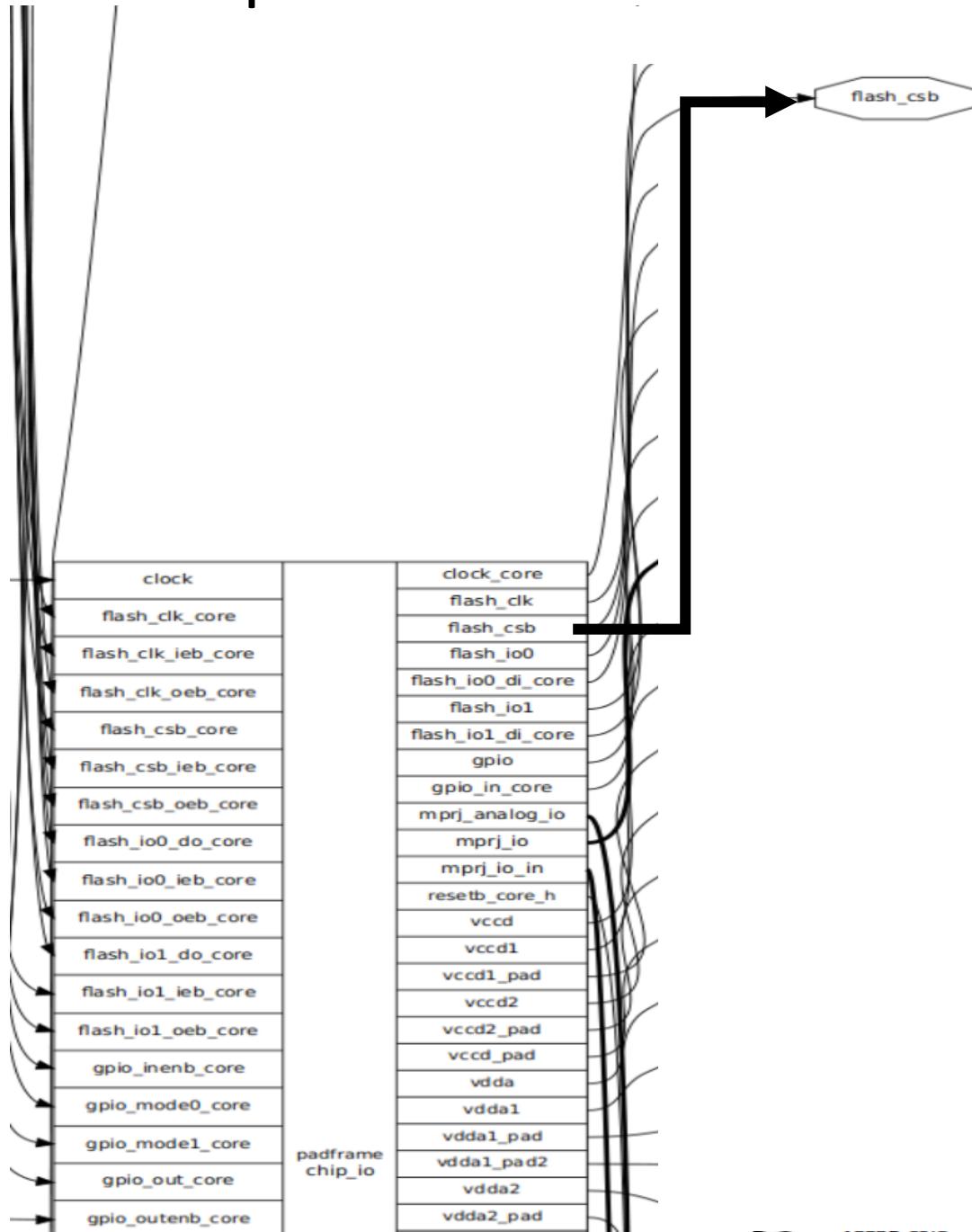


# Board Reset

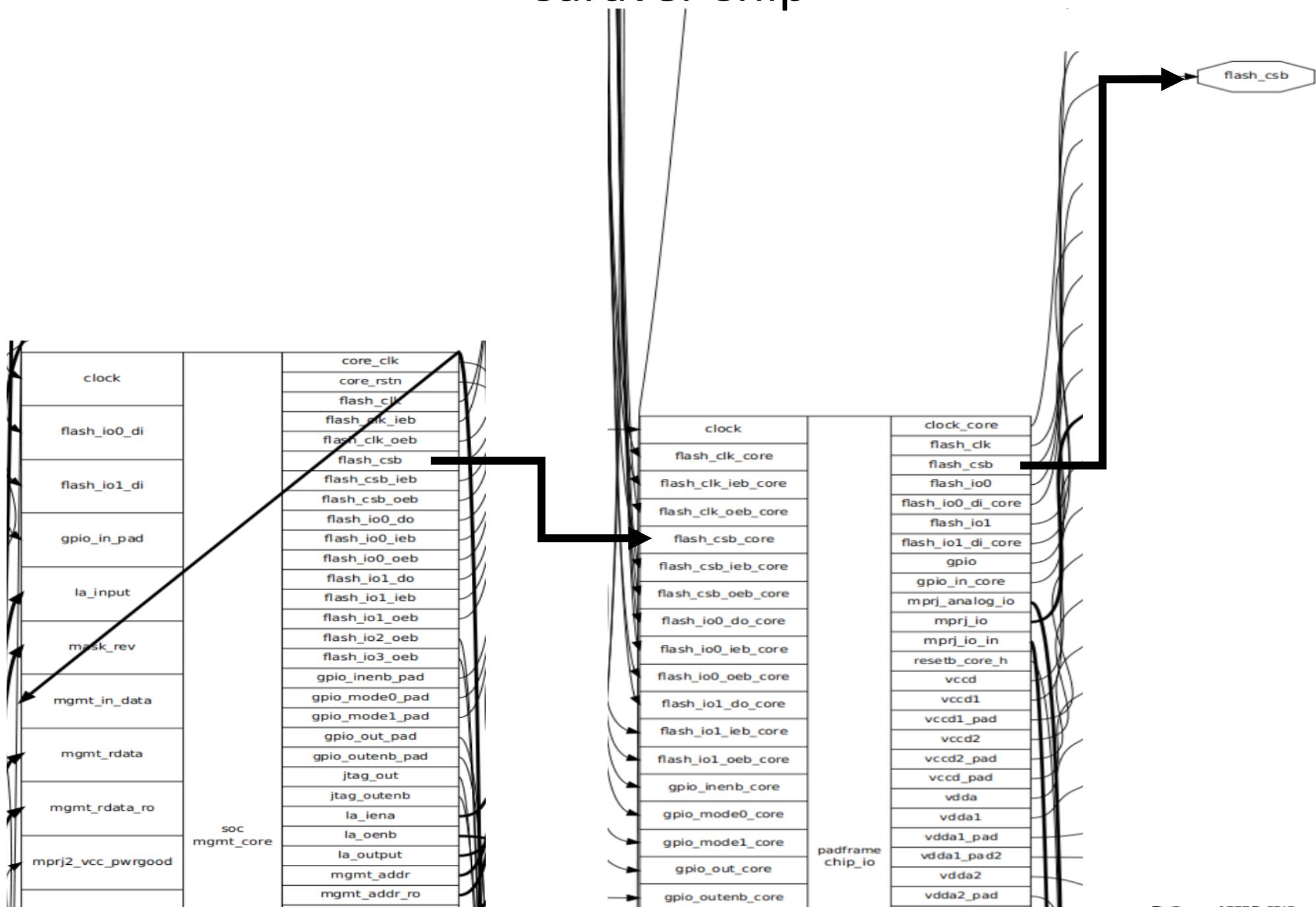




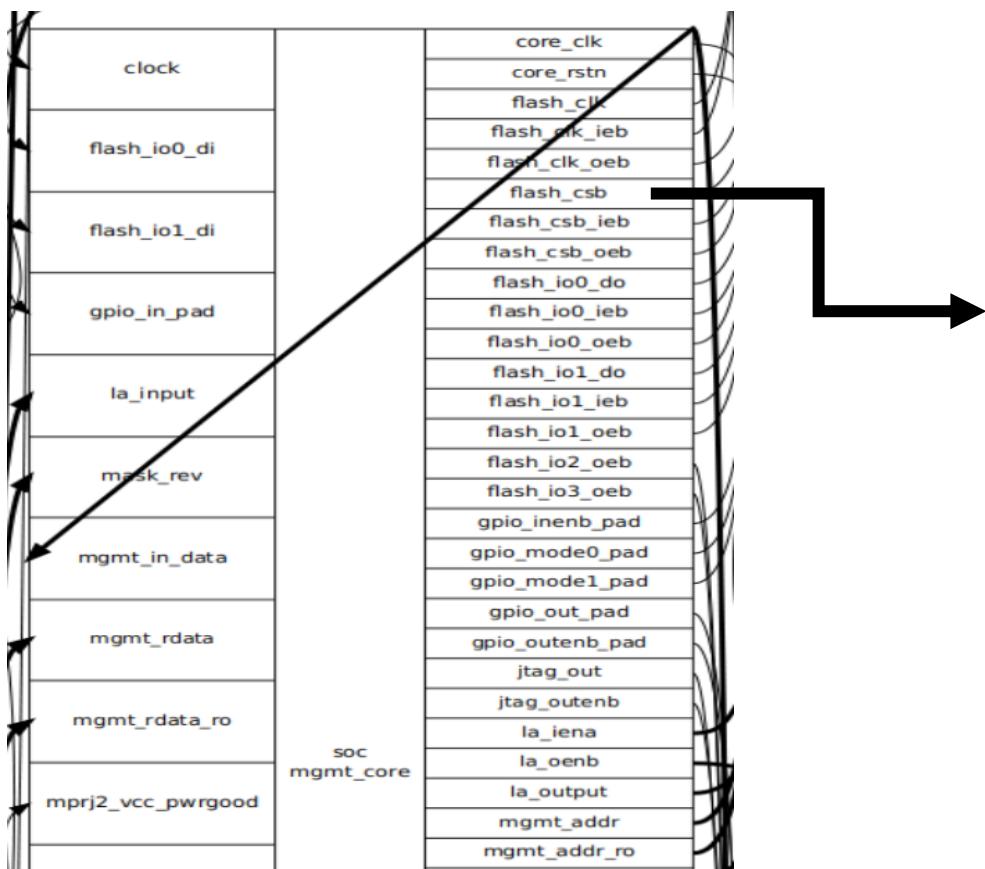
# Caravel Chip



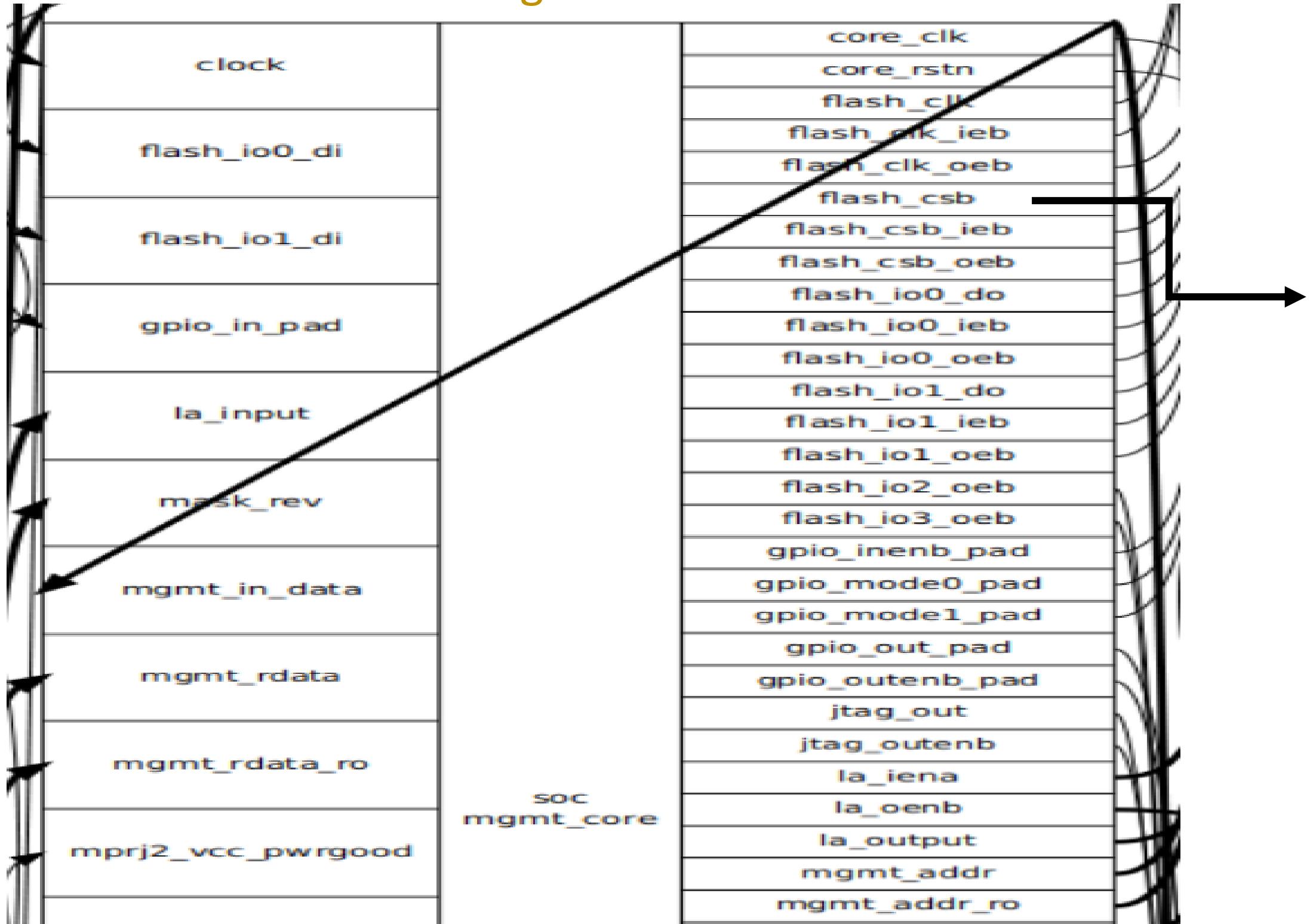
# Caravel Chip



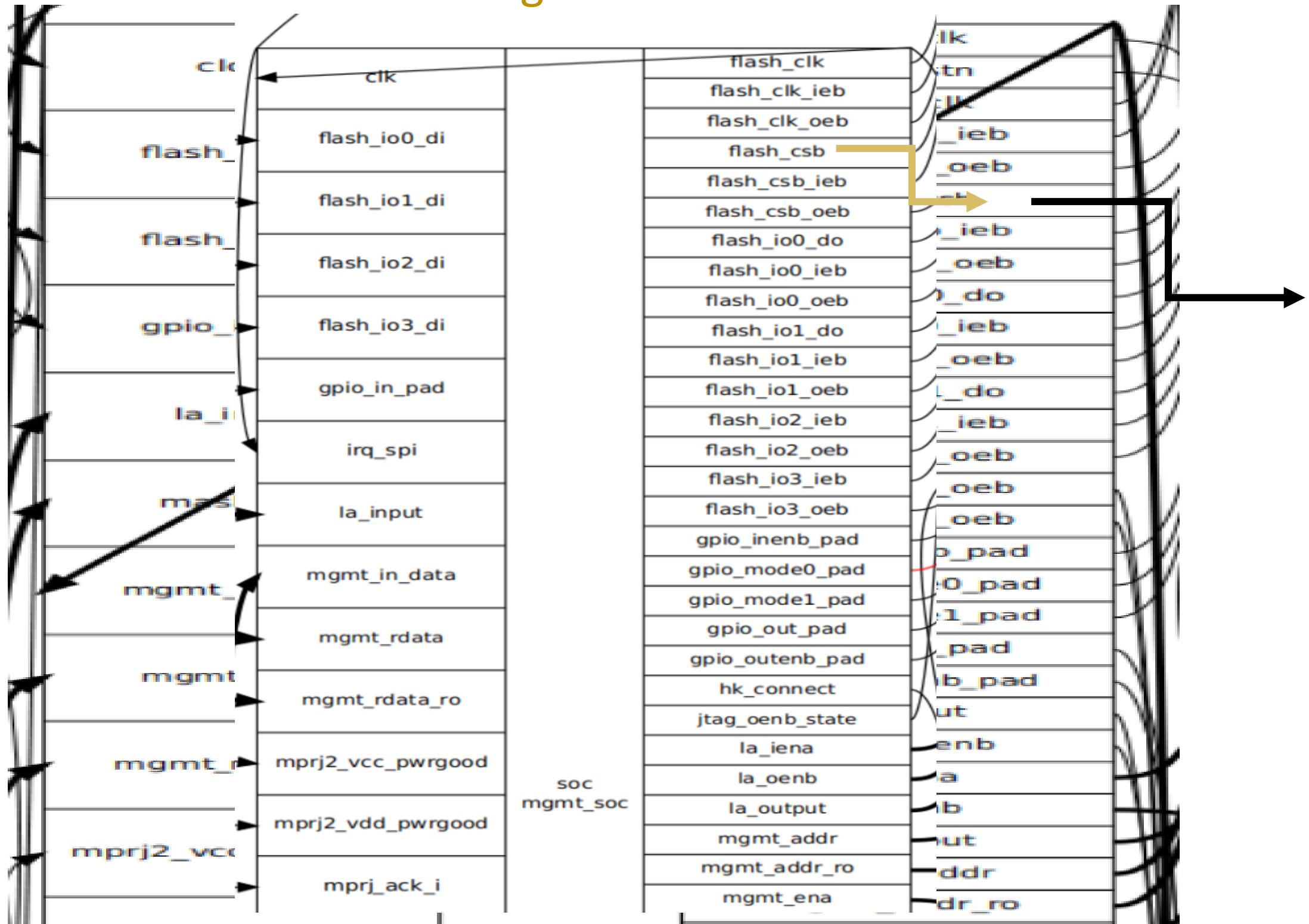
# Management Core



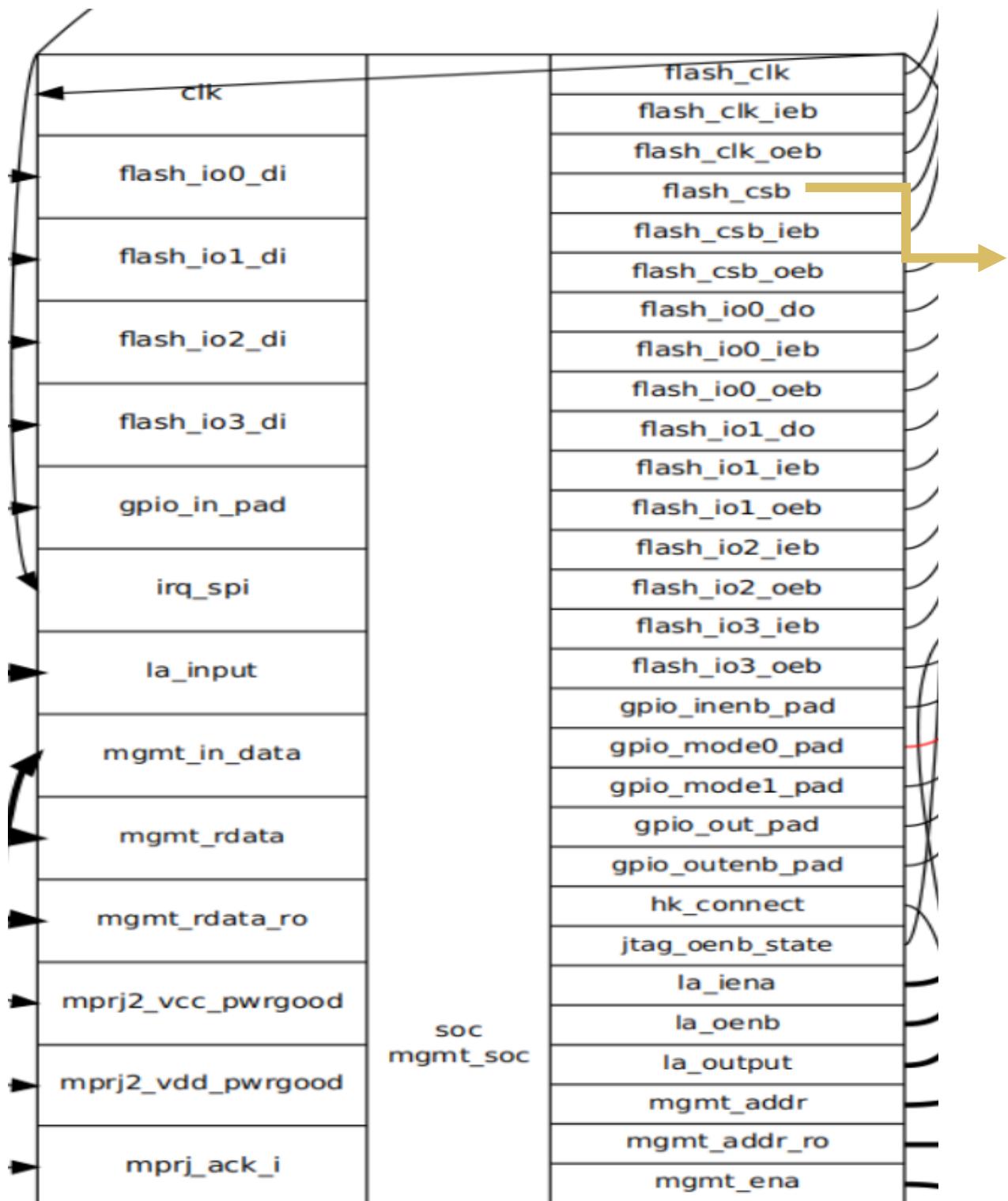
# Management Core



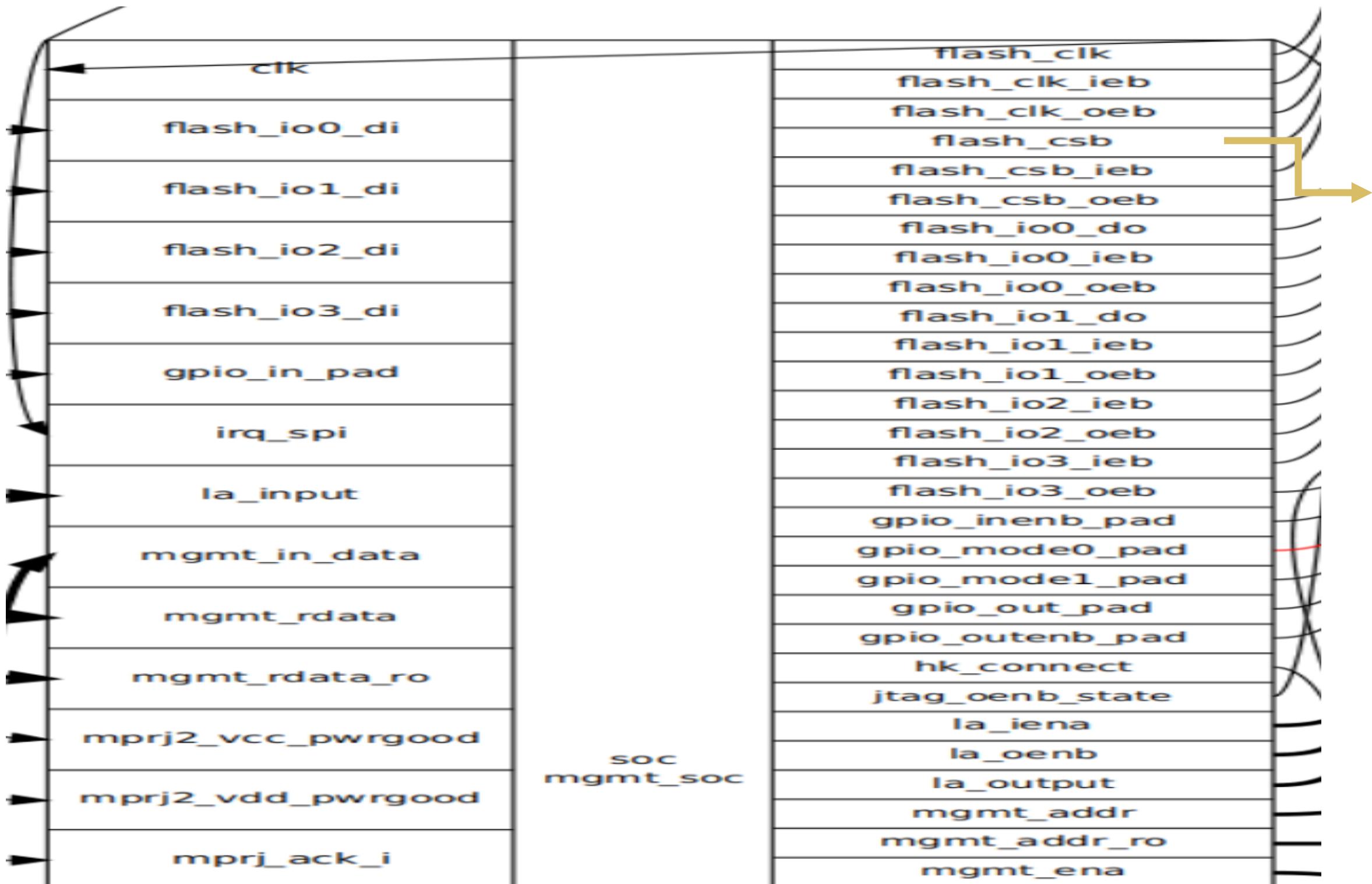
# Management Core



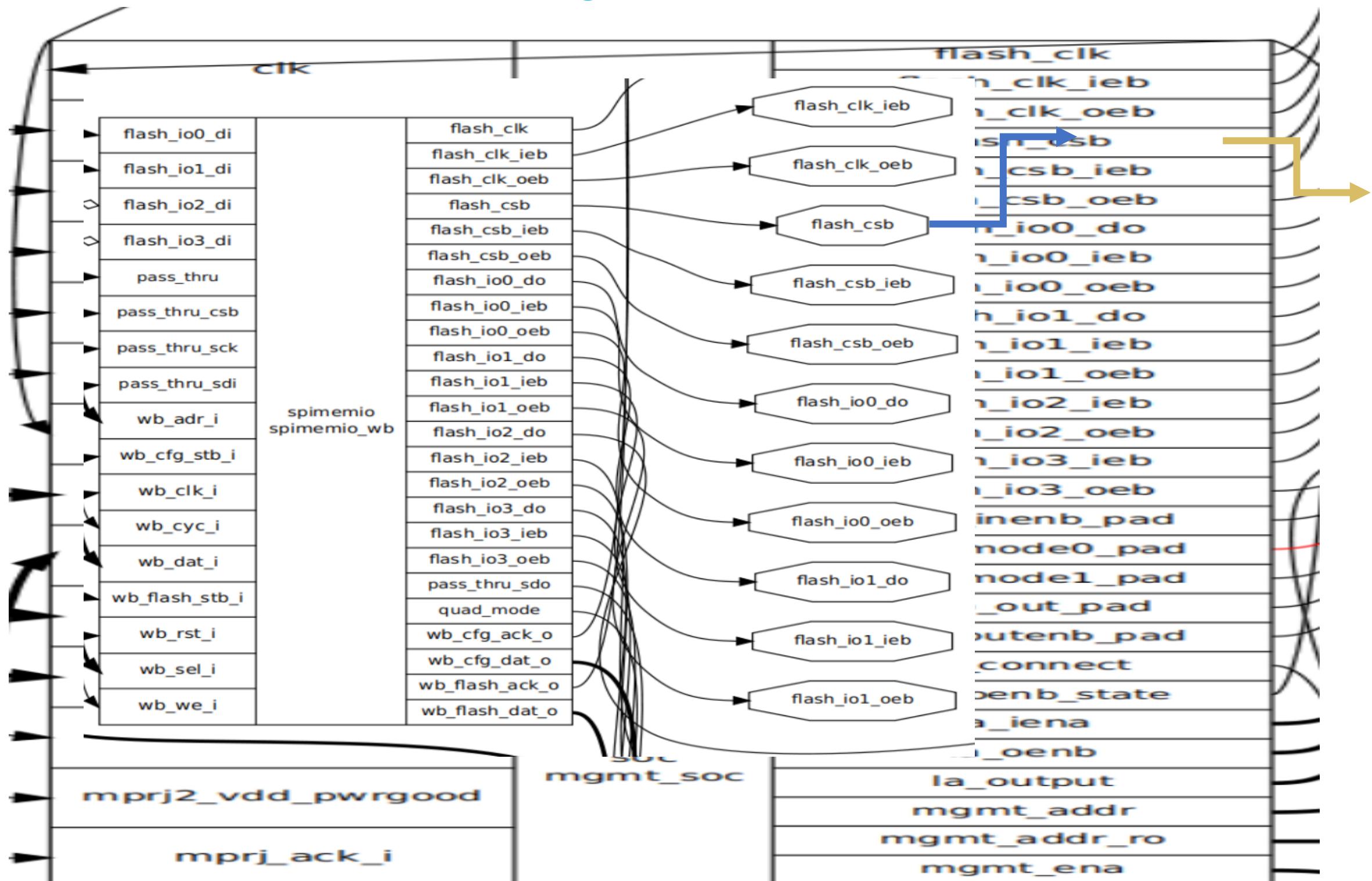
# Management SoC



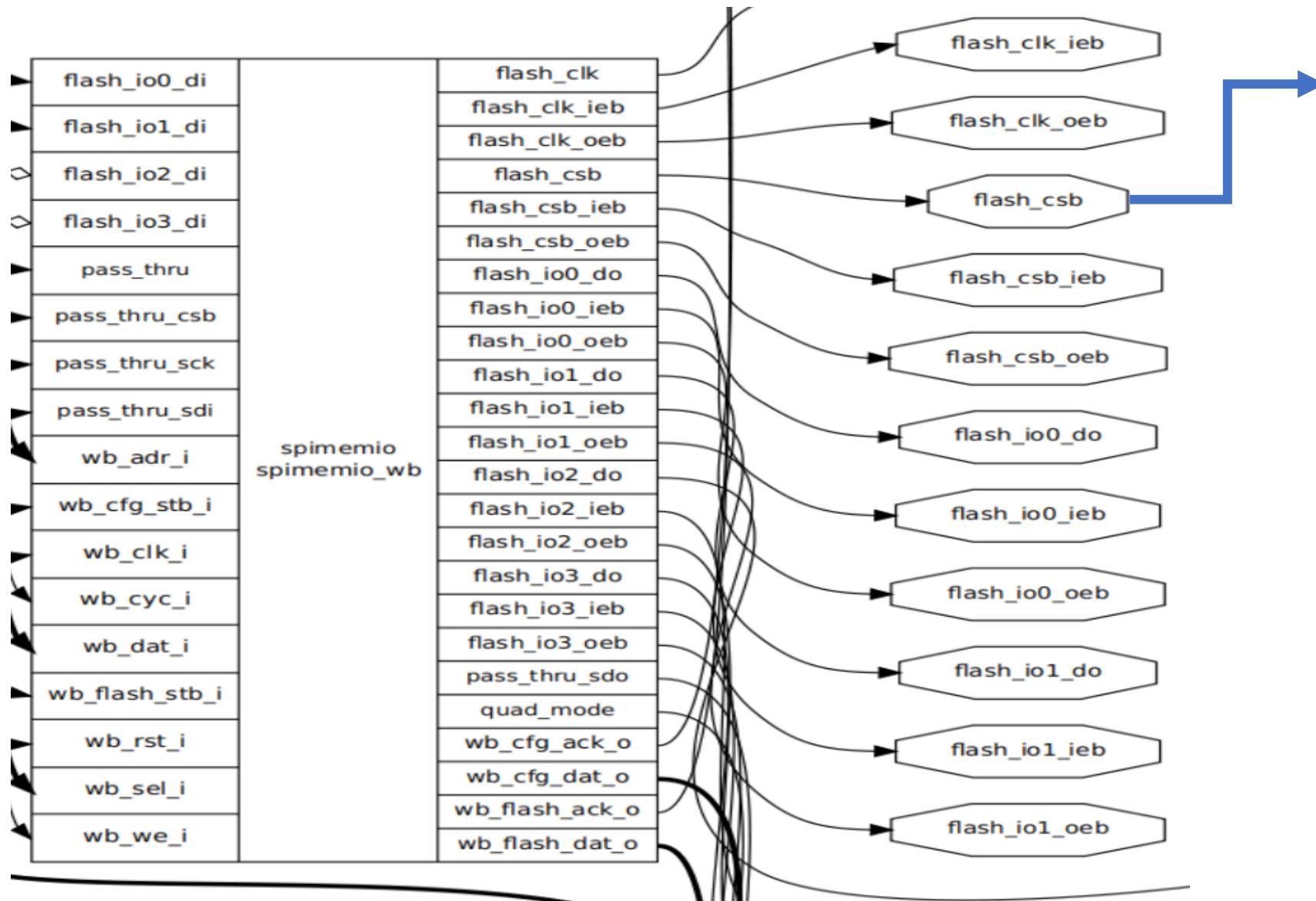
# Management SoC



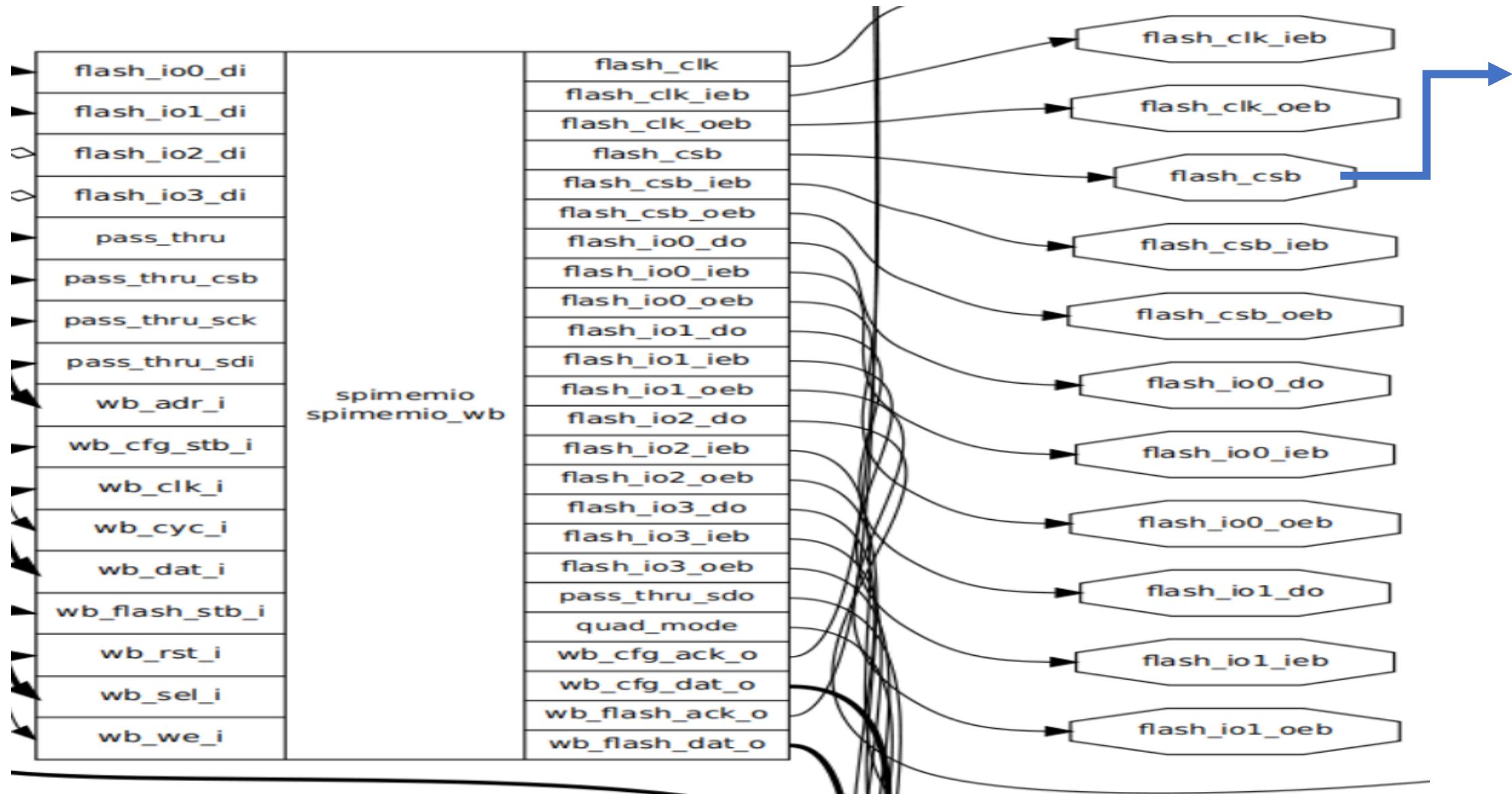
# Management SoC



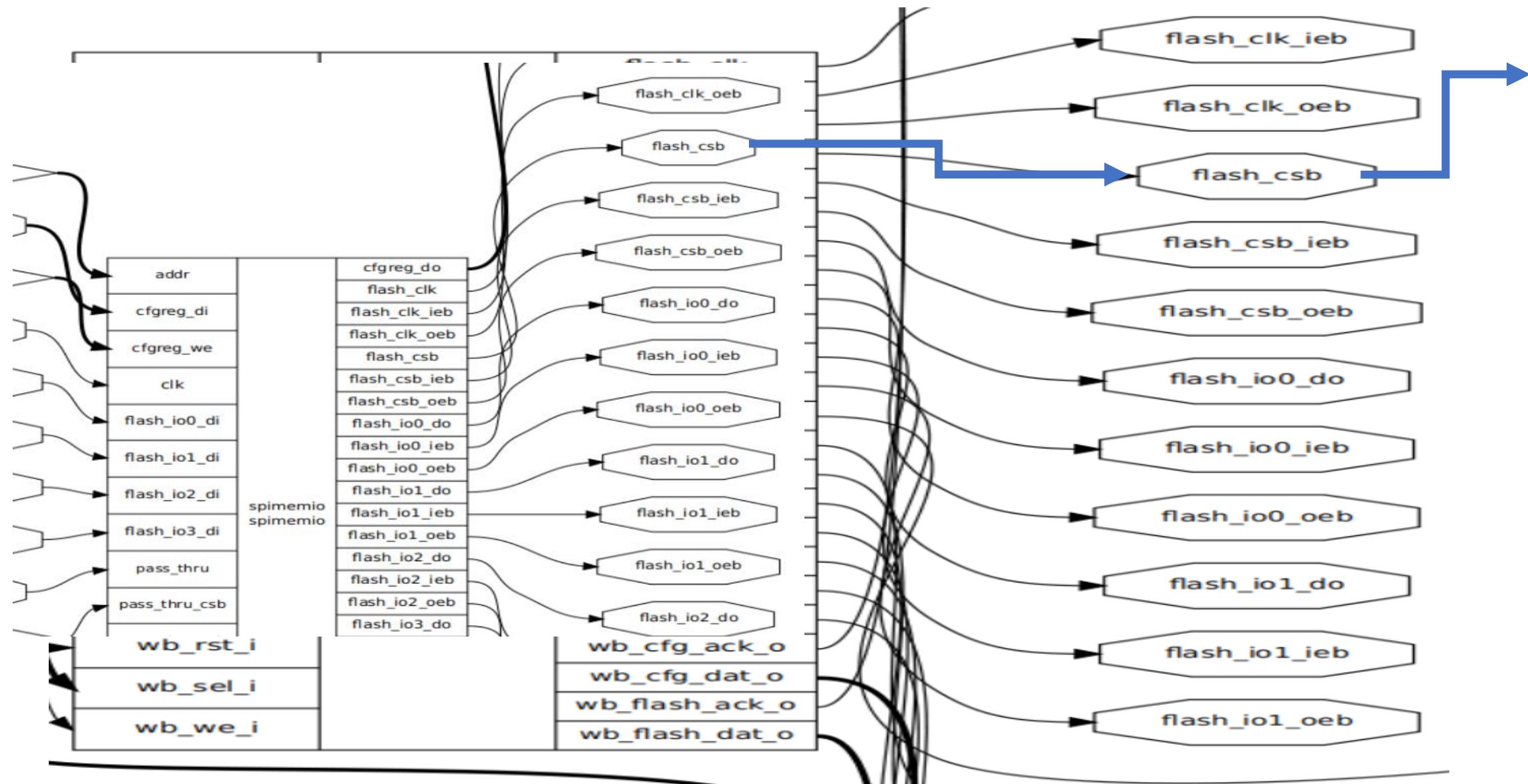
# Management SoC



# Management SoC



# Management SoC



# Management SoC

