Frequency Divider

Dantu Nandini Devi
Electronics and communication
International Institute of Information Technology Bangalore
Bangalore, India

***Abstract*—This document is a model and analysis of a Freqency Divider. This model will contain a 4 bit number lines to select by which factor does the input frequency has to be divided. It is simulated using verilog.**

***Index Terms*—Frequency Division, Clock**

I. Introduction

A frequency divider takes an input frequency and generated a output frequency depending on the division factor. One of the well-known application of frequency divider is a phase lock loop, which generates multiples of a reference frequency. The other applications include frequency synthesizers, audio equipments, radar and satellite communication, Military equipments and RF devices. It is basically used in any application where frequency matching is needed and down scaling of frequency has to performed.

$$fout = \frac{fin}{n} \tag{1}$$

Frequency dividers can be designed in 2 ways: analog and digital. Analog frequency dividers are rare and used only in very high frequency applications. One of the most important application of analog frequency divider was used in the development of televisions, the device was called injection-locked frequency divider. Digital frequency dividers are the most widely used frequency dividers. For the power of 2 integer division, a simple binary counter can be used, clocked by the input signal. In this case the LSB becomes 1/2 of the input signal, the next bit becomes 1/4 of the input signal, the third bit becomes 1/8 of the input signal and so on. Other division ratios can be obtained by adding logic gates to the chains of flipflops.

This is a Frequency Divider model which has 4 bit number line and a clock signal. It provides an output clock signal that alligns with the equation(1). The 4 bit number is taken as a input. Depending on the 4 bit number there is a algorithm running which divides the input clock signal and provides a appropriate output.

Fig. 1. Frequency Divider

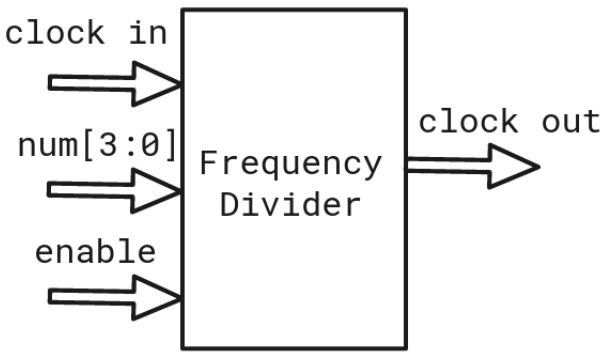

Fig. 2. Basic Block Diagram

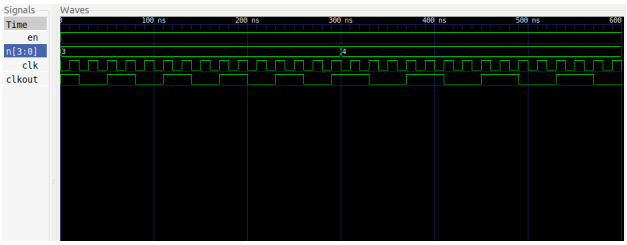

Fig. 3. Waveforms after execution of the verilog code

References

[1] http://pgandhi189.blogspot.com/2014/11/universal-frequency-dividor.html, the verilog code was taken from here.

[2] https://en.wikipedia.org/wiki/Frequency_divider, some content was taken from here..

[3] https://eng.libretexts.org/Bookshelves/Electrical_Engineering/Electronics/Microwave_and_RF_Design_IV%3A_Modules_(Steer)/06%3A_Mixer_and_Source_Modules/6.08%3A_Frequency_Divider, some content and fig.1. was taken from here..