which bus in a microprocessor system is responsible for determining whether an address is for memory or an I/O device?

A) Address Bus B) Data Bus C) Control Bus
D) System Bus E) Cache Bus

2. Which clock speed range did the 8086 microprocessor support?

A) 1 MHz to 3 MHz B) 5 MHz to 10 MHz
C) 10 MHz to 15 MHz D) 20 MHz to 25 MHz
E) 60 MHz to 66 MHz

3. What is the primary difference between the 8086 and 8088 microprocessors?

A) Clock speed B) Internal architecture
C) Address bus width D) Number of instructions
E) Data bus width

4. In IEEE 754 single precision, how many bits are allocated for the exponent?

A) 4 bits B) 7 bit C) 8 bits D) 10 bits E) 11 bits

5. What is the IEEE 754 single precision hexadecimal format representation for the number +12?

A) 0x51400000 B) 0x41400000 C) 0x4F400000
D) 0x41500000 E) 0x5F400000

6. Which unit in the 8086 architecture is responsible for handling memory addresses and instructions?

A) Execution Unit (EU) B) Stack Segment
C) Instruction Queue D) Control Unit
E) Bus Interface Unit (BIU)

7. What is the main function of the AX register in the 8086 microprocessor?

A) Base register for address calculations
B) Accumulator for arithmetic operations
C) Counter for loop operations
D) Holds data for I/O operations
E) Stores segment addresses

8. Which register points to the next instruction in a program?

A) SP (Stack Pointer) B) BP (Base Pointer)
C) IP (Instruction Pointer) D) SI (Source Index)
E) DI (Destination Index)

9. In the 8086 programming model, which register is used to store data temporarily?

A) CS (Code Segment) B) DS (Data Segment)
C) ES (Extra Segment) D) SS (Stack Segment)
E) BX (Base Register)

10. How much memory can each segment in the 8086 microprocessor access?

A) 16 KB B) 32 KB C) 64 KB D) 128 KB E) 1 MB

11. What is the purpose of the Code Segment (CS) register in the 8086?

A) Stores data values
B) Contains program instructions
C) Points to the stack area D) Stores extra data like strings
E) Holds offset addresses

12. In the 8086, what is the range of values for a logical address's offset?

A) 0x0000 to 0xFFFF B) 0x1000 to 0x2000
C) 0x2000 to 0x3000 D) 0x0000 to 0x0FFF
E) 0xF000 to 0xFFFF

13. What is the decimal equivalent of the binary number $(1101\ 1011)_2$?

A) 219 B) 175 C) 123 D) 135 E) 193

14. In the 8086 microprocessor, which flag is set if there is a carry out from the most significant bit during an addition operation?

A) Parity Flag (PF) B) Auxiliary Carry Flag (AF)
C) Sign Flag (SF) D) Carry Flag (CF)
E) Direction Flag (DF))

15. How is the physical address calculated in the 8086 microprocessor if the segment address is 3000H and the offset address is 1234H?

A) 31234H B) 41234H C) 50000H
D) 4234H E) 30000H

16. In the ... address?

A) A 16-bit address that identifies a segment block
B) A 20-bit address that is placed on the address bus to access memory
C) A 12-bit address that points to a register
D) An address used only within the stack segment
E) A 64-bit address used in the BIU

17. How do you determine the result's sign when subtracting binary numbers using two's complement?

A) By converting to hexadecimal first
B) By checking if the LSB is 0
C) By taking the one's complement
D) By adding an extra bit to the result
E) By checking if the MSB is 1

18. What is the hexadecimal representation of the binary number $(1011\ 0101\ 0110)_2$?

A) B56 B) A5F C) C7A D) D43 E) 8B2

19. If you have an internet speed of 48 Mb/s, how many Megabytes (MB) of data can be downloaded per second?

A) 2 MB B) 3 MB C) 4 MB D) 6 MB E) 8 MB

20. Which unit is used to represent 64 bits in binary terminology?

A) Byte B) Word C) Double-word
D) Quad-word E) Mega-word

21. What is the two's complement of the binary number $(1010)_2$?

A) 0101 B) 1010 C) 0110
D) 1101 E) 1110

22. Which format stores numbers with the least significant byte in the lowest-numbered memory location?

A) Big Endian B) Double-precision
C) Floating-point D) ASCII
E) Little Endian

A) 4000H to 4FFFH D) 0000H to FFFFH
C) 40000H to 4FFFFH
E) 1000H to 1FFFH

24. In ASCII encoding, how many bits are used t represent each character?

A) 5 bits B) 6 bits C) 7 bits D) 8 bits E) 10 bits

25. What is the primary function of the 8284A chip in relation to the 8086/8088 microprocessor?

A) Data storage
B) Memory management
C) Data transmission
D) Clock generation and synchronization
E) Cache control

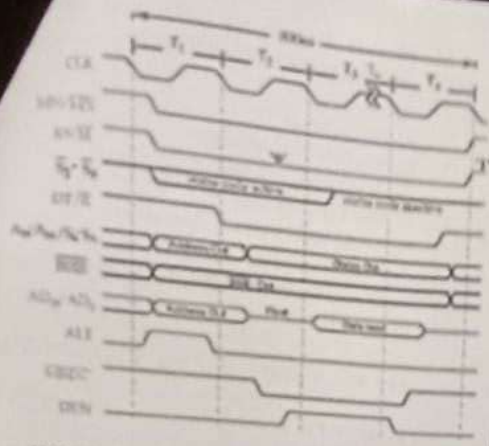
26. In the 8284A clock section, what frequency does a 15 MHz crystal generate as the primary clock signal for the 8086?

A) 5 MHz B) 10 MHz C) 15 MHz
D) 20 MHz E) 2.5 MHz

27. What is the function of the ALE (Address Latch Enable) pin in the 8086 minimum mode?

A) It enables data transfer from memory
B) It resets the
C) It signals the end of a read cycle
D) It controls the clock signal
E) processor it latches the address onto the address bus

28. In which option is the description of the Timing diagram given in the figure given correctly?



A) Minimum mode IO read timing diagram
B) Minimum mode IO write timing diagram
C) Maximum mode memory read timing diagram
D) Minimum mode memory read timing diagram
E) Maximum mode memory write timing diagram

29. **What is the purpose of memory banking in the 8086 microprocessor?**

A) To enable the use of cache memory
B) To allow access to both 8-bit and 16-bit data
C) To manage I/O devices
D) To increase clock speed
E) To enhance interrupt handling

30. **In maximum mode, what is the purpose of the bus grant (BG) signal?**

A) It grants the CPU exclusive control over the bus
B) It resets the CPU
C) It enables external memory access
D) It activates the interrupt system
E) It releases the bus to the DMA controller

31. **What signal in the 8086 maximum mode is used by the CPU to indicate that it is ready to release control of the bus?**

A) $\overline{LOCK}$ B) HOLD C) $\overline{RQ/GT}$ D) INTA E) READY

32. **Which signal in 8086 maximum mode indicates that the CPU is involved in a read-modify-write operation and should not be interrupted?**

A) INTA B) LOCK C) HLDA D) RQ/GT E) READY

33. **What is the role of the 8288 Bus Controller in 8086 maximum mode?**

A) To maage clock signals for the CPU
B) To generate data for the address bus
C) To handle memory addressing directly
D) To process status signals and control communication
E) To manage internal CPU registers

34. **What is the main purpose of an interrupt in a microprocessor system?**

A) To increase processing speed
B) To alert the CPU of a task needing immediate attention
C) To control memory access
D) To manage data transfer rates
E) To synchronize clock signals

35. **What is the role of the 8259 Programmable Interrupt Controller in the 8086 system?**

A) To decode the interrupt vector
B) To synchronize clock signals
C) To handle data transfers
D) To store register values during an interrupt
E) To manage and prioritize multiple interrupt requests

36. **Which interrupt in the 8086 is typically used for handling major system faults such as power failures?**

A) INTR B) INT 21H C) INT 3 D) IRQE) NMI

37. **What is the first action taken by the 8086 during a real-time mode interrupt?**

A) Loads the interrupt vector into the instruction pointer (IP)
B) Clears the interrupt flag (IF)
C) Pushes the flag register onto the stack
D) Increments the program counter
E) Saves register values into battery-backed memory

38. **What does the interrupt vector table provide for each interrupt?**

A) The priority level of the interrupt
B) The type of device that triggered the interrupt
C) The starting address for the interrupt service routine
D) The exact time of interrupt occurrence
E) The status of the processor

39. Which type of memory is volatile and loses its data when the computer is turned off?

A) ROM B) Cache Memory C) RAM
D) Flash Memory E) Hard Disk

40. What was the maximum memory addressable by the Intel 8086 microprocessor?

A) 640 KB B) 4 KB C) 16 MB D) 1 MB E) 64 MB

41. Which of the following was a key feature of the 8086 microprocessor that improved instruction processing efficiency?

A) Dual-core processing
B) Pipelining
C) Built-in graphics processing
D) Hyper-threading
E) Virtualization

42. What was the width of the address bus in the Intel 8086 microprocessor?

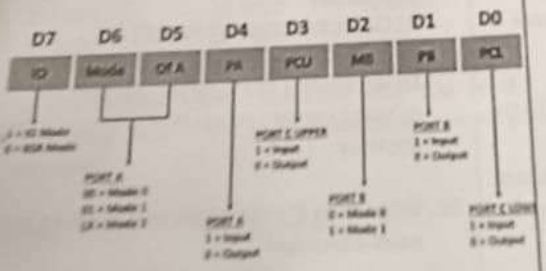
A) 8-bit B) 16-bit C) 20-bit D) 32-bit E) 24-bit

43. What is the main purpose of the 8255 Programmable Peripheral Interface (PPI)?

A) To control memory operations
B) To decode addresses
C) To generate clock signals
D) To manage interrupts
E) To interface I/O devices with the microprocessor

44. In the 8255, which mode allows for the setting or resetting of individual bits on Port C?

A) Mode 0 B) Mode 1 C) Mode 2
D) BSR mode E) Control mode



45. Identify the Mode 0 control Word to configure port A & upper port C as output port and port B & lower port C as input port?

A) 83H B) A3H C) 8FH D) 82H E) 93H

46. What is the primary function of the 8253/8254 programmable interval timer?

A) Data storage
B) Interrupt management
C) Clock signal generation
D) Address decoding
E) Timing and counting operations

47. Each counter in the 8253/8254 timer is how many bits wide?

A) 4 bits B) 8 bits C) 12 bits D) 16 bits E) 32 bits

48. What is the primary function of the 8257 DMA controller?

A) To generate clock signals
B) To facilitate data transfer between peripherals and memory
C) To manage interrupts
D) To control I/O operations
E) To decode addresses

49. Which signal input is used to control the count in each counter of the 8253/8254?

A) Clock signal B) Load signal C) Enable signal
D) Reset signal E) Start signal

50. Which signal in the 8257 indicates that the DMA controller is requesting control of the system bus?

A) LOCK B) HOLD C) HLDA
D) READY E) MEMR