Microprocessors

The clock generator (8284A) for 8086

The 8284A provides the following basic functions or signals:

- Clock generation,
- RESET synchronization,
- READY synchronization,
- TTL-level peripheral clock signal.

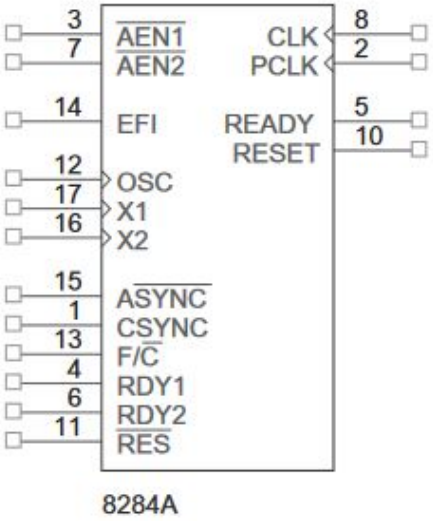
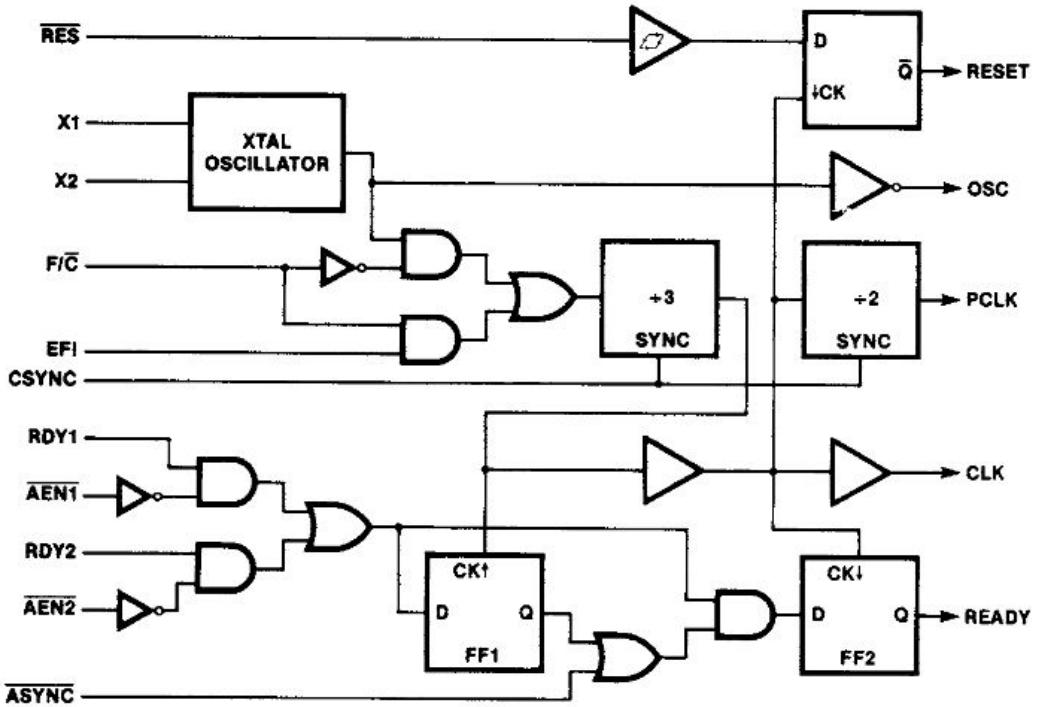


FIGURE 9–2 The pin-out of the 8284A clock generator.

The clock generator (8284A) for 8086

FIGURE 9–3 The internal block diagram of the 8284A clock generator.



Operation of the Clock Section

X1 - X2: If a crystal is attached to X1 and X2, the oscillator generates a square-wave signal.

EFI (External Frequency Input): An external clock signal can be applied directly to this pin (e.g., TTL clock).

F/C (Frequency/Crystal Select): This pin determines whether a crystal or external clock is used.

F/C' = 1: Crystal oscillator is used.

F/C' = 0: External clock signal (EFI) is used.

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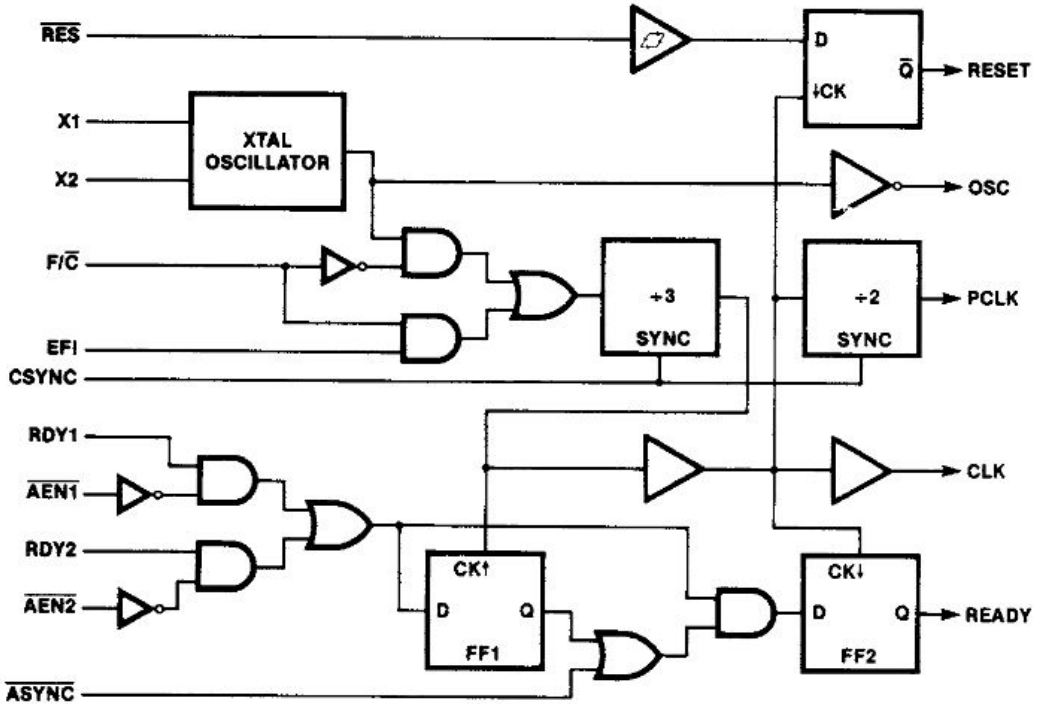
CLK and PCLK Outputs:

CLK (Clock): This is the main clock signal going to the 8086/8088 processor. This signal is 1/3 of the crystal frequency.

For example: 15 MHz crystal → CLK = 5 MHz

PCLK (Peripheral Clock): The clock signal provided for peripheral devices. It is half the frequency of CLK.



The clock generator (8284A) for 8086

Reset (RST) Signal Generation

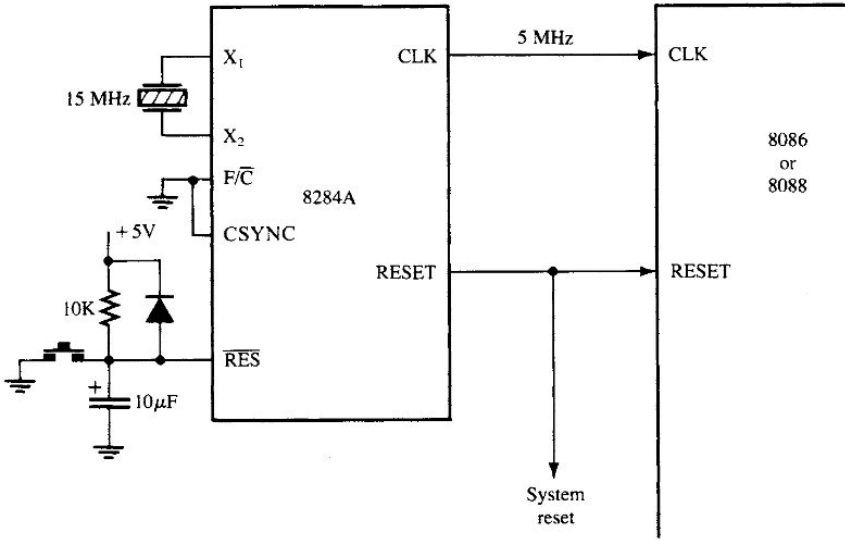
The 8284A generates a RESET signal when the system is powered up or manually triggered. This signal returns the 8086/8088 processor to its initial state.

Reset Generation Process:

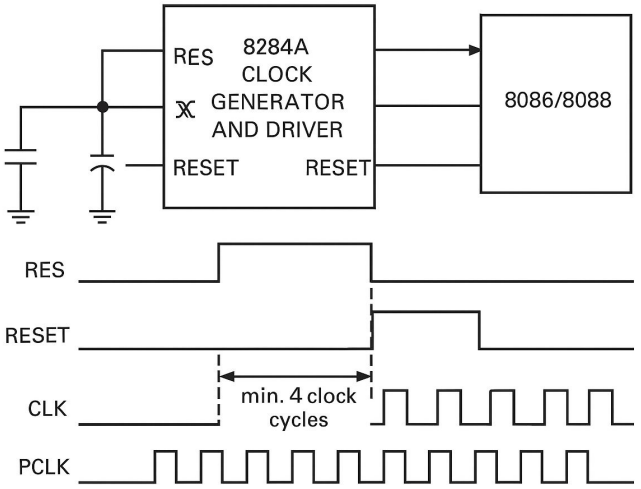
RES (Reset Input): Can be triggered by an external button or circuit.

RC circuit: When power is applied, the RESET signal is held active for a period of time by an RC time constant.

RESET output: This is the reset signal sent to the 8086/8088 processor. This signal causes the processor to reset.



The clock generator (8284A) for 8086



828A Clock Generator and Driver

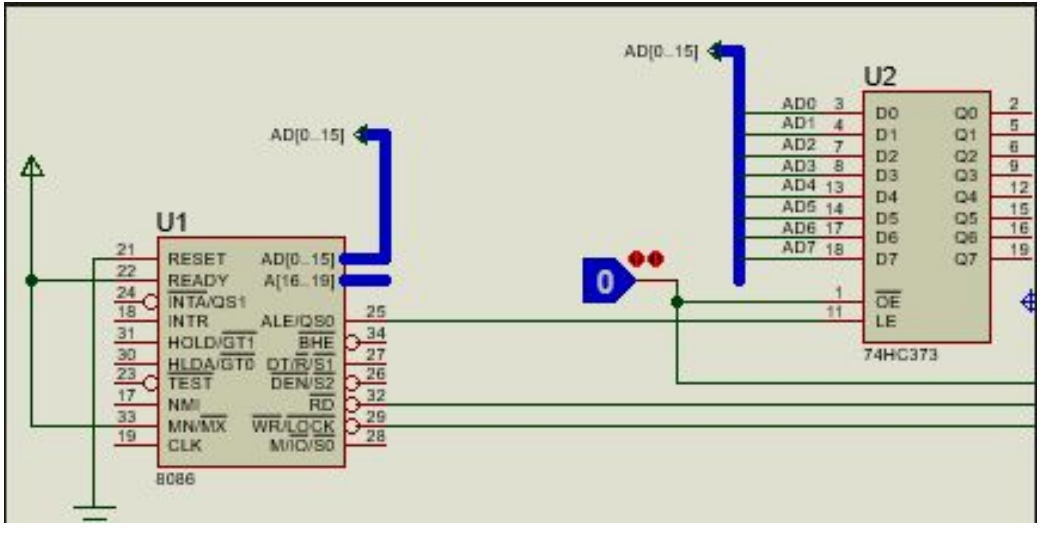
Function	Pins	Description
Clock Generation	X1, X2, EFI, F/C, CLK, PCLK	Generates the system clock using either a crystal oscillator or external clock input. CLK is the main clock output for the CPU; PCLK is for peripherals.
Reset Generation	RES, RESET	Produces a reset signal for the CPU during power-up or manual reset. Ensures proper initialization of the processor.

8282 8-bit latch (or 74HC373)

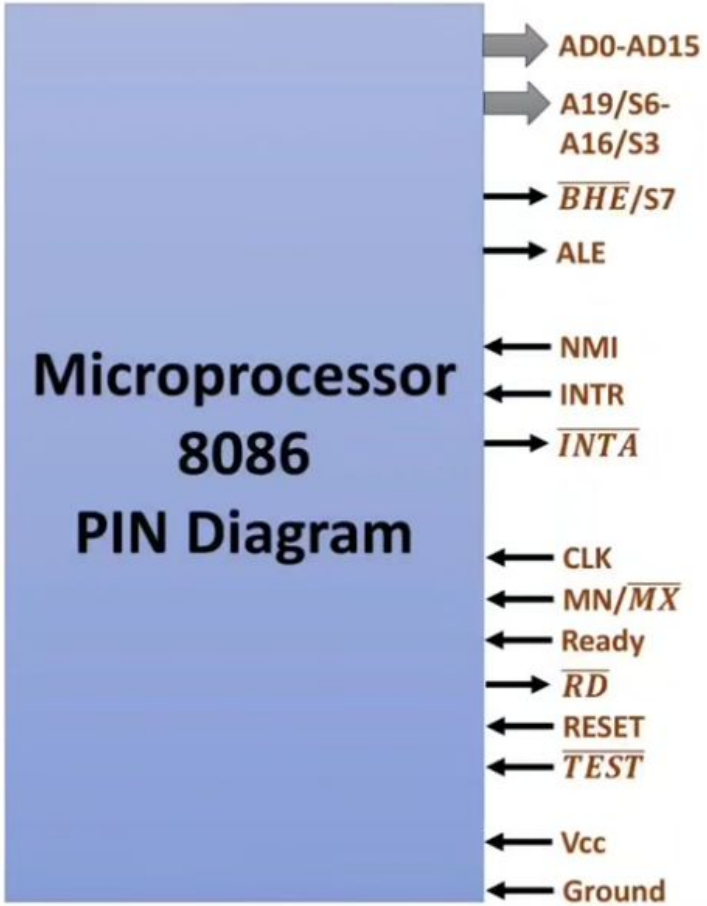
The 8086 uses a **multiplexed address/data bus (AD0–AD15)**, meaning the same lines carry **address** during the first part of the bus cycle and **data** during the second part.

1. **During T1 state of the bus cycle**, the 8086 places the **address** on AD0–AD15.
2. The **ALE (Address Latch Enable)** signal from 8086 goes high, indicating that the address is valid.
3. The **STB̄** pin of 8282 (**LE** pin 74HC373) is triggered by ALE (usually connected directly).
4. The 8282 **latches the lower byte of the address** (AD0–AD7) and holds it on its outputs (Q0–Q7).
5. The **OĒ** pin enables the outputs to be used as part of the full address bus.

Note: For AD8–AD15, a second latch (like another 8282 or 74HC373) is used to hold the upper byte of the address.



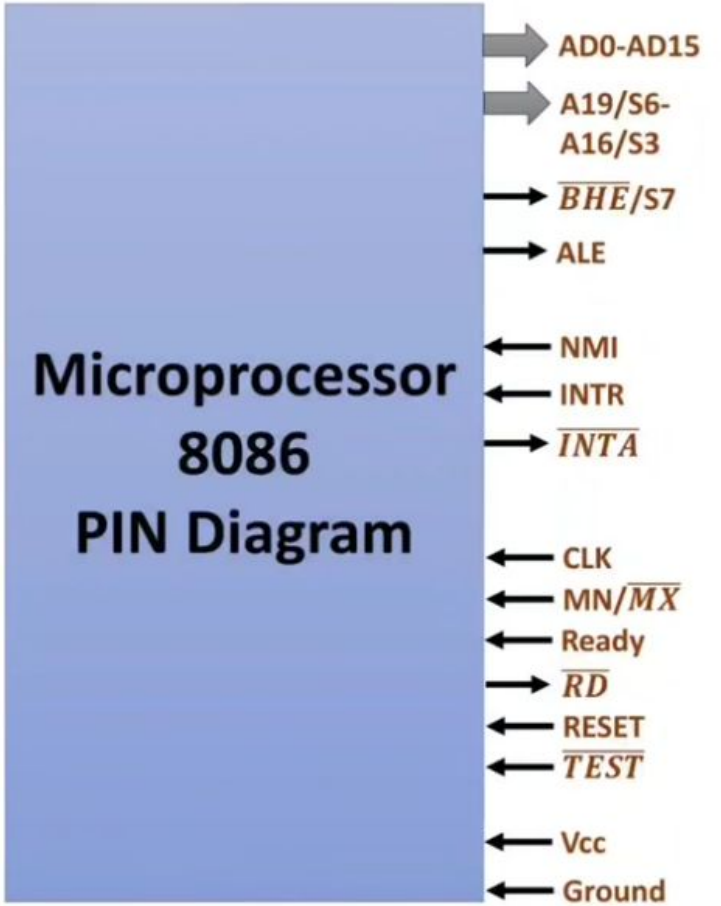
Control Signals in the 8086 Microprocessor



Control signals are essential for managing internal operations and communication with external devices.

These signals determine when data is read, written, and which operations are performed.

Control Signals in the 8086 Microprocessor



Operating Modes

The 8086 can operate in two modes:

- **Minimum Mode**: Used in single-processor systems.
- **Maximum Mode**: Used in multiprocessor systems.

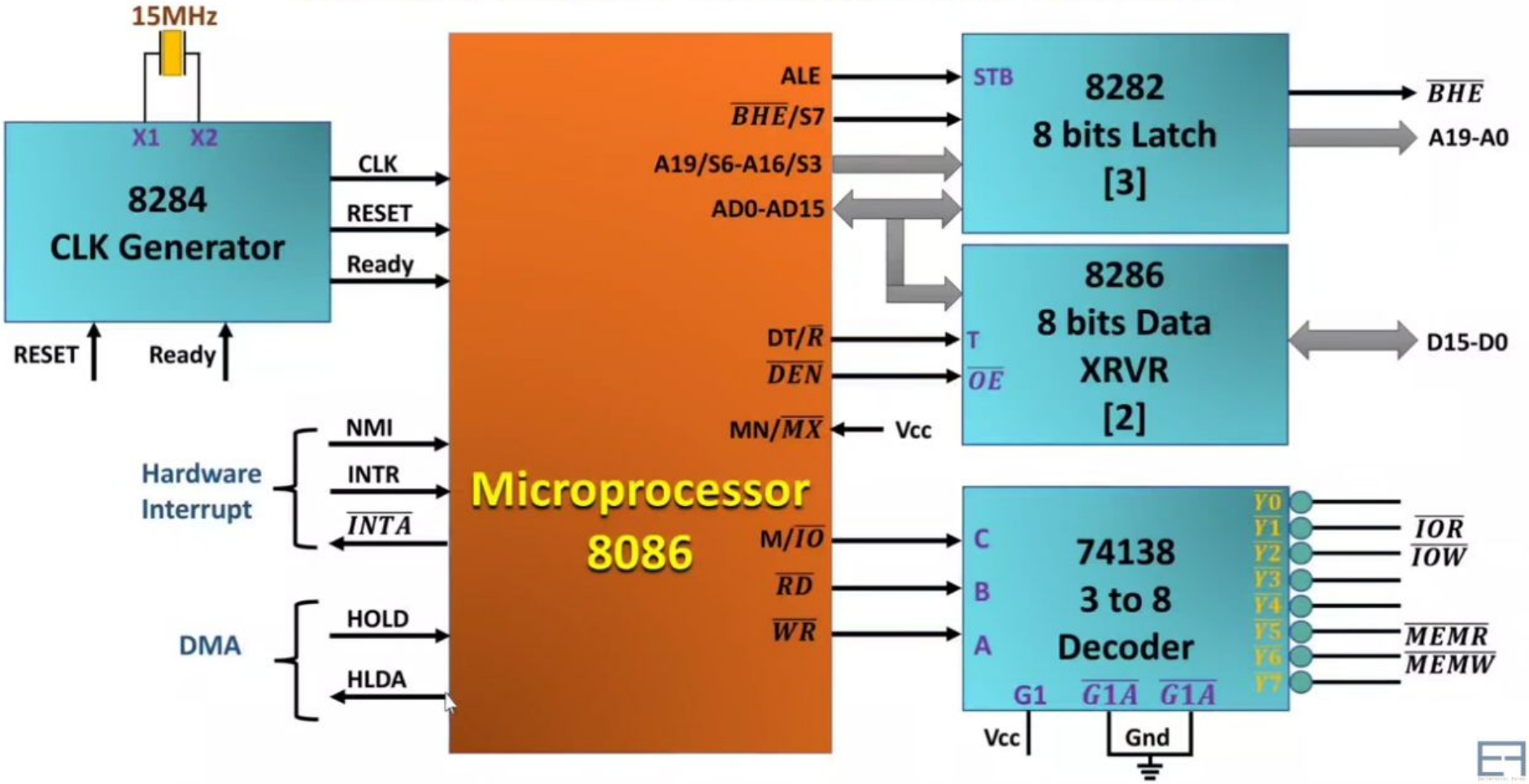
Control signals vary depending on the selected mode.

Control Signals in the 8086 Microprocessor

Minimum Mode Control Signals

Signal	Description
$\overline{RD}$ (Read)	Indicates a read operation from memory or I/O. Active low.
$\overline{WR}$ (Write)	Indicates a write operation to memory or I/O. Active low.
ALE (Address Latch Enable)	Used to latch the address from the multiplexed address/data bus.
DT/$\overline{R}$ (Data Transmit/Receive)	Determines the direction of data flow. High = transmit, Low = receive.
DEN (Data Enable)	Enables the data bus transceivers.
$\overline{INTA}$ (Interrupt Acknowledge)	Indicates that the processor is acknowledging an interrupt request.
HOLD / HLDA	Used for Direct Memory Access (DMA). HOLD requests control of the bus, HLDA acknowledges it.

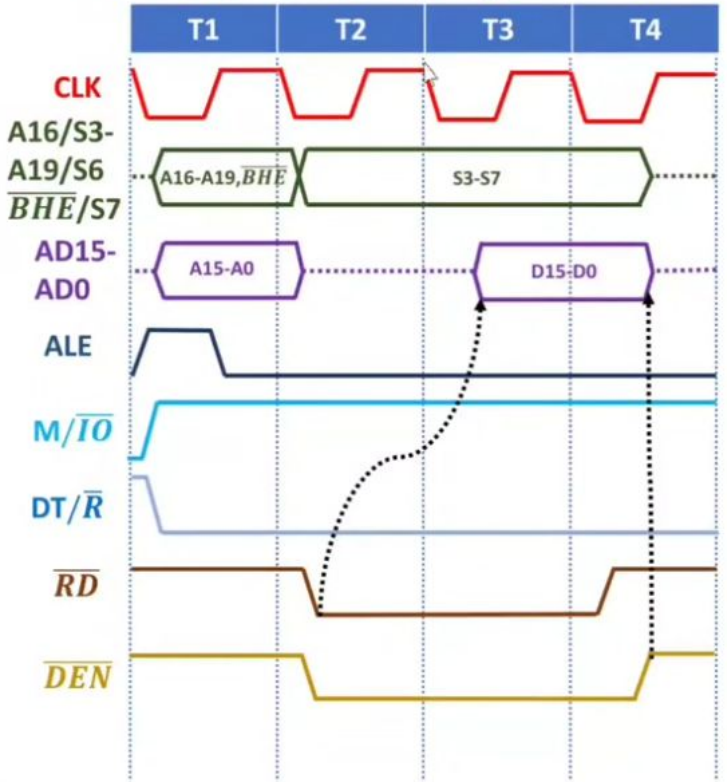
Minimum Mode of 8086



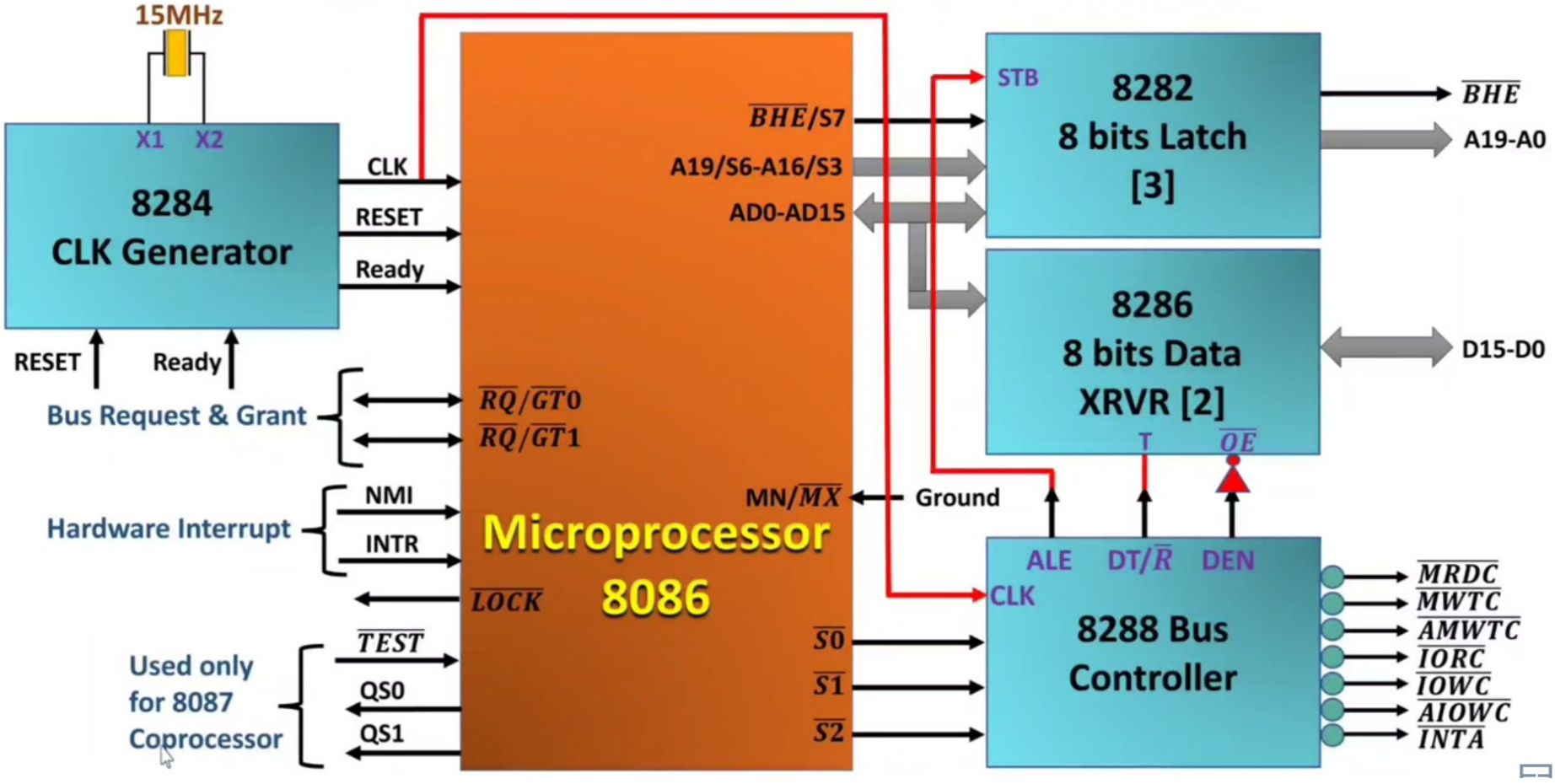
Timing Diagram (Minimum Mode - Memory Read)

- By using three terminals [$\overline{RD}$, $\overline{WR}$ & M/$\overline{IO}$], we can execute four Machine Cycles.
  - Memory Read [$\overline{RD} = 0, \overline{WR} = 1$ & M/$\overline{IO} = 1$]
  - Memory Write [$\overline{RD} = 1, \overline{WR} = 0$ & M/$\overline{IO} = 1$]
  - IO Read [$\overline{RD} = 0, \overline{WR} = 1$ & M/$\overline{IO} = 0$]
  - IO Write [$\overline{RD} = 1, \overline{WR} = 0$ & M/$\overline{IO} = 0$]

❖ Memory Read Timing Diagram



Maximum mode in 8086

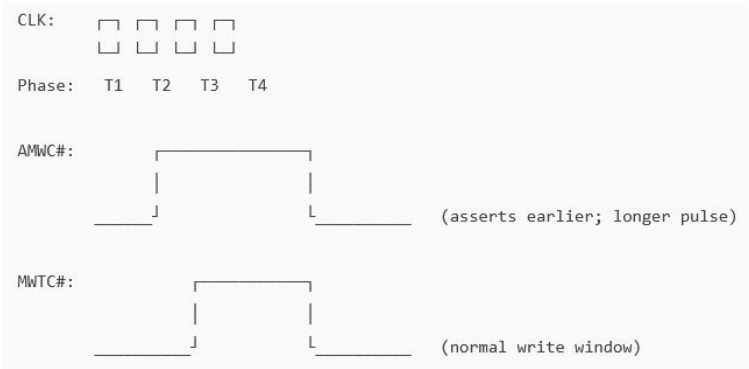


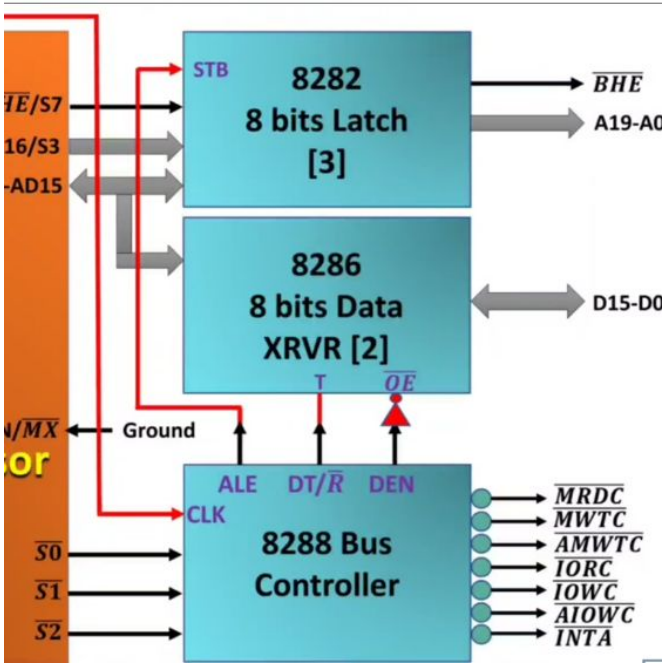
Maximum mode in 8086 - Status signals with 8288 Bus Controller

- In **Minimum Mode**, the 8086 processor handles all necessary control signals directly and does not require an additional bus controller.
- In **Maximum Mode**, the 8086 processor generates various **status signals** and these signals are received and processed by a bus controller such as the 8288.

The **8288 Bus Controller** receives these status signals and is used to control communication between the processor and other system components. This is especially important in systems with multiple processors or I/O devices.

Note:
MWTC (Memory Write Command): the *normal* active-low write command asserted during a write bus cycle to tell memory to store the data on the data bus.
AMWC (AMWTC - Advanced Memory Write Command): an *early* (advanced) active-low write command that goes active **one clock earlier** (timing aligned like a read command) to provide a **wider write pulse** for slower memory devices.





Maximum mode in 8086

- Bus timing diagram

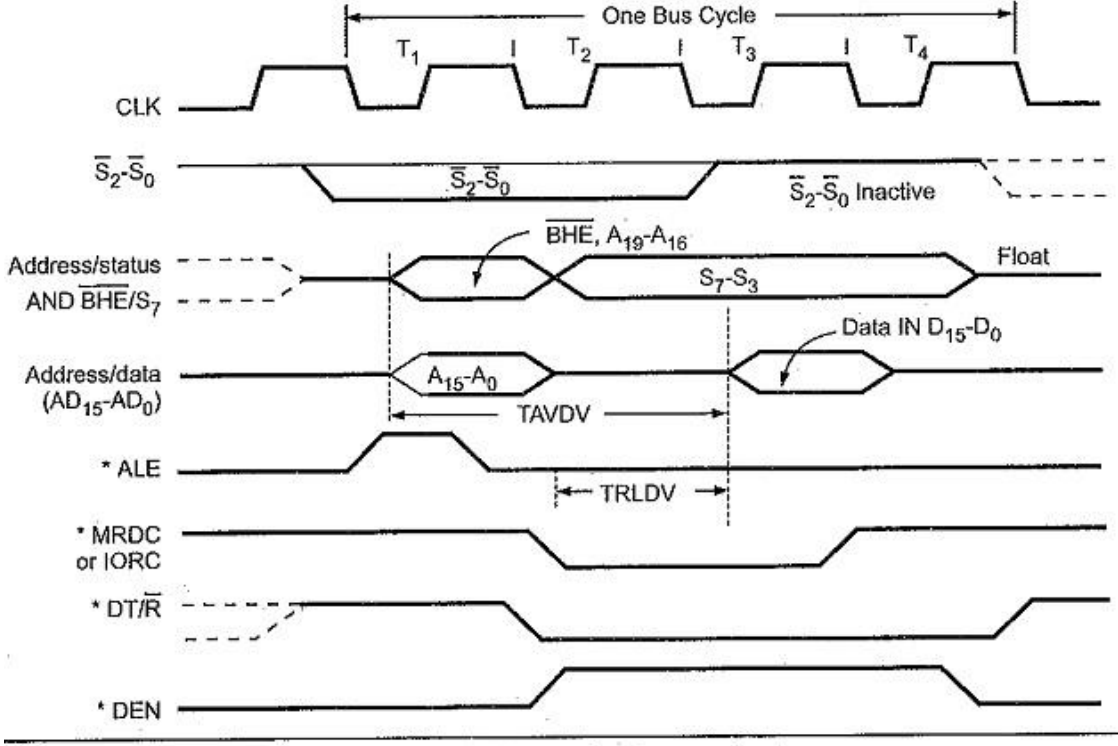


Fig. 10.10 (a) Input (read operation)

1. S_0,S_1,S_2 are set at the beginning of bus cycle. On detecting the change on passive state $S_0 = S_1 = S_2 = 1$, the 8288 bus controller will output a pulse on its ALE and apply a required signal to its DT/R pin during T_1.
2. In T_2, 8288 will set DEN = 1 thus enabling transceiver. For an input, 8288 it will activates MRDC or IORC. These signals are activated until T_4. For an output, the AMWC or AIOWC is activated from T_2 to T_4 and MWTC or IOWC is activated from T_3 to T_4.
3. The status bits S_0 to S_2 remain active until T_3, and become passive during T_3 and T_4.
4. If ready input is not activated before T3, wait state will be inserted between T_3 and T_4.

Maximum mode in 8086

- Bus timing diagram

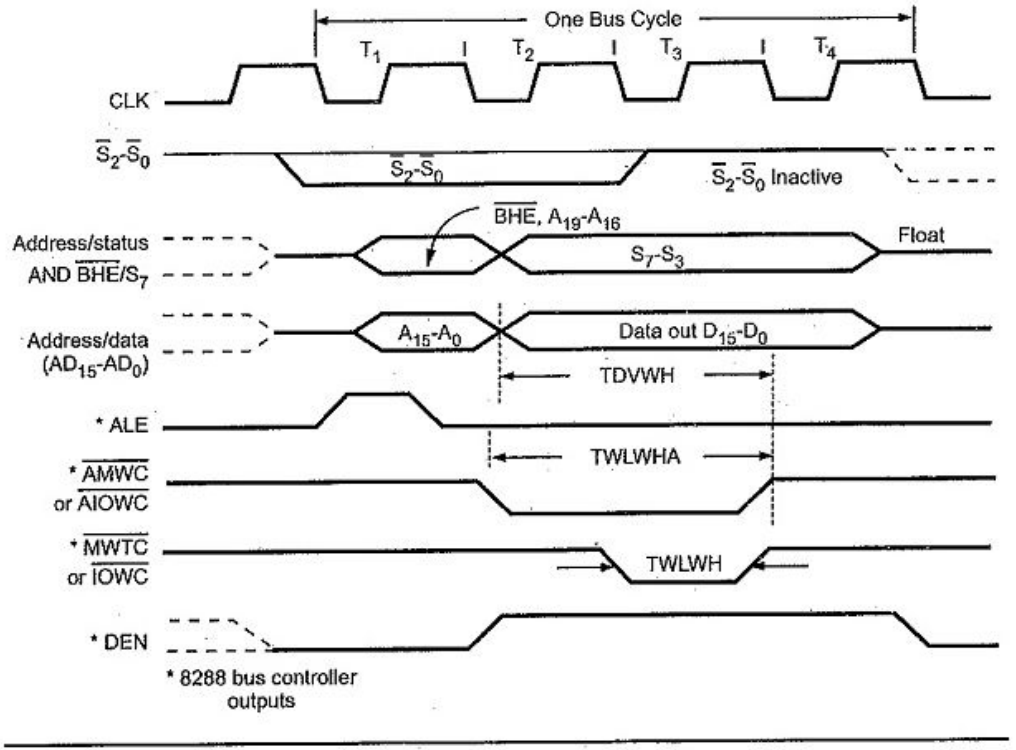
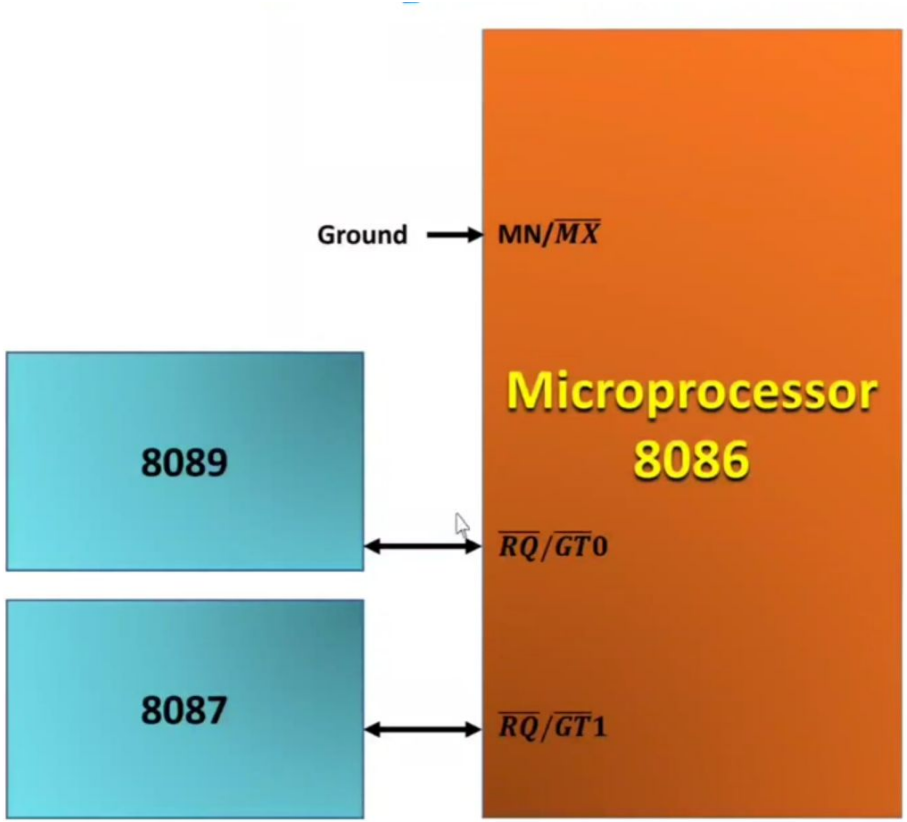


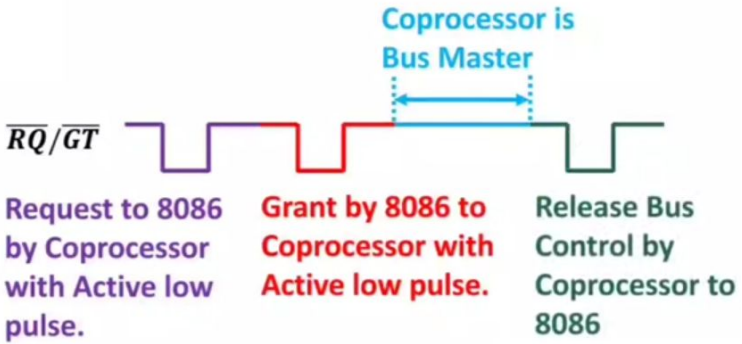
Fig. 10.10 (b) Output (write operation)

1. S_0,S_1,S_2 are set at the beginning of bus cycle. On detecting the change on passive state $S_0 = S_1 = S_2 = 1$, the 8288 bus controller will output a pulse on its ALE and apply a required signal to its DT/R pin during T_1.
2. In T_2, 8288 will set DEN = 1 thus enabling transceiver. For an input, 8288 it will activates MRDC or IORC. These signals are activated until T_4. For an output, the AMWC or AIOWC is activated from T_2 to T_4 and MWTC or IOWC is activated from T_3 to T_4.
3. The status bits S_0 to S_2 remain active until T_3, and become passive during T_3 and T_4.
4. If ready input is not activated before T3, wait state will be inserted between T_3 and T_4.

Maximum mode in 8086 - Bus request and bus grant



- Request/Grant $\overline{RQ}/\overline{GT}$ is used in Maximum mode for coprocessor taking control of system Bus.
- For Maximum mode, MN/$\overline{MX}$ should be connected to ground [logic 0].
- In Maximum Mode, $\overline{RQ}/\overline{GT}0$ and $\overline{RQ}/\overline{GT}1$ two lines are there for coprocessor operation.
- $\overline{RQ}/\overline{GT}0$ is having higher priority then $\overline{RQ}/\overline{GT}1$.
- By default, $\overline{RQ}/\overline{GT}$ lines are there at logic 1.



Maximum mode in 8086 - Lock signal in 8086