ES203 Digital Systems
LAB Assignment - 4

Indian Institute of Technology, Gandhinagar
Time & Venue: Friday 2-5 pm [ONLINE]
Submission deadline: 14th Oct, 2021

For each of the questions, write a Verilog code. You also need to create a testbench and show the simulation results.

Please refer to Lecture-18 Video for more details on this lab.

1. **[15 Marks]** Read how LFSR (linear feedback shift registers) are designed and implement at 4-bit LFSR in Verilog.

2. **[15 Marks]** Design a 5-bit up/down counter with signals (a) clear, (b) enable and (c) Mode, and in the same priority sequence (clear -> enable -> Mode). Clear and Enable are asynchronous signals, and Mode can be taken as asynchronous or synchronous signal. The counter has i*nit_count* that can be asynchronously set. The counter can be cleared to all zero at any time, and if the counter is disabled after that (or not enabled), the output is 0.

   Once the counter is enabled, it will count up or down based on the Mode input. If init_count = 00111 and mode is set to "up," the counter will count 7, 8, 9,...31,7,8,9…If it is disabled, then the output will be the last count. For example, if the counter is disabled when the count output is 9, the output will remain 9. If the mode changes asynchronously, then the count will begin from init_count. For example, if the mode changes at 9 when the counter was counting up, then the new sequence will be: 9, 7, 6, 5, ….0, 7, 6,5,..

   Use behavioral coding.

[Please note that if you still have questions about the lab, you can ask your TA, or me during tutorial sessions. Please join 5 mins before the tutorial session begins.]