ES203 Digital Systems
LAB Assignment - 1

Indian Institute of Technology, Gandhinagar
August 17, 2021
Time & Venue: Friday 2-5 pm [ONLINE]

Submission deadline: Aug 20, 2021 1 pm

For each of the questions, write a Verilog code. You also need to create a testbench and show the simulation results. You can use Xilinx Vivado or EDA playground for this assignment.

1. **[10 Marks**] Implement the following function using logic gates (structural code) and continuous assignment.

$$\boldsymbol{f}\ (\boldsymbol{a}, \boldsymbol{b}, \boldsymbol{c}, \boldsymbol{d}) = \sum \boldsymbol{m}(\mathbf{0}, \mathbf{3}, \mathbf{6}, \mathbf{9}, \mathbf{11}, \mathbf{13}, \mathbf{15})$$

2. **[10 Marks]** Implement a full adder and test it.