ES203 Digital Systems
LAB Assignment - 8

Indian Institute of Technology, Gandhinagar
Time & Venue: Friday 2-5 pm [ONLINE]
Submission deadline: 15th Nov, 2021

For each of the questions, write a Verilog code. You also need to create a testbench and show the simulation results.

1. **[30 marks]** Write a **structural code** for implementing Moore FSM for the following: If the input (overlapping) sequence is 00100 then output a=1, if the input (overlapping) sequence is 10100 then b=1, else both are 0.
   For this question, you need to show the state assignment table and hardware circuits separately. You need to use JK flip-flop for implementing the FSM. You may write a behavioral code for JK FF.

   Submission guideline: You have to submit the scanned image of state table, state assignment table, state excitation table and hardware implementation. Along with this, you will submit the Verilog code, test bench and simulation waveforms.