ES203 Digital Systems
LAB Assignment - 6

Indian Institute of Technology, Gandhinagar
Time & Venue: Friday 2-5 pm [ONLINE]
Submission deadline: 28th Oct, 2021

For each of the questions, write a Verilog code. You also need to create a testbench and show the simulation results.

1. Write a Moore and Mealy implementation for detecting the following sequences:

   (a) **[10 marks]** Overlapping 1011 sequence
   (b) **[20 marks]** Overlapping 1001 **OR** 1101 sequences.

   Draw the state diagrams as well.