ES203 Digital Systems
LAB Assignment - 7

Indian Institute of Technology, Gandhinagar
Time & Venue: Friday 2-5 pm [ONLINE]
Submission deadline: 6th Nov, 2021

For each of the questions, write a Verilog code. You also need to create a testbench and show the simulation results.

1. **[20 marks]** Write a **structural code** for implementing Moore and Mealy FSM for detecting the following overlapping sequence: 10010
   For this question, you need to show the state assignment table and hardware circuits separately. You may write the DFF code using behavioral coding.
   Submission guideline: You have to submit the scanned image of state table, state assignment table, hardware implementation. Along with this, you will submit the Verilog code, test bench and simulation waveforms.

2. **[20 marks]** Consider an FSM with 2 inputs and one output. Write a Verilog code to implement the Mealy FSM implementation for detecting the following overlapping sequence [11,00,11]. Write a **behavioral code** for the same. Show the Mealy FSM state diagram also.
   Submission guideline: You have to submit the scanned image of state diagram. Along with this, you will submit the Verilog code, test bench and simulation waveforms.