ES203 Digital Systems
LAB Assignment - 2

Indian Institute of Technology, Gandhinagar

Time & Venue: Friday 2-5 pm [ONLINE]

For each of the questions, write a Verilog code. You also need to create a testbench and show the simulation results.

1. **[10 Marks]** Implement a 3x8 decoder and use it to implement the function
$$\boldsymbol{f}\ (\boldsymbol{a}, \boldsymbol{b}, \boldsymbol{c}, \boldsymbol{d}) = \sum \boldsymbol{m}(\mathbf{0}, \mathbf{3}, \mathbf{6}, \mathbf{9}, \mathbf{11}, \mathbf{13}, \mathbf{15})$$

2. **[10 Marks**] Implement a 8-bit shift register using D-flip-flops.

3. **[10 Marks]** Implement 4-bit synchronous and asynchronous UP counters using (a) JK flip-flops (b) Using behavioral code. Use active low enable.

4. **[10 Marks]** Design a BCD/Binary up/down counter that can count the following sequences: 0…15, 15…0, 0…9, 9…0. Implement the code in such a way that lock-out states are handled appropriately. Also, provide an active low *reset*.