ES203 Digital Systems
LAB Assignment - 3

Indian Institute of Technology, Gandhinagar

Time & Venue: Friday 2-5 pm [ONLINE LAB]
Dt 7.9.2021

This lab has to be implemented using Vivado. For testing your code, you can use EDAboard, but the final codes need to be on Vivado.

1. Implement the following three Parallel adders and compare them in terms of LUTs utilization and critical path delay (i.e. worst case delay).

    a. **[10 marks] Ripple carry adder (Sect 3.2.2) -- parameterized code for n-bits using generate**
    b. **[15 marks] Carry- Lookahead adder (Sect 3.4.1) – 4-bit implementation**
    c. [15 marks] Carry-select adder is one other type of adder – 4 bit implementation.