ES203 Digital Systems
LAB Assignment - 5

Indian Institute of Technology, Gandhinagar
Time & Venue: Friday 2-5 pm [ONLINE]
Submission deadline: 21st Oct, 2021

For each of the questions, write a Verilog code. You also need to create a testbench and show the simulation results.

1. **[10 Marks]** Implement a 16x4 priority encoder design. All values at inputs should be handled appropriately.

2. **[20 Marks]** Write a Verilog code for a 4-bit shift and add multiplier. (Do not use the in-built multiplier function *). Assume unsigned numbers.