ES215: Semester II [2021-2022]
Assignment 3
Due Date: 10-04-2022 (11:59pm) 100 points

Note: Make appropriate assumptions when required. State your assumptions, which do not contradict what has been given in the problem statement, clearly along with your solutions. Late assignments will not be graded. Please type up the solutions and submit them in PDF format. The source files have to be submitted separately. Please upload all the assignments in Google Classroom. Please follow the honor code. Any violations will have severe repercussions.

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1. Consider the individual stages of the Datapath have the following latencies: (**50 pts**)

IF	ID	EX	MEM	WB
200ps	100ps	200ps	400ps	100ps

Further, consider that the program with 1Million instructions has the following mix of instructions executed:

ALU	BEQ	LW	SW
50%	20%	15%	15%

   a. What is the best clock cycle time and clock frequency achievable in a single-cycle, multi-cycle and pipelined processors? (**15 pts**)
   b. What is the total latency of an LW instruction in a single-cycled, multi-cycle and pipelined processors? (**5 pts**)
   c. What is the speedup achieved by the Pipelined and Multi-cycle processors over a single cycle processor, if any? (**15 pts**)
   d. Further, if we assume that intermediate buffers in the pipeline stage consume a non-negligible time of 10ps. What would be the overall impact on the speedup (baseline being single-cycle processor)? (**15 pts**)

2. As an architect, you are requested to recommend on the pipelining strategy for custom ASIC based processors. Due to price and power constraints, it has been decided that the chip will not have any cache, but be able to simultaneously access Instruction and Data from memory in 1000ps. Register read, register write, and ALU operations all take up 100ps. Also, it has been decided that at-most one forwarding/bypassing unit can be implemented to detect and avoid the data hazards and the latency overhead for each pipelining stage to be 100ps. Consider the sample application to be a very small program with less than 20 instructions. (**30 pts**)

a. What is the performance for single cycle & multicycle design? (**10 pts**)

b. What would be the performance if you were to design a five-stage pipeline as discussed in the classroom? (**10 pts**)

c. Is there a better alternative? What would you recommend for pipeline design? (**10 pts**)

3. Consider a pipelined processor with stages IF, ID, EX, MEM, WB and consider the following sequence of instructions: (**25 pts**)

```
add $s0, $t0, $t1
add $s0, $s0, $t2
add $s1, $s1, $s0.
```

Now, compute the execution time for the following cases.

(a) Case 1: WB takes the entire cycle for register update. (**5 pts**)
(b) Case 2: WB finishes register update in the first half of the cycle and ID can read the register in the second half of the same cycle. (**5 pts**)
(c) Case 3: EX can directly use the result in the next cycle (forwarding). (**5 pts**)
(d) Calculate the speedup for the Case 2 and Case 3 with respect to Case 1. (**5 pts**)