



# Daozheng Xue

✉ 120602715@sjtu.edu.cn

X @Daozheng\_Xue

## **Education**

**Aug 2023 – present** **Shanghai Jiao Tong University.**  
B.S. in Computer Science, ACM Honors Class.  
**ACM Honors Class** is an elite CS program in SJTU for students ranked in the top 2% with aspirations in research.

## Research Interest

My research aims to explore more efficient and powerful Artificial Intelligence systems, with broad interests in machine learning and a current focus on efficient deep learning architectures.

## **Research Experience**

Jun. 2025 – Present	<p><b>Shanghai Jiao Tong University</b> <i>Research Intern at the SJTU LUMIA Lab, advised by Prof. Zhouhan Lin.</i></p> <p><b>Hierarchical Models Interacting with High-level Abstract Concepts</b> Explored concept representations beyond the token level, aiming to design hierarchical architectures capable of utilizing high-level abstract concepts.</p>
---------------------	-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

## Research Publications

## Journal Articles

- 1 Beiya Dai, Yuliang Liu, Daozheng Xue, Qipeng Guo, Kai Chen, Xinbing Wang, Bowen Zhou, and Zhouhan Lin. *Context-level Language Modeling by Learning Predictive Context Embeddings*. 2025. arXiv: 2510.20280 [cs.CL]. URL: <https://arxiv.org/abs/2510.20280>.

## Personal Projects

Mar. 2025	<b>Linear Crossformer</b> An Incremental Try For Crossformer Introduce the basic linear attention to enhance the efficiency and performance of origin Crossformer	Course Project of Machine Learning
June. 2025	<b>No-Linear attention</b> The attempt to introduce the nonlinear component to the traditional linear attention	Course Project of large language model
Feb. 2025	<b>MY OS</b> An operating system on RISC-V platform finishing by RUST. Implement a microkernel with shell and basic file system.	Course Project of Operating System
Dec. 2024	<b>MY CPU</b> A RISC-V General Purpose CPU with Thomaslo architecture(Verilog).	Course Project of Computer Architecture

## Personal Projects (continued)

Aug. 2024	<b>MY Compiler</b> A compiler for Mx (a C-like educational programming language) to RISC-V backend	Course Project of Compiler
-----------	-------------------------------------------------------------------------------------------------------	----------------------------

## Awards

2024-2025	<b>Zhiyuan Honor Scholarship</b> Awarded to top 2% students in SJTU annually	Zhiyuan Colledge, SJTU
	<b>Academic Excellence Scholarship</b> Awarded to students with top academic performance in SJTU	SJTU

## Skills

Programming	C/C++, Python, Java, Verilog , Rust
Tools	Git, Docker, LaTeX, Markdown