In IA-32 architecture along with the general flags, which of the following conditional flags are provided?

A. TF

B. IOPL

C. IF

D. All of the mentioned

Which method of representation has two representations for ‘0’?

A. Sign-magnitude

B. 1’s complement

C. 2’s complement

D. None of the mentioned

Who developed the basic architecture of computer?

A. Blaise Pascal

B. Charles Babbage

C. John Von Neumann

D. None of the above

In some pipelined systems, a different instruction is used to add to numbers which can affect the flags upon execution. That instruction is _____

A. AddSetCC

B. AddCC

C. Add++

D. SumSetCC

Which method/s of representation of numbers occupies a large amount of memory than others?

A. Sign-magnitude

B. 1’s complement

C. 2’s complement

D. 1’s & 2’s compliment

Which of the following format is used to store data?

A. Decimal

B. Octal

C. BCD

D. Hexadecimal

When we subtract -3 from 2, the answer in 2's complement form is _____

A. 0001

B. 1101

C. 0101

D. 1001

The processor keeps track of the results of its operations using flags called _____

A. Conditional code flags

B. Test output flags

C. Type flags

D. None of the mentioned

The IA-32 system follows which of the following design?

A. CISC

B. SIMD

C. RISC

D. None of the mentioned

What does CSA stands for?

A. Computer Service Architecture

B. Computer Speed Addition

C. Carry Save Addition

D. None of the mentioned

Which of the following is a combinational logic circuit that has 2n input lines and a single output line?

A. Multiplexer

B. Demultiplexer

C. Encoder

D. Decoder

Which of the following is the operation executed on data stored in registers?

A. Byte operation

B. Bit operation

C. Macrooperation

D. Microoperation

What is the content of stack pointer (SP)?

A. Address of the top element in the stack

B. Address of current instruction

C. Address of next instruction

D. None of the above

What is computer organization?

A. structure and behaviour of a computer system as observed by the user

B. structure of a computer system as observed by the developer

C. structure and behaviour of a computer system as observed by the developer

D. All of the mentioned

What does VLIW stands for?

A. Very Long Instruction Width

B. Very Large Instruction Word

C. Very Long Instruction Width

D. Very Long Instruction Word

Which of the following computer bus connects the CPU to a memory on the system board?

A. Expansion bus

B. Width bus

C. System bus

D. None of the above

Which of the following is a type of computer architecture?

A. Microarchitecture

B. Harvard Architecture

C. Von-Neumann Architecture

D. All of the mentioned

Computer address bus is -

A. Multidirectional

B. Bidirectional

C. Unidirectional

D. None of the above

The memory devices which are similar to EEPROM but differ in the cost effectiveness is _____

A. CMOS

B. Memory sticks

C. Blue-ray devices

D. Flash memory

The data is transferred over the RAMBUS as _____

A. Blocks

B. Swing voltages

C. Bits

D. Packets

Which of the following is a way in which the components of a computer are connected to each other?

A. Computer parts

B. Computer architecture

C. Computer hardware

D. None of the above

The bit used to signify that the cache location is updated is _____

A. Flag bit

B. Reference bit

C. Update bit

D. Dirty bit

When we perform subtraction on -7 and 1 the answer in 2's complement form is _____

A. 1010

B. 1110

C. 0110

D. 1000

In which of the following form the computer stores its data in memory?

In which of the following term the performance of cache memory is measured?

A. Chat ratio

B. Hit ratio

C. Copy ratio

D. Data ratio

In CISC architecture most of the complex instructions are stored in _____

A. CMOS

B. Register

C. Transistors

D. Diodes

In a 4M-bit chip organisation has a total of 19 external connections, then it has _____ address if 8 data lines are there.

A. 2

B. 5

C. 9

D. 8

Which of the following memory unit communicates directly with the CPU?

A. Auxiliary memory

B. Main memory

C. Secondary memory

D. None of the above

Which of the architecture is power efficient?

A. RISC

B. ISA

C. IANA

D. CISC

While using the direct mapping technique, in a 16-bit system the higher order 5 bits are used for _____

A. Id

B. Word

C. Tag

D. Block

Which of the following operations is/are performed by the ALU?

A. Data manipulation

B. Exponential

C. Square root

D. All of the above

Which of the following is the subcategories of computer architecture?

A. Microarchitecture

B. Instruction set architecture

C. Systems design

D. All of the mentioned

Which of the following computer memory is fastest?

A. Register

B. Hard disk

C. RAM

D. None of the above

Which of the following is page fault?

A. Page fault occurs when a program accesses a page of another program

B. Page fault occurs when a program accesses a page in main memory

C. Page fault occurs when there is an error in particular page

D. Page fault occurs when a program accesses a page which is not present in main memory

Which of the following architecture is suitable for a wide range of data types?

A. IA-32

B. ARM

C. ASUS firebird

D. 68000

What does EEPROM stands for?

A. Electrically Erasable and Programmable Read-Only Memory

B. Electronically Erasable and Programmable Read-Only Memory

C. Electrically Enabled and Programmable Read-Only Memory

D. None of the above

RISC stands for -

A. Reduce Instruction Set Computer

B. Risk Instruction Sequential Compilation

C. Risk Instruction Source Compiler

D. None of the above

The address in the main memory is known as -

A. Logical address

B. Physical address

C. Memory address

D. None of the above

If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have _____ A Generation word

A. Exception handling

B. Imprecise exceptions

C. None of the mentioned

Which of the following is a combinational logic circuit which converts binary information from n coded inputs to a maximum of 2n unique outputs?

A. Multiplexer

B. Demultiplexer

C. Encoder

D. Decoder

For a given FINITE number of instructions to be executed, which architecture of the processor provides for a faster execution?

A. ANSA

B. Super-scalar

C. ISA

D. All of the mentioned

If the instruction Add R1, R2, R3 is executed in a system which is pipelined, then the value of S is (Where S is term of the Basic performance equation).

A. 2

B. ~1

C. ~7

D. 2

Which of the following is the function of the control unit in the CPU?

A. It stores program instruction

B. It decodes program instruction

C. It performs logic operations

D. None of the above

Which of the following topology is used in Ethernet?

An n-bit microprocessor has -

A. n-bit instruction register

B. n-bit address register

C. n-bit program counter

D. None of the above

The status bit is also called as -

A. Unsigned bit

B. Signed bit

C. Flag bit

D. None of the above

Which of the following is a combinational logic circuit which sends data from a single source to two or more separate destinations?

A. Multiplexer

B. Demultiplexer

C. Encoder

D. Decoder

Which of the following computer register collects the result of computation?

A. Accumulator

B. Instruction Pointer

C. Storage register

D. None of the above

In order to read multiple bytes of a row at the same time, we make use of _____

A. Memory extension

B. Cache

C. Shift register

D. Latch

What does DRAM stands for?

A. Dynamic Read Access Memory

B. Digital Random-Access Memory

C. Dynamic Random-Access Memory

D. Dynamic Read Allocation Memory

Which of the following is a combinational logic circuit that change the binary information into N output lines?

A. Multiplexer

B. Demultiplexer

C. Encoder

D. Decoder

The difference in the address and data connection between DRAM's and SDRAM's is _____

A. The requirement of more address lines in SDRAM's

B. The usage of a buffer in SDRAM's

C. The usage of more number of pins in SDRAM's

D. None of the mentioned

Which of the following register can interact with the secondary storage?

A. PC

B. MAR

C. MDR

D. IR

The register used to store the flags is called as _____

A. Flag register

B. Status register

C. Test register

D. Log register

The drawback of building a large memory with DRAM is _____

_____ are the different type/s of generating control signals.

A. Hardwired

B. Micro-instruction

C. Micro-programmed

D. Both Micro-programmed and Hardwired

Which of the following allows simultaneous write and read operations?

A. ROM

B. EROM

C. RAM

D. None of the above

The reason for the cells to lose their state over time is _____

A. Use of Shift registers

B. The lower voltage levels

C. Usage of capacitors to store the charge

D. None of the mentioned

Which of the following is correct about memory and storage?

A. Memory is temporary, Storage is temporary

B. Memory is temporary, Storage is permanent

C. Memory is permanent, Storage is temporary

D. Memory is slow, Storage is Fast

In IA-32 architecture along with the general flags, which of the following conditional flags are provided?

A. TF

B. IOPL

C. IF

D. All of the mentioned

Which method of representation has two representations for ‘0’?

A. Sign-magnitude

B. 1’s complement

C. 2’s complement

D. None of the mentioned

Which method of representation has two representations for ‘0’?

A. Sign-magnitude

B. 1’s complement

C. 2’s complement

D. None of the mentioned

Which method of representation has two representations for ‘0’?

A. Sign-magnitude

B. 1’s complement

C. 2’s complement

D. None of the mentioned

Who developed the basic architecture of computer?

A. Blaise Pascal

B. Charles Babbage

C. John Von Neumann

D. None of the above

In a 4M-bit chip organisation has a total of 19 external connections, then it has _____ address if 8 data lines are there.

A. 2

B. 5

C. 9

D. 8

If the instruction Add R1, R2, R3 is executed in a system which is pipelined, then the value of S is (Where S is term of the Basic performance equation).

A. 2

B. ~1

C. ~7

D. 2

If the instruction Add R1, R2, R3 is executed in a system which is pipelined, then the value of S is (Where S is term of the Basic performance equation).

A. 2

B. ~1

C. ~7

D. 2

If the instruction Add R1, R2, R3 is executed in a system which is pipelined, then the value of S is (Where S is term of the Basic performance equation).

A. 2

B. ~1

C. ~7

D. 2

The drawback of building a large memory with DRAM is _____ Blank 1. Fill in the blank, read surrounding text.

Answers

Here are the answers to your queries about computer architecture and systems:

1. In IA-32 architecture, along with the general flags, which of the following conditional flags are provided?

- Answer: D. All of the mentioned

2. Which method of representation has two representations for '0'?

- Answer: B. 1’s complement

3. Who developed the basic architecture of a computer?

- Answer: C. John Von Neumann

4. In some pipelined systems, a different instruction is used to add two numbers which can affect the flags upon execution. That instruction is:

- Answer: B. AddCC (This seems to be a specific term used in certain contexts; generally, in pipelining, instructions like "add" can set condition codes, but the specific term "AddCC" is less standard.)

5. Which method/s of representation of numbers occupies a large amount of memory than others?

- Answer: D. 1’s & 2’s complement (This is somewhat subjective; in general, the memory occupied depends more on the bit width than the number representation system.)

6. Which of the following formats is used to store data?

- Answer: C. BCD

7. When we subtract -3 from 2, the answer in 2’s complement form is:

- Answer: B. 1101

8. The processor keeps track of the results of its operations using flags called:

- Answer: A. Conditional code flags

9. The IA-32 system follows which of the following designs?

- Answer: A. CISC

10. What does CSA stand for?

- Answer: C. Carry Save Addition

11. Which of the following is a combinational logic circuit that has 2^n input lines and a single output line?

- Answer: A. Multiplexer

12. Which of the following is the operation executed on data stored in registers?

- Answer: D. Microoperation

13. What is the content of the stack pointer (SP)?

- Answer: A. Address of the top element in the stack

14. What is computer organization?

- Answer: C. structure and behaviour of a computer system as observed by the developer

15. What does VLIW stand for?

- Answer: D. Very Long Instruction Word

16. Which of the following computer buses connects the CPU to memory on the system board?

- Answer: C. System bus

17. Which of the following is a type of computer architecture?

- Answer: D. All of the mentioned

18. Computer address bus is:

- Answer: C. Unidirectional

19. The memory devices which are similar to EEPROM but differ in cost-effectiveness are:

- Answer: D. Flash memory

20. The data is transferred over the RAMBUS as:

- Answer: D. Packets

21. Which of the following is a way in which the components of a computer are connected to each other?

- Answer: B. Computer architecture

22. The bit used to signify that the cache location is updated is:

- Answer: D. Dirty bit

23. When we perform subtraction on -7 and 1 the answer in 2's complement form is:

- Answer: B. 1110

24. In which of the following form does the computer store its data in memory?

- The question seems incomplete. Generally, computers store data in binary form in memory.

25. In which of the following term is the performance of cache memory measured?

- Answer: B. Hit ratio

26. In CISC architecture, most of the complex instructions are stored in:

- Answer: B. Register

27. In a 4M-bit chip organization that has a total of 19 external connections, it has _____ address if 8 data lines are there.

- Answer: C. 9 (11 address lines + 8 data lines = 19 total connections)

28. Which of the following memory units communicates directly with the CPU?

- Answer: B. Main memory

29. Which of the architectures is power efficient?

- Answer: A. RISC

30. While using the direct mapping technique, in a 16-bit system the higher order 5 bits are used for:

- Answer: C. Tag

31. Which of the following operations is/are performed by the ALU?

- Answer: D. All of the above

32. Which of the following are the subcategories of computer architecture?

- Answer: D. All of the mentioned

33. Which of the following computer memory is fastest?

- Answer: A. Register

34. Which of the following is a page fault?

- Answer: D. Page fault occurs when a program accesses a page which is not present in main memory

35. Which of the following architecture is suitable for a wide range of data types

?

- Answer: B. ARM

36. What does EEPROM stand for?

- Answer: A. Electrically Erasable and Programmable Read-Only Memory

37. RISC stands for:

- Answer: A. Reduced Instruction Set Computer

38. The address in the main memory is known as:

- Answer: B. Physical address

39. If an exception is raised and the succeeding instructions are executed completely, then the processor is said to have:

- Answer: B. Imprecise exceptions

40. Which of the following is a combinational logic circuit which converts binary information from n coded inputs to a maximum of 2^n unique outputs?

- Answer: C. Encoder

41. For a given finite number of instructions to be executed, which architecture of the processor provides for a faster execution?

- Answer: B. Super-scalar

42. If the instruction Add R1, R2, R3 is executed in a system which is pipelined, then the value of S is (Where S is a term of the Basic performance equation).

- Answer: B. ~1 (This assumes ideal conditions in pipelining where each stage of the pipeline takes approximately the same amount of time.)

43. Which of the following is the function of the control unit in the CPU?

- Answer: B. It decodes program instructions

44. Which of the following topology is used in Ethernet?

- The question seems incomplete. Ethernet commonly uses star topology in modern networks.

45. An n-bit microprocessor has:

- Answer: D. None of the above (It generally has an n-bit data bus; the size of the instruction register, address register, and program counter can vary.)

46. The status bit is also called as:

- Answer: C. Flag bit

47. Which of the following is a combinational logic circuit which sends data from a single source to two or more separate destinations?

- Answer: B. Demultiplexer

48. Which of the following computer registers collects the result of computation?

- Answer: A. Accumulator

49. In order to read multiple bytes of a row at the same time, we make use of:

- Answer: C. Shift register

50. What does DRAM stand for?

- Answer: C. Dynamic Random-Access Memory

51. Which of the following is a combinational logic circuit that changes the binary information into N output lines?

- Answer: C. Encoder

52. The difference in the address and data connection between DRAM's and SDRAM's is:

- Answer: C. The usage of more number of pins in SDRAM's

53. Which of the following registers can interact with the secondary storage?

- Answer: B. MAR (Memory Address Register)

54. The register used to store the flags is called as:

- Answer: A. Flag register

55. The drawback of building a large memory with DRAM is:

- The question seems incomplete. One potential answer could be "higher latency and refresh requirements compared to SRAM."

56. _____ are the different type/s of generating control signals.

- Answer: D. Both Micro-programmed and Hardwired

57. Which of the following allows simultaneous write and read operations?

- Answer: C. RAM

58. The reason for the cells to lose their state over time is:

- Answer: C. Usage of capacitors to store the charge

59. Which of the following is correct about memory and storage?

- Answer: B. Memory is temporary, Storage is permanent

Please note that some of these answers may vary depending on the specific context or source material you are using.