# 7

# FIELD EFFECT TRANSISTOR

## 7.1. INTRODUCTION

In the previous unit, we have studied about Bipolar Junction (BJT). We discussed several configurations and operating regions alongwith concerned biasing techniques. The forthgoing unit describes another class of transistors, the field-effect transistors abbreviated as FET. The FET is also a three terminal device. It has got numerous applications in electronic circuits like BJT. There are several similarities and dissimilarities between FET and BJT. Constructional features, operating mechanism and performance characteristics differ greatly from those of BJTs.

The main difference between BJT and FET is that former has got two junctions ($J_E$ and $J_C$) but later has no any junction. Because of this advantage, several qualities have been enhanced in the transistors which were lacking in BJT. Another interesting difference between the BJT and FET is that a bipolar junction transistor is a current-current device. That is why, the output characteristics of this device are controlled by the base current and not by the base voltage. While the FET is a voltage-controlled device. That is why, the ouput characteristics of FET are controlled by input voltage and not by the input current. In this unit, we will study about the FET and BJT comparatively and will be able to know why and how FET replaced the BJT in most specific applications.

## 7.2. CLASSIFICATION OF FIELD-EFFECT DEVICES

Depending upon the constructional features and operating principles, FETs broadly classified in two main types field-effect transistors.

1. Junction field-effect transistor (JFET)
2. Metal oxide semiconductor field-effect transistor (MOSFET) or insulated gate field-effect transistor (IGFET).

Both of these type further divided into *n*-channel and *p*-channel. For better understanding about the classification tree form is shown below in Fig. 7.1.

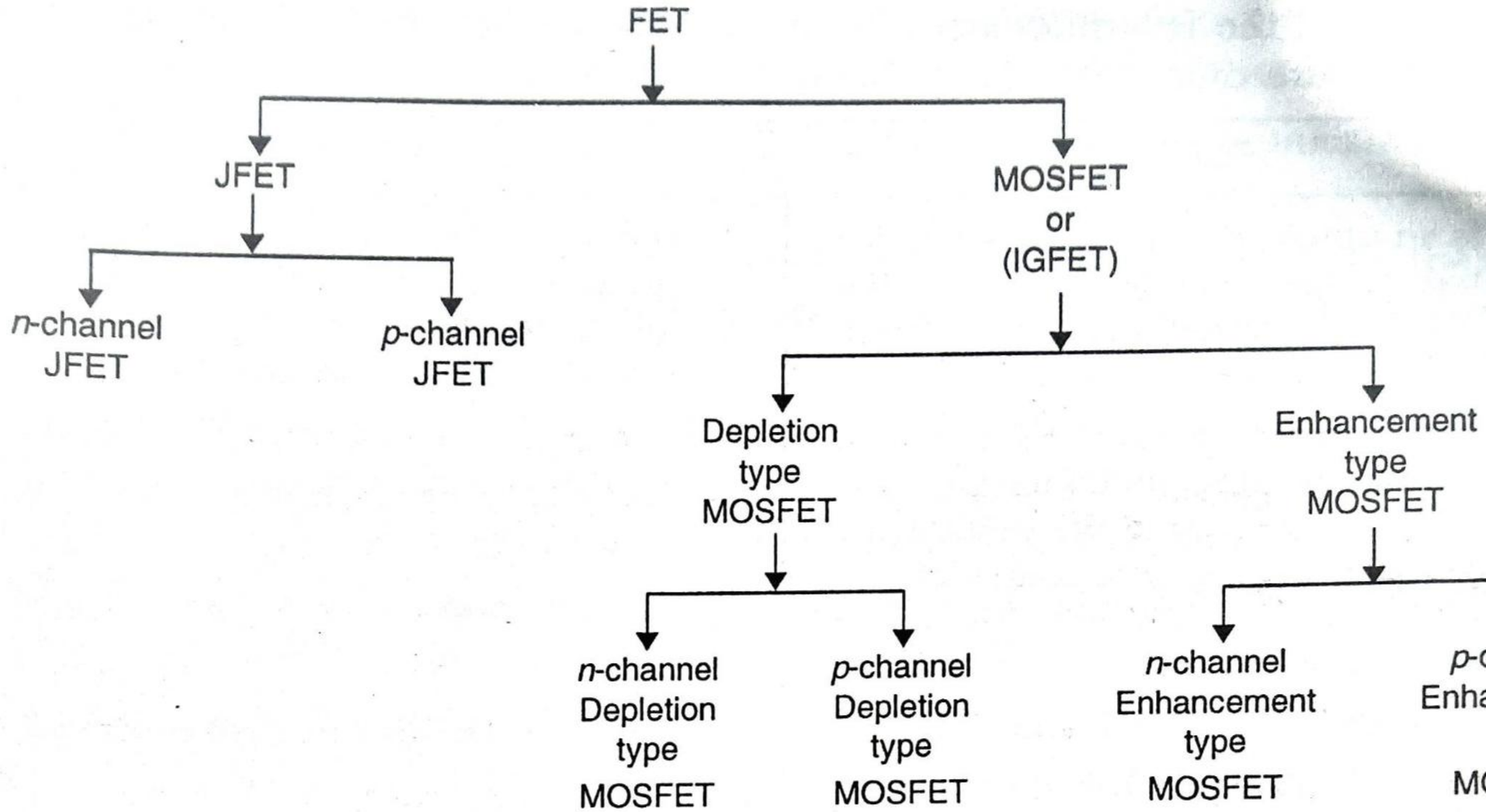



**Fig. 7.1.** *Different types of field effect transistors.*

## 7.1 Introduction

- The Field Effect Transistor abbreviated as **FET** is an another semiconductor device like a BJT which can be used as an amplifier or switch. Like BJT, FET is also a three terminal device; however, the principle of operation of FET is completely different from that of BJT.
- The three terminals of FET are named as Drain (D), Source (S) and Gate (G), as shown in the Fig. 7.1.1. Out of these three terminals gate terminal acts as a controlling terminal.

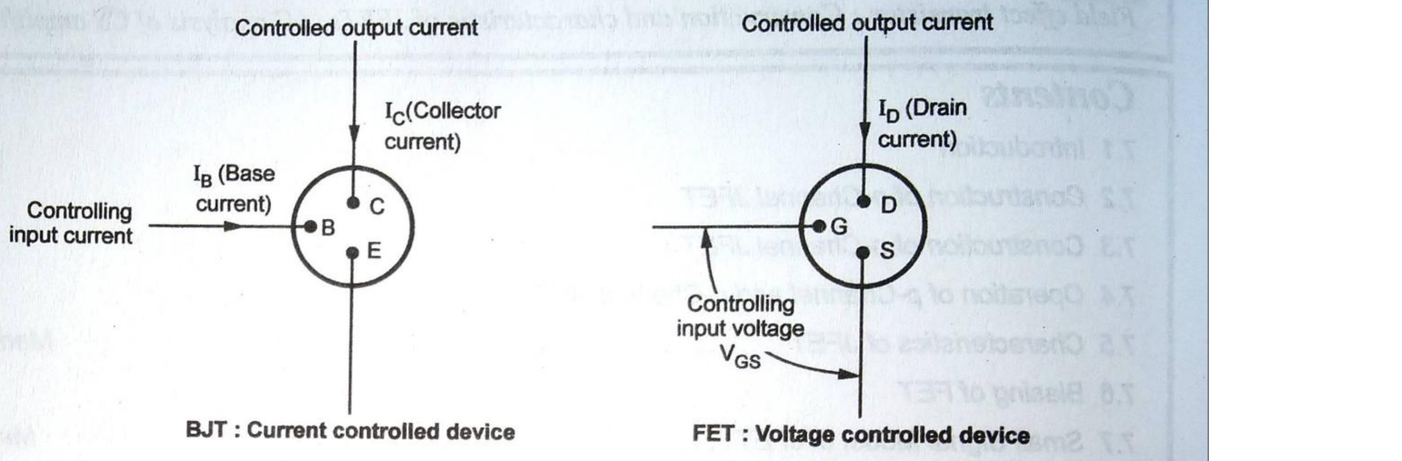



**Fig. 7.1.1 Controlling element for BJT and FET**

### Important features of FET

- **Voltage Controlled Device :** As shown in the Fig. 7.1.1, in BJT the output current, $I_C$ is controlled by the base current $I_B$. Hence BJT is a current controlled device. On the other hand, in FET, the voltage applied between gate and source ($V_{GS}$) controls the drain current $I_D$. Therefore, FET is a voltage controlled device.
- The name **field effect** is derived from the fact that the output current flow is controlled by an electric field set up in the device by an externally applied voltage between gate and source terminals.
- **Unipolar Device :** We know that in BJT, the current is carried by both electrons and holes, and hence the name "**bipolar**" junction transistor. However in FET, current is carried by only one type of charge particles, either electrons or holes. Hence FET is called **unipolar device**.
- Like BJT, the parameters of FET are also temperature dependent. In FET, as temperature increases drain resistance also increases, reducing the drain current. Thus unlike BJT, thermal runaway does not occur with FET. Thus we can say that FET is **more temperature stable** as compared to the BJT.

- **FET has very high input impedance.** Typically, it is in the range of one to several megaohms. Because FETs have higher input impedance than BJT they are preferred in amplifiers where high input impedance is required.
- **FETs require less space** than that for BJTs, hence they are preferred in integrated circuits.

## 7.2 Construction of n-Channel JFET

- The Fig. 7.2.1 shows structure and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n type is taken and at its two ends, two ohmic contacts are made which are the drain and source terminals of FET.

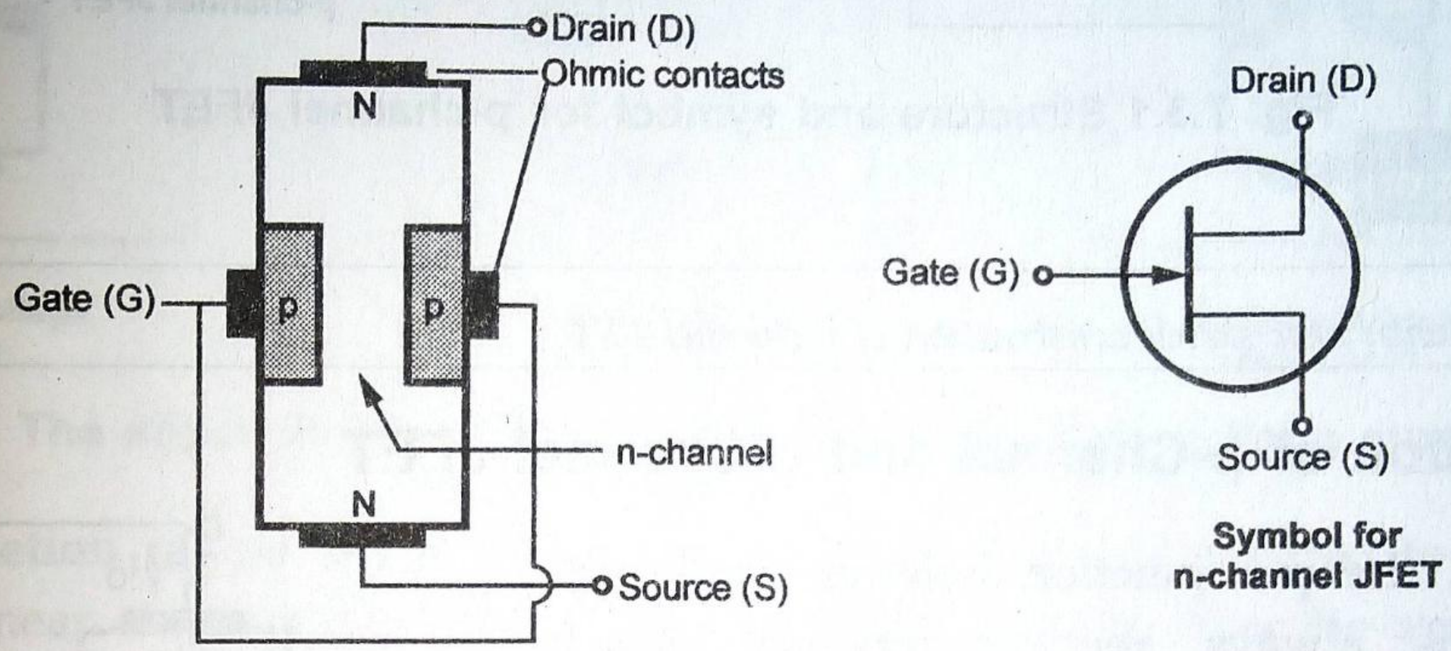



**Fig. 7.2.1 Structure and symbol for n-channel JFET**

- Heavily doped electrodes of p type material form p-n junctions on each side of the bar. The thin region between the two p gates is called the **channel**. Since this channel is in the n type bar, the FET is known as **n-channel JFET.**
- The electrons enter the channel through the terminal called **source** and leave through the terminal called **drain**. The terminals taken out from heavily doped electrodes of p type material are called **gates**. Usually, these electrodes are connected together and only one terminal is taken out, which is called **gate**, as shown in the Fig. 7.2.1.

## 7.3 Construction of p-Channel JFET

- The device could be made of p type bar with two n type gates as shown in the Fig. 7.3.1. Then this will be **p-channel JFET.**
- The principle of working of n-channel JFET and p-channel JFET is similar; the only difference being that in **n-channel JFET** the current is carried by electrons while in **p-channel JFET,** it is carried by holes.

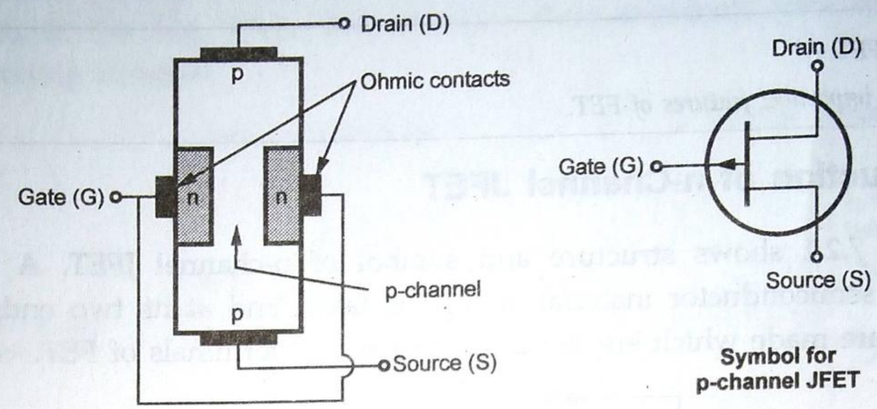



**Fig. 7.3.1 Structure and symbol for p-channel JFET**

**Review Question**

1. *Explain with neat sketch construction of p-channel FET.*

## 7.4 Operation of p-Channel and n-Channel JFET

- In JFET, the p-n junction between gate and source is always kept in reverse biased conditions. Since the current in a reverse biased p-n junction is extremely small, practically zero; the gate current in JFET is often neglected and assumed to be zero.
- Let us consider the circuit shown in Fig. 7.4.1. As shown in Fig. 7.4.1, voltage $V_{DD}$ is applied between drain and source. Gate terminal is kept open. The bar is of n-type material.

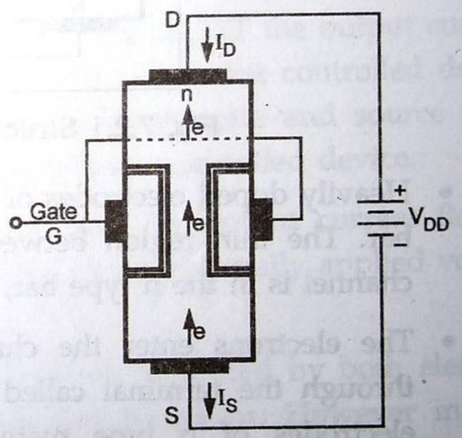
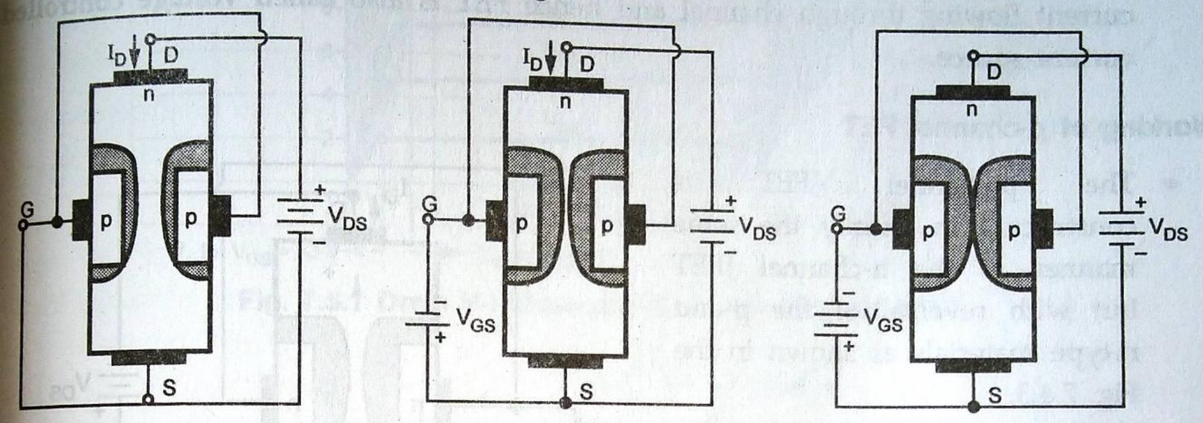



**Fig. 7.4.1 JFET with gate open and $V_{DD}$ is applied between drain and source**

- Due to the applied voltage, the majority carriers i.e. the electrons start flowing from the source to the drain. This flow of electrons makes the drain current, $I_D$.
- The majority carriers (electrons in n-channel JFET and holes in p-channel JFET) move from source to drain through the space between the gate regions. This space

is commonly known as **channel**. The width of this channel can be controlled by varying the gate voltage.

- Fig. 7.4.2 (a) shows that an n-channel JFET with the gate directly connected to the source terminal. When drain voltage $V_{DS}$ is applied, a drain current $I_D$ flows in the direction shown. Since the n-material is resistive, the drain current causes a voltage drop along the channel. This voltage drop reverse biases the pn junctions, and causes the depletion regions to penetrate into the channel. Since gate is heavily doped and the channel is lightly doped, the width of the depletion region will mainly be spread in the channel shown in the Fig. 7.4.2 (a). This penetration depends on the reverse bias voltage.




(a) No bias voltage on gates

(b) Small negative gate source bias

(c) Large negative gate source bias

**Fig. 7.4.2 The effect of gate voltage on channel-width and on drain current $I_D$**

- The **depletion region width** is more at the drain side as compared to source side because near the junction, voltage at drain side is more than the voltage at the source side. This shows that reverse bias is not uniform near the junction; it gradually increases from source side to drain side.

**JFET as voltage controlled current source**

- The depletion region does not contain charge carriers, the space between two depletion regions is available for the conducting portion of the channel. If we externally apply reverse bias voltage to the gate, the reverse bias will further increase and hence increase the penetration of the depletion region, which reduces the width of the conducting portion of the channel. As width of the conducting portion of the channel reduces, the number of electrons flowing from source to drain reduces and hence the current flowing from drain to source reduces.
- If we go on increasing the reverse bias voltage to the gate as shown in Fig. 7.4.2 (b) and (c), depletion regions will increase more and more, and stage will come when the width of the depletion regions will be equal to the original

width of the channel, leaving zero width for conducting portion of the channel. This will prevent any current flow from drain to source and hence cut off the drain current. The gate to source voltage that produces cut-off is known as **cut-off voltage** and it is denoted by $V_{GS(off)}$.

- When the gate is shorted to source, there is minimum reverse bias between gate and source p-n junction, making depletion region width minimum and conducting channel width maximum. In this case maximum drain current flows which is designated by $I_{DSS}$.
- From above discussion it is cleared that the gate to source voltage controls the current flowing through channel and hence FET is also called **voltage controlled current source.**

**Working of p-channel FET**

- The p-channel JFET is constructed in exactly the same manner as the n-channel JFET but with reversal of the p-and n-type materials as shown in the Fig. 7.4.3.
- All current directions and voltage polarities are reversed
- For $V_{GS} = 0$, channel width is maximum. By increasing positive gate to source ($V_{GS}$) voltage, the channel width is reduced.

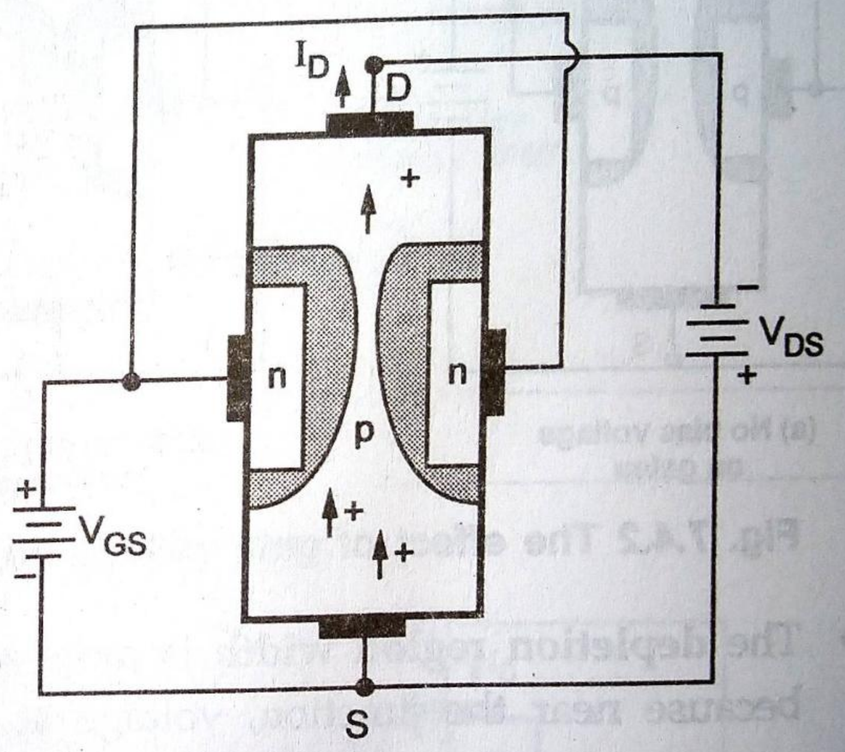



**Fig. 7.4.3 p-channel FET**