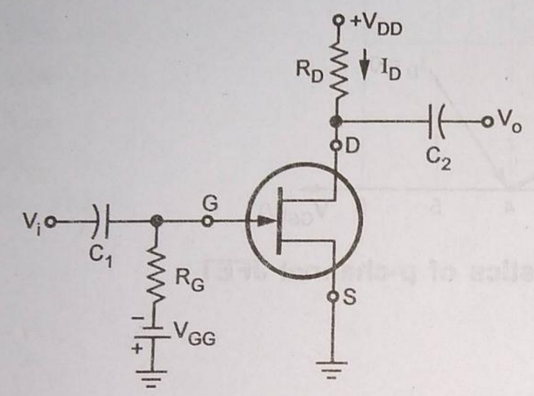
7.6 Biasing of FET

- Different biasing circuits of FET are :
  - Fixed bias circuit
  - Self bias circuit
  - Voltage divider bias circuit

7.6.1 Fixed-bias Circuit

- Fig. 7.6.1 shows the fixed bias circuit for the n-channel JFET. This is the simplest biasing arrangement.
- To make gate-source junction reverse-biased, a separate supply V_{GG} is connected such that gate is more negative than the source.
- For the d.c. analysis coupling capacitors are open circuits. The current through R_G is I_G which is zero.
- This permits R_G to replace by short circuit equivalent, simplifying the fixed bias circuit as shown in the Fig. 7.6.2



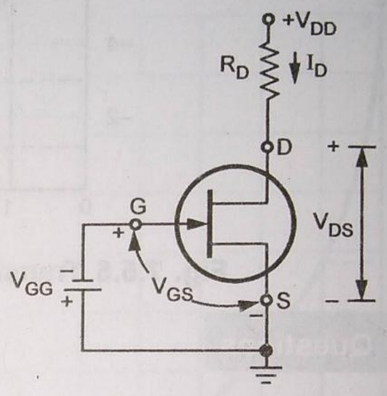


Fig. 7.6.1 Fixed bias circuit for n-channel circuit **Fig. 7.6.2 Simplified fixed bias circuit**

Step 1 : Calculate V_{GS}

- We know for d.c. analysis $I_G = 0$ A and applying KVL to the input circuit we get,

$$V_{GS} + V_{GG} = 0$$

$$\therefore \quad V_{GS} = -V_{GG} \qquad \ldots (7.6.1)$$

- Since V_{GG} is a fixed d.c. supply, the voltage V_{GS} is fixed in magnitude, and hence the name fixed bias circuit.

Step 2 : Calculate I_{DQ}

- The drain current I_D can be calculated using equation.

$$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Step 3 : Calculate V_{DS}

- The drain to source voltage of drain circuit can be determined by applying KVL.

$$V_{DD} - I_D R_D - V_{DSQ} = 0$$

$$\therefore \quad V_{DSQ} = V_{DD} - I_D R_D \qquad \ldots (7.6.2)$$

- The main drawback of fixed bias circuit of FET is that it requires two power supplies.

Example 7.6.1 *For the circuit shown in the Fig. 7.6.3, calculate :*

a) V_{GSQ}, *b)* I_{DQ},

c) V_{DSQ}, *d)* V_D

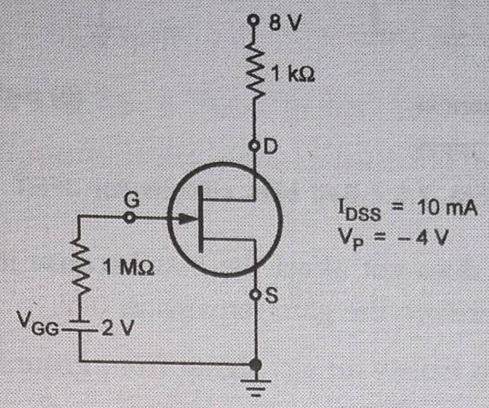


Fig. 7.6.3

Solution :

a) $V_{GSQ} = -V_{GG} = -2\ V$ $\quad \because I_G = 0$ and $I_G R_G = 0$

b) $$I_{DQ} = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 = 10 \times 10^{-3}\left(1 - \frac{-2\ V}{-4\ V}\right)^2$$

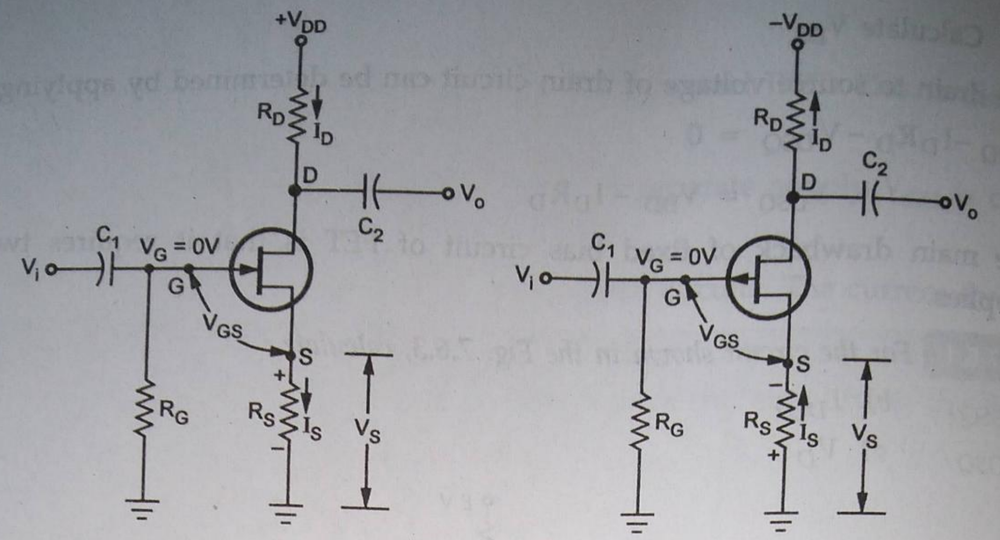
$$= 10 \times 10^{-3}\ (1 - 0.5)^2 = 10 \times 10^{-3}\ (0.25) = 2.5\ mA$$

c) $V_{DSQ} = V_{DD} - I_{DQ} R_D = 8\ V - 2.5 \times 10^{-3}\ (1 \times 10^3) = 5.5\ V$

d) $V_D = V_{DS} + V_S = 5.5 + 0 = 5.5\ V$

7.6.2 Self Bias Circuit

- Self bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate source junction is always reverse-biased.
- This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET. This can be achieved using the self bias arrangement shown in Fig. 7.6.4.



Note : $I_S = I_D$ in all JFETs

Fig. 7.6.4 Self bias circuits for JFET

- The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V.
- R_G is necessary only to isolate an a.c. signal from ground in amplifier applications.
- The voltage drop across resistor, R_S makes gate source junction reverse biased.

Step 1 : Obtain expression for V_{GS}

- For the n-channel FET in Fig. 7.6.4 (a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = I_S R_S = I_D R_S$. The gate to source voltage is,

$$V_{GS} = V_G - V_S = 0 - I_D R_S = - I_D R_S$$

- For the p-channel FET in Fig. 7.6.4 (b), I_S produces a voltage drop across R_S and makes the source negative with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then $V_S = - I_S R_S = - I_D R_S$. The gate to source voltage is

$$V_{GS} = V_G - V_S = 0 - (- I_D R_S) = + I_D R_S$$

- In the following D.C. analysis, the n-channel JFET shown in Fig. 7.6.4 (a) is used to for illustration.
- For D.C. analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent, since $I_G = 0$. This is illustrated in Fig. 7.6.5.

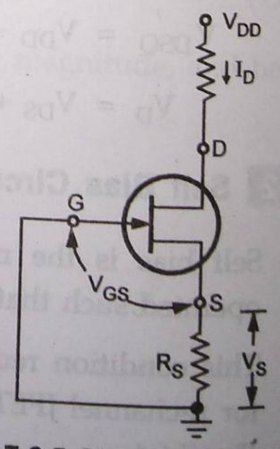


Fig. 7.6.5 Simplified self bias circuit for d.c. analysis

Step 2 : Calculate I_{DQ}

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_p}\right)^2 = I_{DSS}\left(1 + \frac{I_D R_S}{V_p}\right)^2 \quad \ldots (7.6.3)$$

Step 3 : Calculate V_{DS}

Applying KVL to the output circuit we get,

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore \quad V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D R_S - I_D R_D = V_{DD} - I_D (R_S + R_D)$$