Logic Gates

2.1 Introduction

A logic gate is a circuit that performs a logic function on a number of input binary signals. The logic gate is the building block from which many different kinds of logic circuit can be constructed. The signals at the input and output terminals of gate either at HIGH level voltage or at a LOW level. A gate will produce one output level whenever any other combination is present at the inputs. Logic gates are readily available in integrated circuit form, basic gates are AND, OR and NOT gate are available. The logic functions are defined by a truth table. This table, which lists all the possible combinations of the input variables applied to a gate and output variable. Each variable can only be at either 0 (logic 0 level) or 1 (logic 1 level).

The total number of possible combinations of binary inputs to a gate is determined by the following formula.

$$N = 2^n$$

Where N is the number of possible combinations
n is the number of bits.

For two variables : $N = 2^2 = 4$ combinations
For three variables : $N = 2^3 = 8$ combinations

2.2 AND Gate

Definition

Logic Gate An electronic circuit that performs a Boolean algebraic function

Truth Table A list of all possible input values to a digital circuit, listed in ascending binary order, and the output response for each input combination

AND Gate A logic circuit whose output is HIGH when all inputs are HIGH

The AND function combines two or more input variables so that the output is HIGH (1) only if all the inputs are HIGH (1). Figure 2.1 shows the symbol of AND gate and the truth table is shown in Table 2.1.

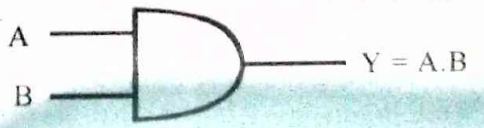


Fig. 2.1 Symbol of AND gate

Algebraically, this is written

$$Y = A \cdot B$$

Table 2.1 Truth table of AND gate

Inputs		Output
A	B	Y=A.B
0	0	0
0	1	0
1	0	0
1	1	1

We can also represent the AND functions as a set of switches in series as shown in Fig.2.2. The circuit consists of a voltage source, a lamp and two series switches.

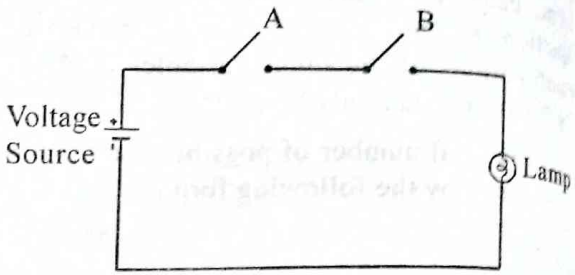


Fig. 2.2 AND function represented by switches

The lamp turns ON when switches A and B are both closed. For any other condition of the switches, the lamp is OFF.

Example 2.1

Draw the output pulse waveform of AND gate for the given input pulses A and B.

Solution:

The output of AND gate is HIGH only if all inputs are HIGH.

uring the period t_1, making the output HIGH (1)

During the time interval t_2, input A is LOW (0) and B is HIGH (1), so the output is LOW (0)

During the time interval t_3, both inputs are HIGH (1) so the output is HIGH (1).

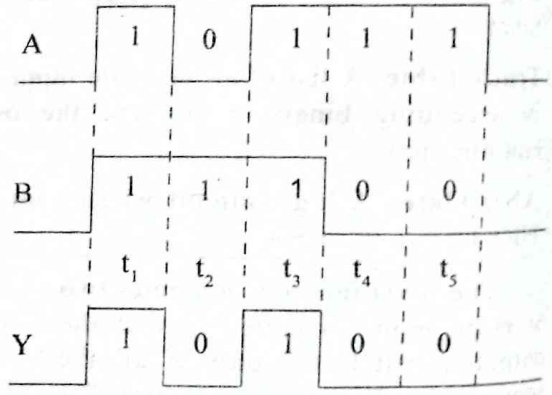


Fig. Ex. 2.1

During the time interval t_4, input A is HIGH (1) and input B is LOW (0), resulting in a LOW (0) output.

During the time interval t_5, input A is HIGH (1) input B is LOW (0) and the output is LOW (0)

2.3 OR Gate

Definition

OR Gate A logic circuit whose output is HIGH when atleast one input is HIGH

The OR function combines two or more input variables in such a way as to make the output variable HIGH (1) if atleast one input is HIGH. Figure 2.3 shows the symbol of OR gate and Table 2.2 shows the truth table of OR gate.

Fig. 2.3 Symbol of OR gate

Table 2.2 Truth Table of OR gate

Inputs		Output
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	1

The algebraic expression for the OR function is

$$Y = A + B$$

The OR function can be explained by a set of switches connected in parallel, as shown in Figure. 2.4. The lamp is ON when either switch A or switch B is closed.

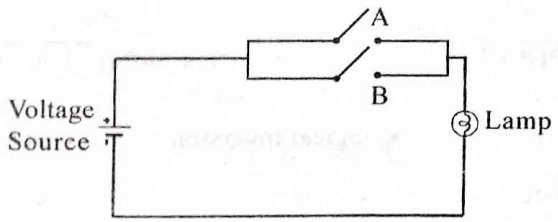


Fig. 2.4 OR function represented by switches

Example 2.2

Draw the output pulse to OR gate for the given input pulses.

Solution:

Inputs A and B are both HIGH (1) during the interval t_1, making the output is HIGH.

During the time interval t_2, input A is LOW (0) but the input B is HIGH (1) so the output pulse is HIGH (1).

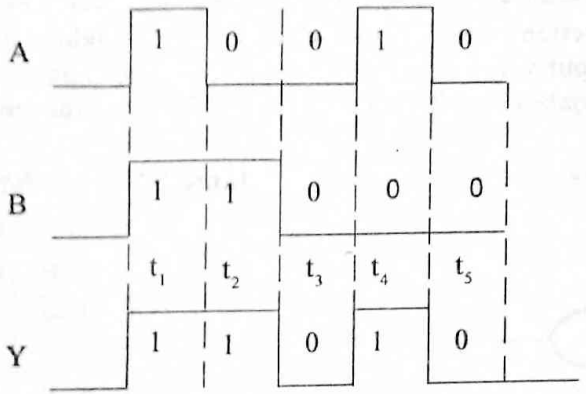


Fig. Ex. 2.2

During the time interval t_3, both inputs are LOW (0) so there is LOW (0) output during this time.

During time interval t_4, the output is HIGH (1) because input A is HIGH (1).

During time interval t_5, the output is LOW(0) because the inputs A and B are LOW (0).

2.4 NOT Gate

Definition

Inverter Also called a NOT gate or an inverting buffer. A logic gate that changes its input logic level to the opposite logic level.

Bubble A small circle indicating logical inversion on a circuit symbol.

The NOT gate (inverter) performs the operation called inversion or complementation. The inverter changes one logic level to the opposite logic level. In terms of bits, it changes a 1 to 0 and a 0 to 1. Figure 2.5 shows the symbol of NOT gate and Table 2.3 shows the truth table of NOT gate.

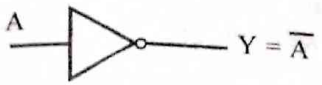


Fig. 2.5 Symbol of NOT gate

Table 2.3 Truth table of NOT gate

Input	Output
A	$Y=\overline{A}$
0	1
1	0

When a HIGH(1) level is applied to an inverter input, a LOW(0) level will appear on its output. When a LOW (0) level is applied to its input, a HIGH (1) will appear on its output.

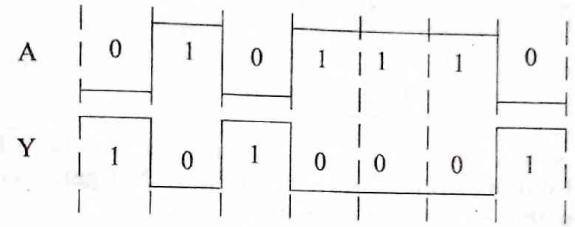
The NOT function is represented algebraically by the Boolean Expression

$$Y = \overline{A}$$

Example 2.3

The given wave form (A) is applied to the input of inverter gate. Determine the output wave form.

Solution :



2.5 Derived Logic Gates

The basic logic gates are AND, OR and NOT, can be combined to make any other logic functions. By using these basic gates, the following gates are obtained.

1. NAND gate
2. NOR gate
3. EX OR gate
4. EX NOR gate

2.6 The NAND Gate

Definition

NAND Gate A logic circuit whose output is LOW when all inputs are HIGH

The term NAND is a combination of NOT - AND and implies an AND function complemented output. The standard logic symbol for a 2 input NAND gate and its equivalent to an AND gate followed by an inverter as shown in Fig.2.6.

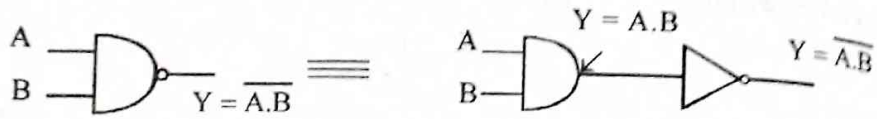


Fig. 2.6 Symbol of 2 input NAND gate and its equivalent

NAND gate produces a LOW (0) output only when all the inputs are HIGH (1). When any of the input is LOW, the output will be HIGH. The Table 2.4 shows the truth table of NAND gate.

Table 2.4 Truth table of NAND gate

Inputs		Output
A	B	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

TheNAND gates operation is the fact that one or more LOW inputs produce a HIGH output. From this viewpoint a NAND gate can be used for an OR operation that requires one or more LOW inputs produce a HIGH output. This aspect of NAND gate operation is referred to as Negative OR gate Figure 2.7 shows the NAND gate and equivalent of negative OR gate.

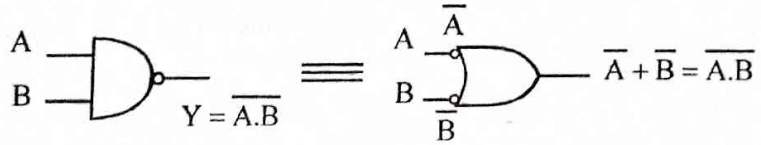


Fig. 2.7 NAND gates and equivalent of negative OR gate

Example 2.4

If the two wave forms A and B shown in Figure are applied to the NAND gate inputs, determine the output wave form of NAND gate.

Solution:

Output waveform Y is HIGH only during any input has LOW period.

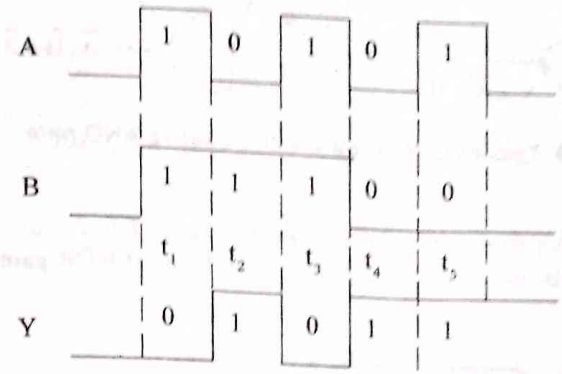


Fig. Ex. 2.4

2.7 The NOR Gate

Definition

NOR Gate A logic circuit whose output is LOW when any one inputs are HIGH

The term NOR is a contraction of NOT - OR and implies OR function with complemented output. The standard logic symbol for a two input NOR gate and equivalent OR gate followed by an NOT gate as shown in Fig. 2.8.

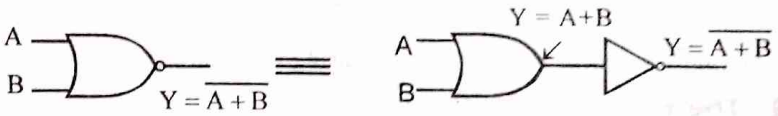


Fig. 2.8 Symbol of NOR gate and its equivalent

A NOR gate produces a LOW output when any of its inputs is HIGH. Only when all of its inputs are LOW the output is HIGH (1). The Table 2.5 shows the truth table of NOR gate.

A NOR gate, like NAND gate, has another aspect of its operation that is inherent in the way it logically functions. From the truth table of NOR gate, a HIGH produced on the gate output only if all of its inputs are LOW. From this situation, a NOR gate can be used for an AND operation that requires all LOW inputs to produce HIGH output. This aspect of NOR operation is called negative AND. Figure 2.9 shows the two input NOR gate with negative AND gate.

Table 2.5 Truth table of NOR gate

Inputs		Output
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 2.9 Two input NOR gate with negative AND gate

Example 2.5

If the two wave forms A and B shown in Figure Ex. 2.5 are applied to the NOR gate inputs, determine the output wave form of NOR gate.

Solution:

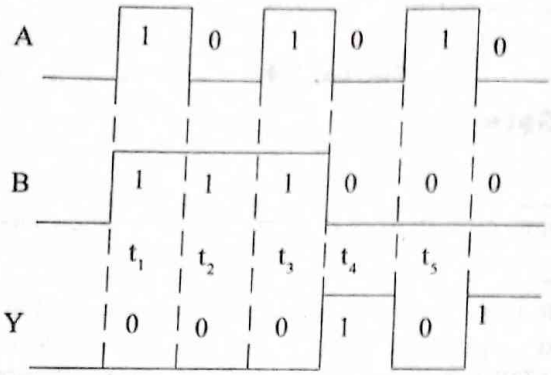


Fig. Ex. 2.5

Output waveform Y is HIGH only during all input has LOW.

2.8 The Exclusive OR Gate

Definition

Exclusive OR Gate A two input logic circuit whose output is HIGH when one input (but not both) is HIGH.

Standard symbol for an exclusive OR (XOR) gate is shown in Fig.2.10. The output of an exclusive OR gate is HIGH only when the two inputs are at opposite logic levels.

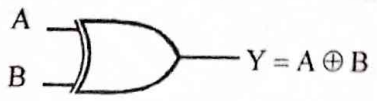


Fig. 2.10 Symbol of EX OR gate

Table 2.6 Truth table of EX OR gate

Inputs		Output
A	B	Y = A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

$$Y = \overline{A}B + A\overline{B} = A \oplus B$$

The truth table of the EX OR gate shows that the output is HIGH when any one of input is HIGH, but not all, of the inputs is at 1. This exclusive feature eliminates a similarity to the OR gate. The EXOR gate responds with a HIGH output only when an odd number of inputs is HIGH. When there is an even number of HIGH inputs such as two or four, the output will always be LOW. Figure 2.11 shows EXOR function by using AND -OR- NOT gates.

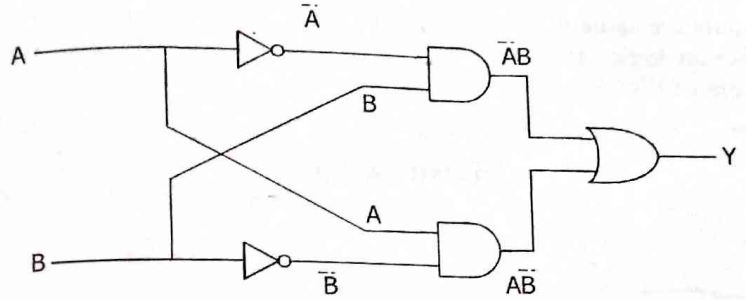


Fig. 2.11 Exclusive OR gate constructed using basic gates

Example 2.6

If the two wave forms A and B shown in Figure are applied to the EX OR gate inputs, determine the output wave form of EX OR gate.

Solution:

Output waveform Y is HIGH only during any odd number input has HIGH

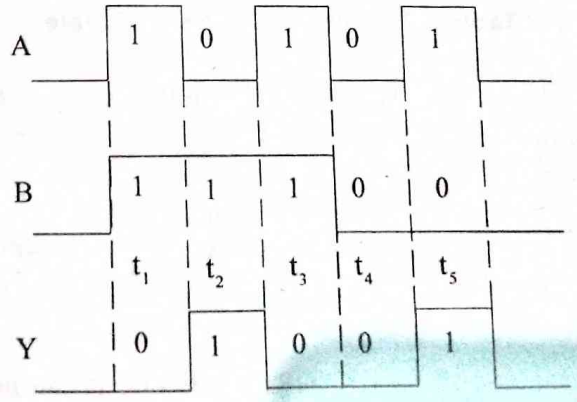


Fig. Ex. 2.6

2.9 The Exclusive NOR Gate

Definition

Exclusive NOR gate A two input logic circuit whose output is the complement of EX OR gate

The exclusive NOR gate, abbreviated EX NOR gate, is an EX OR gate followed by an NOT gate. An exclusive NOR gate has two or more inputs and one output. The output of a two input EX NOR gate, a HIGH state if both inputs are same logic level and the output is LOW when the both inputs are different logic states. Figure 2.12 shows the EX NOR gate symbol and equivalent of EXOR followed by NOT gate.

The expression of EX NOR gate is

$$Y = \overline{A}\overline{B} + AB = A \odot B$$

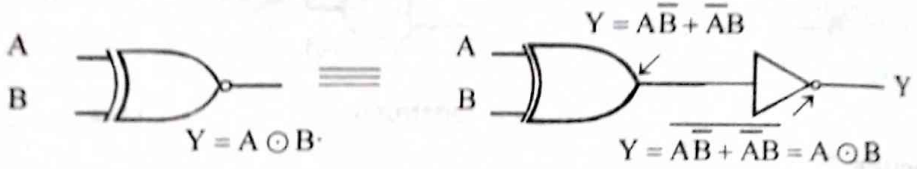


Fig. 2.12 Symbol of EX NOR gate and its equivalent

Table 2.7 shows the truth table of EX NOR gate. An important property of the EX NOR gate is that it can be used for bit comparison. The output of an EX NOR gate is 1 if both the inputs are similar, i.e., both inputs are 0 or 1. Otherwise, its output is 0. Hence, it can be used as a one bit comparator. It is also called a coincidence circuit.

Table 2.7 Truth table of EX NOR gate

Input		Output
A	B	$Y = A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1

Another property of the EXNOR gate is that it can be used as an even parity checker. The output of the EXNOR gate is 1 if the number of 1's in its inputs even, if the number of 1's is odd, the output is 0. Hence it can be used as an even/odd parity checker.

Example 2.7

If the two wave forms A and B shown in Figure Ex.2.7 are applied to the EX NOR gate inputs, determine the output wave form of EX-NOR gate.

Solution:

Output waveform Y is HIGH only during both input has LOW or HIGH period.

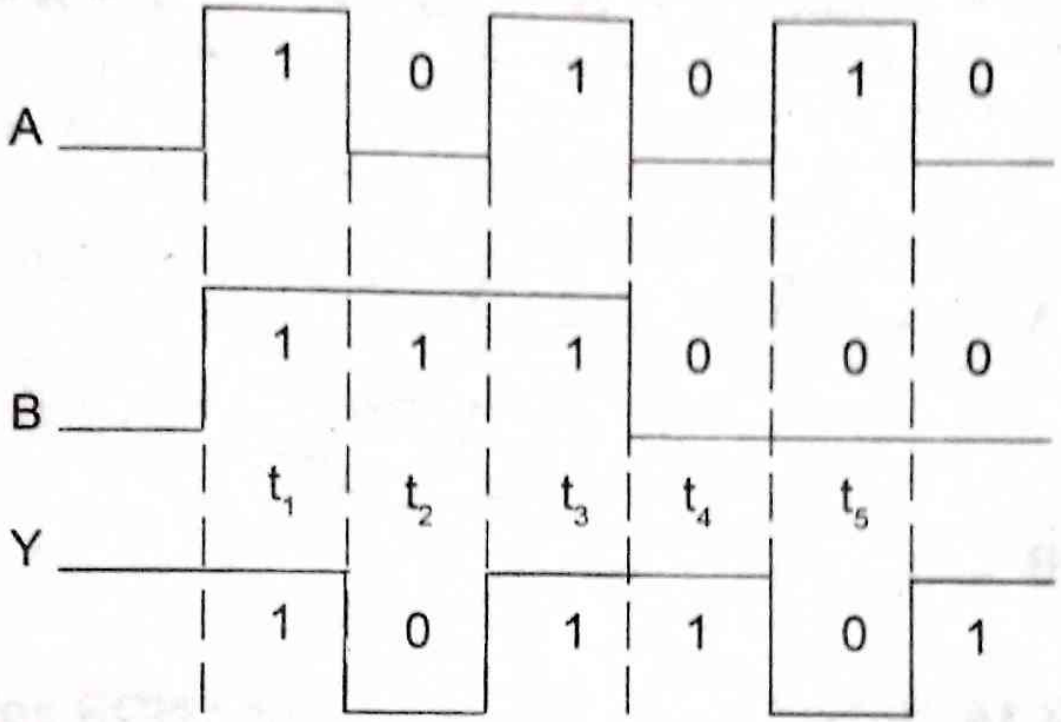


Fig. Ex. 2.7