7.5 Characteristics of JFET

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To understand electrical behaviour of a JFET, it is necessary to study the interrelation of the current and voltages in JFET. These relationships can be plotted graphically which are commonly known as the **characteristics of JFET**. The important characteristics of JFET are drain characteristics and transfer characteristics. The following section explains these characteristics in detail.

7.5.1 Drain Characteristics

- Fig. 7.5.1 shows the drain characteristics of a n-channel JFET. The curves represent relationship between the drain current I_D and drain to source voltage V_{DS} for different values of V_{GS}. Fig. 7.5.2 shows the experimental setup required to plot this characteristics.

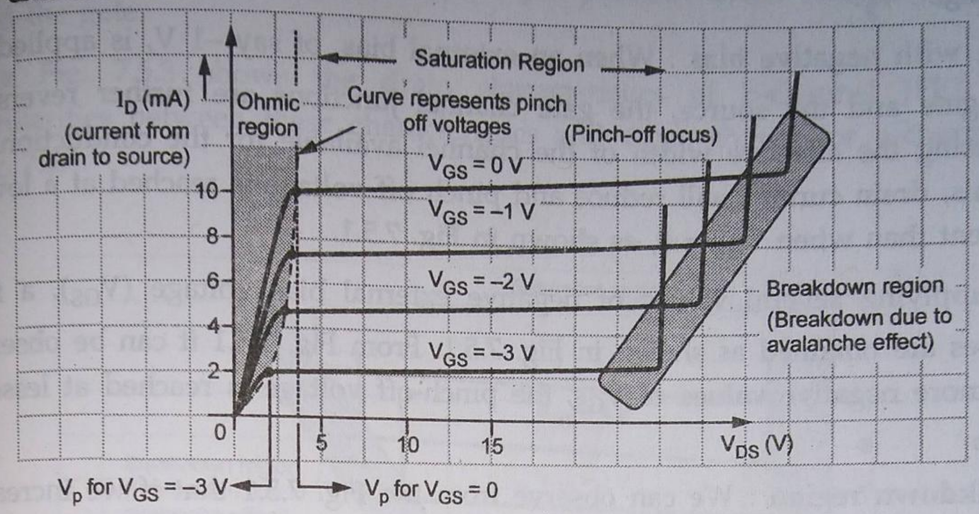

Fig. 7.5.1 Drain V-I characteristics of n-channel JFET

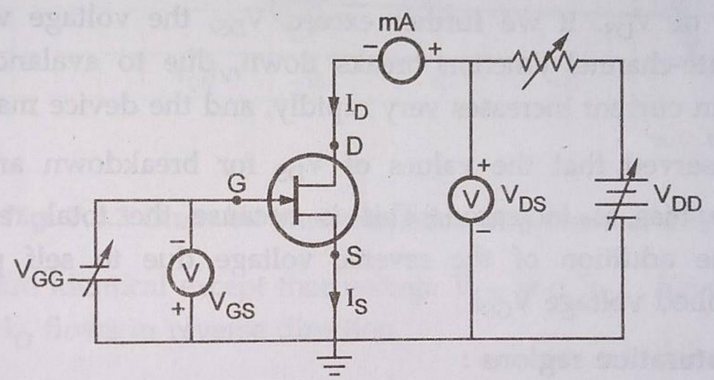

Fig. 7.5.2 Experimental setup to plot JFET characteristics

- **V_{GS} and V_{DS} both = 0** : When V_{GS} = 0 the channel is entirely open. But V_{DS} = 0, so there is no attractive force for the majority carriers (electrons in n-channel JFET) and hence drain current does not flow.
- **Self pinch-off at no bias (V_{GS} = 0)** : At V_{GS} = 0, in response to a small applied voltage V_{DS}, the n-type bar acts as a simple semiconductor resistor, and the current I_D increases linearly with V_{DS}. As V_{DS} increases, the voltage drop along the channel also increases. This increase in voltage drop increases the reverse bias on gate-source junction and causes the depletion regions to penetrate into the channel, reducing channel width. The effect of reduction in channel width provides more opposition to increase in drain current I_D. Thus, rate of increase in I_D with respect to V_{DS} is now reduced. This is shown by the curved shape in the characteristics.

- At some value of V_{DS}, drain current I_D cannot be increased further, due to reduction in channel width. Any further increase in V_{DS} does not increase the drain current I_D. I_D approaches the constant saturation value. The voltage V_{DS} at which the current I_D reaches to its constant saturation level is called **'Pinch-Off Voltage'**, V_p.
- **V_{GS} with negative bias** : When an external bias, of say –1 V, is applied between the gate and the source, the gate channel junctions are further reverse biased, reducing the effective width of the channel available for the conduction. Because of this, drain current will reduce and pinch off voltage is reached at a lower drain current than when $V_{GS} = 0$, as shown in Fig. 7.5.1.
- By applying several values of negative external bias voltage (V_{GS}), a family of curves are obtained as shown in Fig. 7.5.1. From Fig. 7.5.1 it can be observed that for more negative values of V_{GS}, the pinch-off voltage is reached at lesser values of I_D.
- **Breakdown region** : We can observe from the Fig. 7.5.1 that if we increase value of V_{DS} beyond pinch-off voltage, V_p, the drain current I_D remains constant, up to certain value of V_{DS}. If we further exceed V_{DS}, the voltage will be reached at which the gate-channel junction breaks down, due to avalanche effect. At this point the drain current increases very rapidly, and the device may be destroyed.
- It can be observed that the values of V_{DS} for breakdown are reduced as the negative gate bias is increased. This is because the total **reverse breakdown voltage** is the addition of the reverse voltage due to self pinch-off and the externally applied voltage V_{GS}.
- **Ohmic and saturation regions** :
  - It is seen that the drain characteristics of JFET is divided into two regions : Ohmic region and saturation region. In the ohmic region, the drain current I_D varies with V_{DS} and the JFET is said to behave as **voltage variable resistance.**
  - In the saturation region, the drain current I_D remains fairly constant and does not vary with V_{DS}.
- **Cut-off** : As we know, for an n-channel JFET, the more negative V_{GS} causes drain current to reduce and pinch-off voltage to reach at a lower drain current. When V_{GS} is made sufficiently negative, I_D is reduced to 0, as shown in the Fig. 7.5.1. This is caused by the widening of the depletion region to a point where it completely closes the channel. The value of V_{GS} at the cut-off point is designated as $V_{GS(OFF)}$.
- **Relation of $V_{GS(off)}$ and V_p** : I_D is 0 when $V_{GS} = -V_p$.

Drain characteristics for p-channel FET

- In a p-channel JFET the source is positive with respect to the drain. Here the source is the source of holes which flow through the channel to the drain. The pinch-off is achieved by making the source to gate voltage, V_{SG} negative (i.e. V_{GS} positive) there by reverse biasing the p-n junction diode formed by the channel and the gate.
- The Fig. 7.5.3 shows the drain characteristics of p-channel JFET. Note the similarities between these characteristics and those shown for n-channel JFET in Fig. 7.5.1.

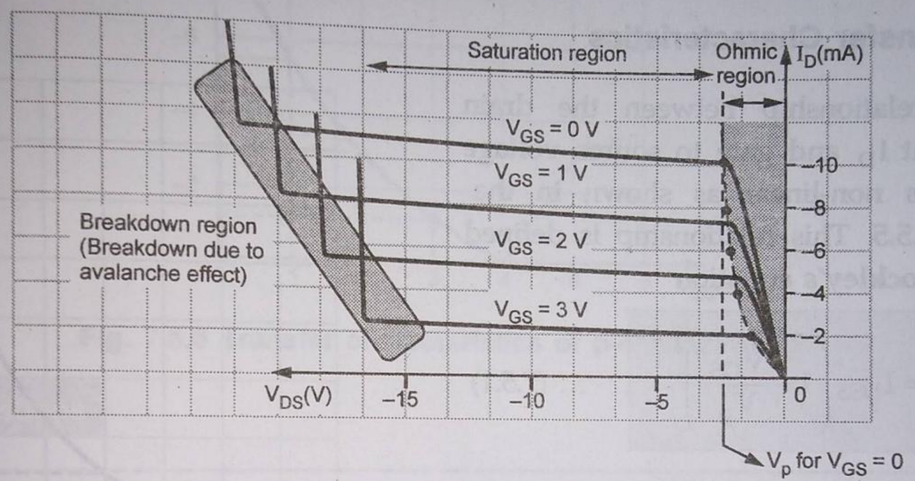

Fig. 7.5.3 Drain V-I characteristics of p-channel JFET

- The curves are identical except that voltage V_{GS} and V_{DS} have reversed polarities and current I_D flows in reverse direction.

7.5.2 JFET as a VVR or VDR

- Let us consider the drain characteristics of FET as shown in the Fig.7.5.4 In this characteristics we can see that in the region before pinch off voltage, drain characteristics is linear, i.e. FET operation is linear. In this region the FET is useful as a voltage-controlled resistor, i.e., the drain to source resistance is controlled by the bias voltage V_{GS}. The operation of FET in this region is useful in most linear applications of FET. In such an application the FET is also referred to as a **voltage-variable resistor (VVR)** or **voltage-dependent resistor (VDR)**.

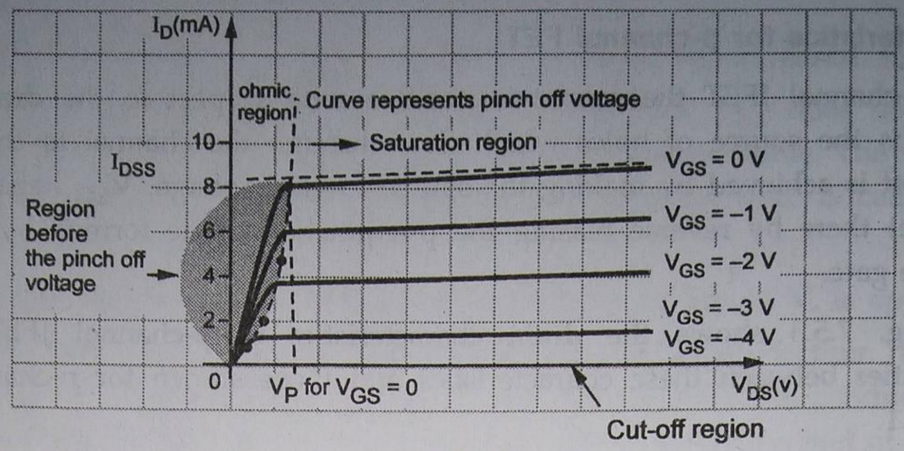

Fig. 7.5.4

7.5.3 Transfer Characteristics

- The relationship between the drain current I_D and gate to source voltage V_{GS} is non-linear as shown in the Fig. 7.5.5. This relationship is defined by **Shockley's** equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \ldots (7.5.1)$$

- The squared term of the equation will result in a non-linear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}. From equation we can also write,

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

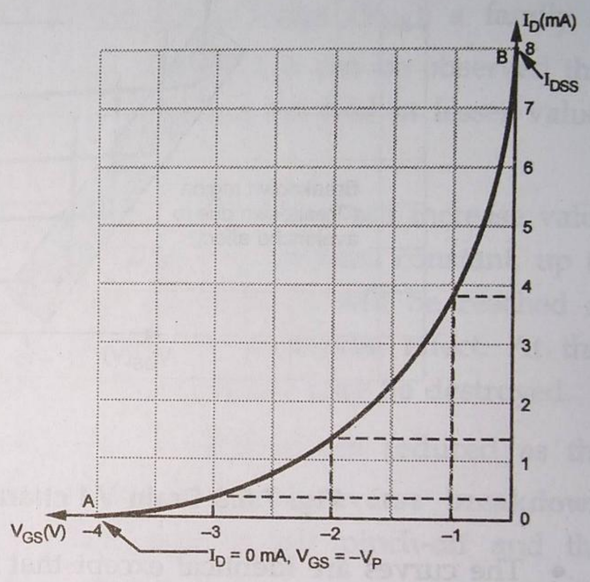

Fig. 7.5.5 Transfer characteristics of n-channel JFET

- In the equation values of I_{DSS} and V_p are constants, value of V_{GS} controls I_D.
- A point A at the bottom end of the curve on the V_{GS}-axis represents $V_{GS\,(off)}$, and point B at the top end of the curve on the I_D axis represents I_{DSS} (maximum drain current at $V_{GS} = 0$). Thus, this curve shows the operating limits of a JFET. These are :
  - $I_D = 0$ when $V_{GS} = V_{GS\,(off)}$
  - $I_D = I_{DSS}$ when $V_{GS} = 0$

Transfer characteristics for p-channel JFET

- The Fig. 7.5.6 shows the transfer characteristics of p-channel JFET. It is identical to transfer characteristics of n-channel JFET except that the polarities of V_{GS} and I_D are reversed.

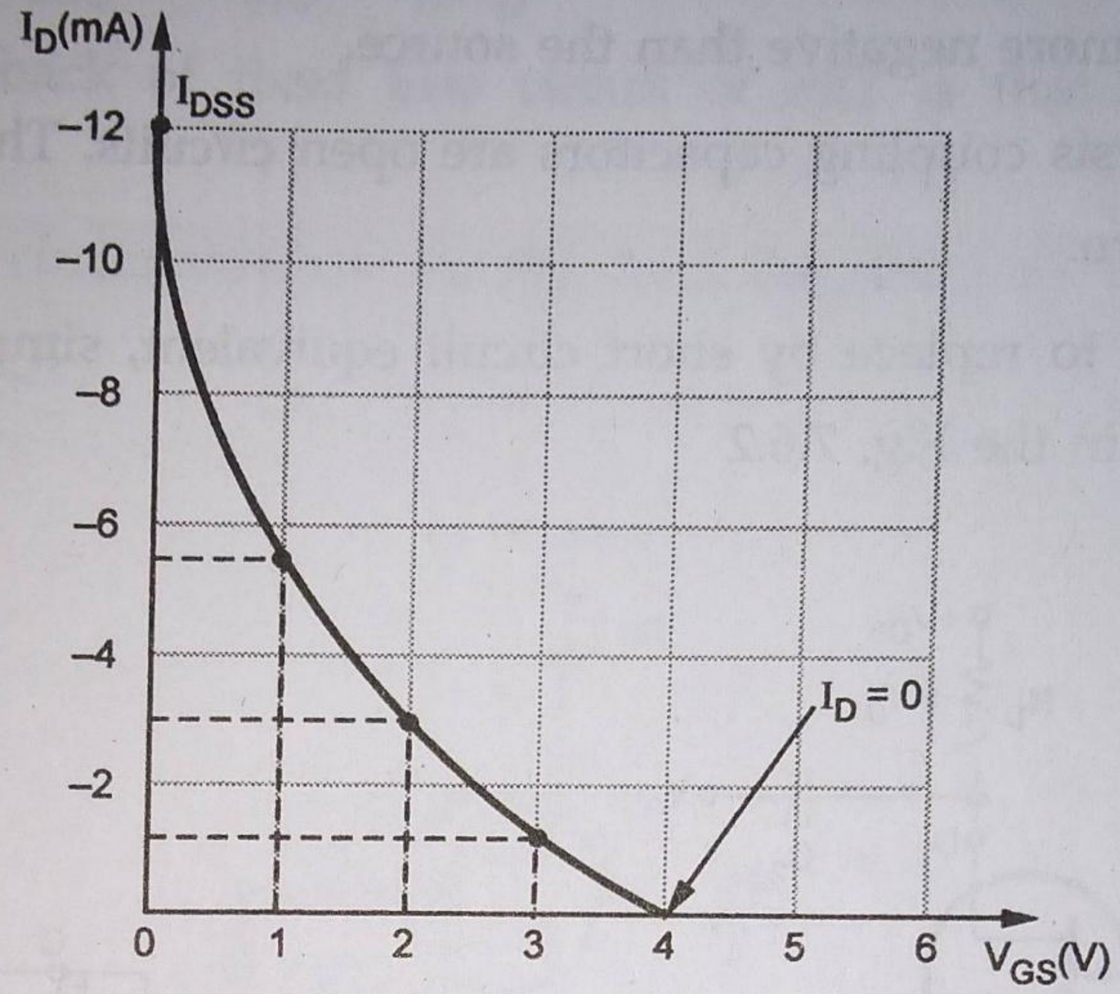

Fig. 7.5.6 Transfer characteristics of p-channel JFET