SYSTEM CALLS AND CACHING

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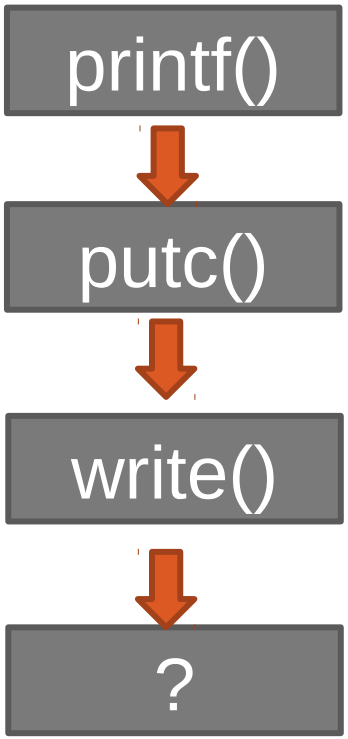
SYSTEM CALLS



SYSTEM CALLS

SYS_CALL:

- **I/O: open, close, read, write, etc.**
- **Files: delete, dup, dup2, etc.**
- **Process: fork, exec*, etc.**
- **Network: socket, etc.**
- **…**

SYSTEM CALLS

Q. Why we need system calls?

SYSTEM CALLS

- **What should we do a system call?**
- **The same as function call.**
  - We need pass arguments.
  - And run the system function.

Is this right?

SYSTEM CALLS

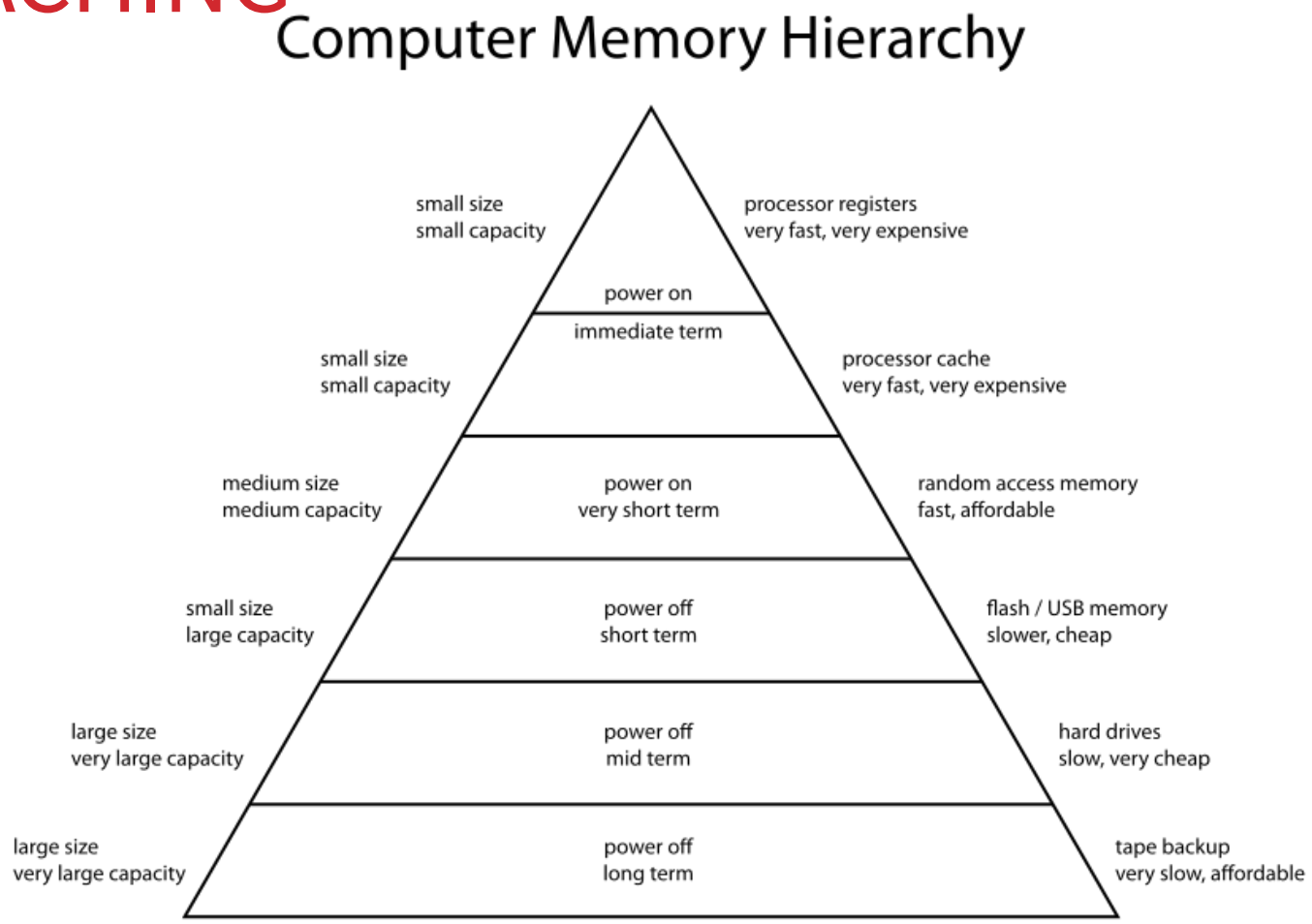
- **Do you remember the import concept pr otection?**
  - Every system call should be run in kernel mode
  - Thus, when we run a system call, we must switc h to kernel mode

SYSTEM CALLS

- **What should we do a system call?**
- **The same as function call.**
  - We need pass arguments.
  - And run the system function.

Switch to kernel mode

CACHING

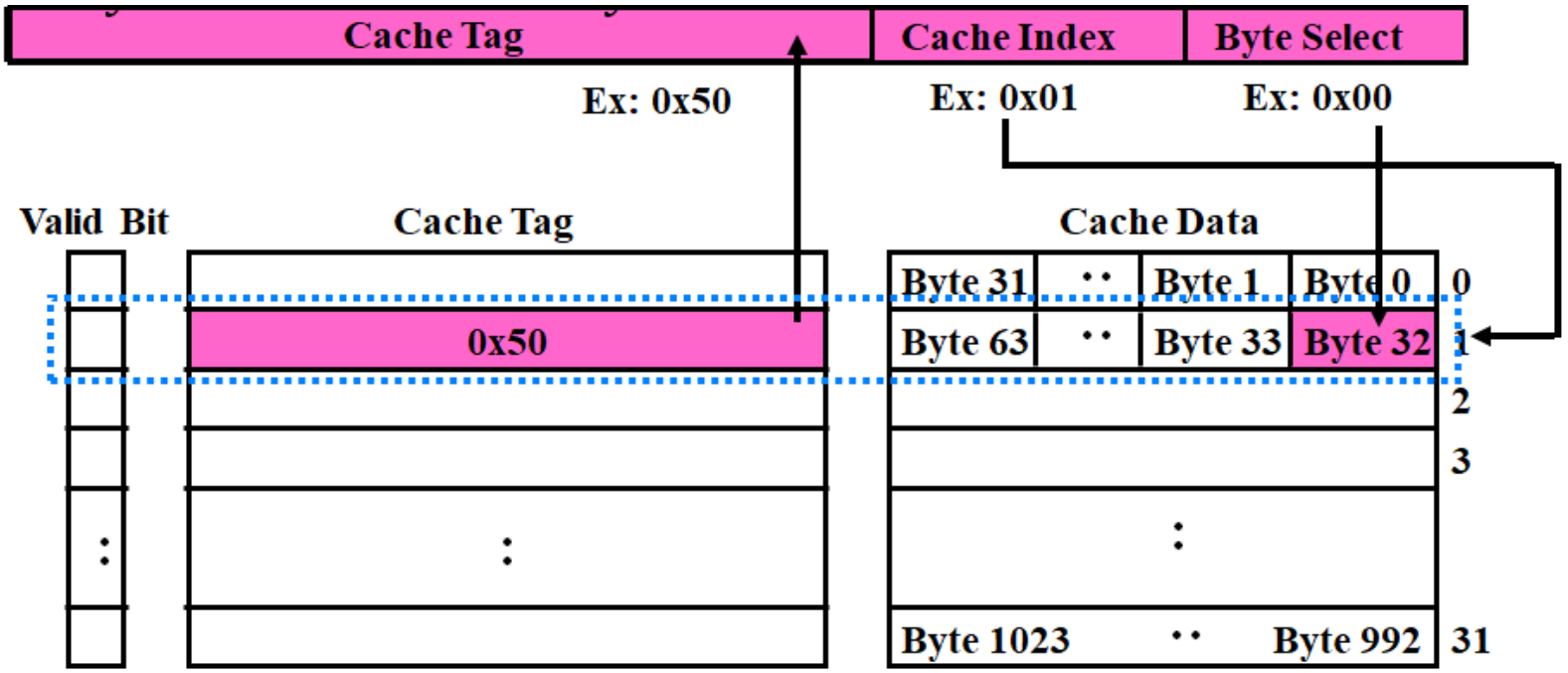


Pictures from wiki

CACHING

- **Direct-mapped cache with Y bits**
  - Each cache line contain 2^a bytes, we use the least significant a bits to discard them
  - Using M bits to identify each cache line
  - Tag field is the most N bits

DIRECT MAPPED CACHE



DIRECT MAPPED CACHE

- **All address with the same least significant a + M bits will mapped to same place**
- **Eg. 40004 03X, 50328 03X**
- **May cause a lot of fix problem**

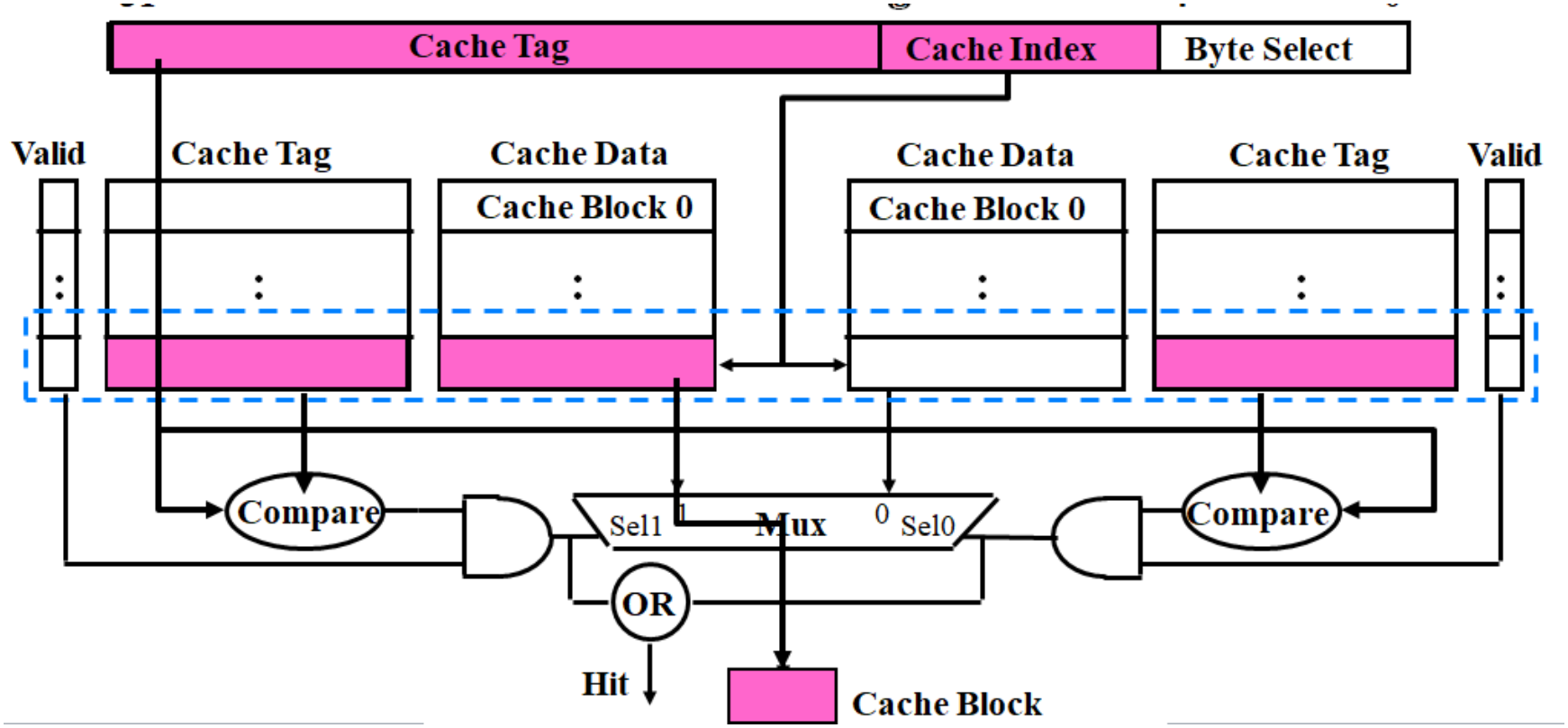
SET ASSOCIATIVE CACHE

How to avoid a lot of fix problem?

We store many of them!

- **We have N-direct mapped caches**
  - Each time we compare cache tag in N sets
- **We can find faster but more expensive**

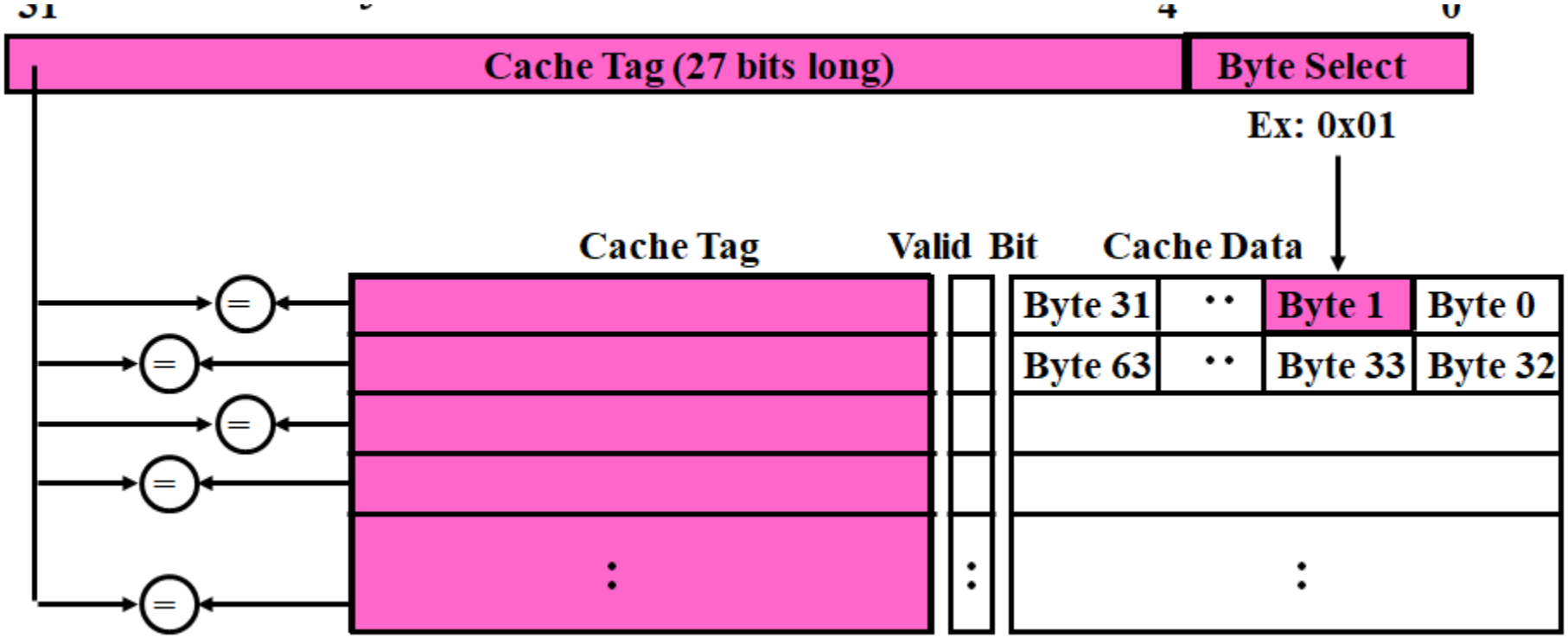
SET ASSOCIATIVE CACHE



FULLY ASSOCIATIVE CACHE

- **We don’t use cache index. We can use c ache tag to distinguish them.**
- **We need to compare all cache tags.**

FULLY ASSOCIATIVE CACHE



WRITE PROBLEM

We know that I/O is really slow…

- **We use cache to solve "I" problem.**
- **How about "O"?**

TLB

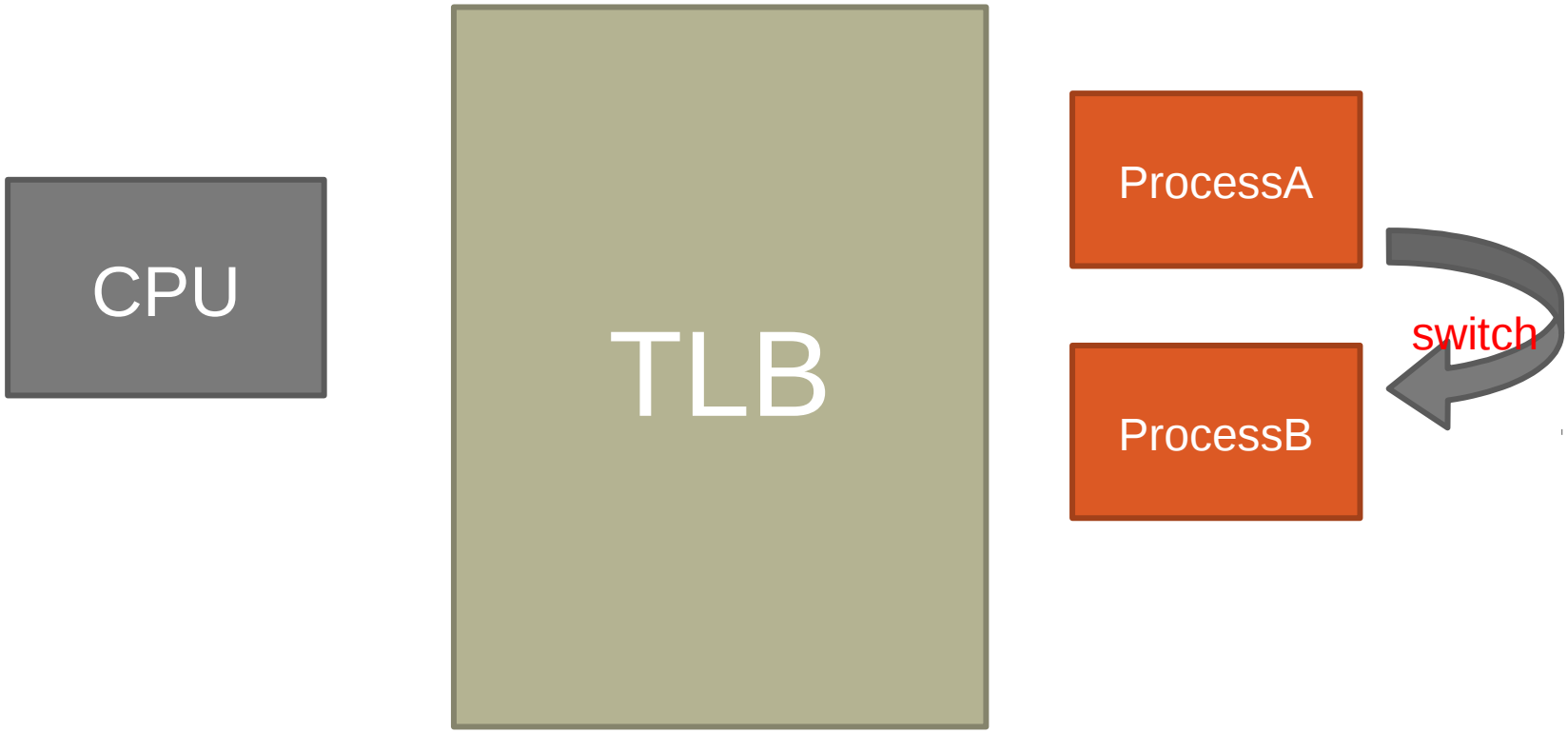
Translation Lookaside Buffer : **The same idea as cache but more complicated…**

Why?

TLB

Remember VIRTUAL?

The virtual address is the same, but the physical address is changed!



TLB

Q. How to make TLB more efficient?

LAB REQUIREMENT

1. **Write a direct cache simulator.**

   Requirement: Cache size is 1KB, cache line size is 16 b ytes, cache memory size is 256MB

2. **You can try to simulate other cache strategy, wh ich will give you bonus points.**

3. **Package should be named as: OS_lab6_Name_ xxxxxxxx where xxxxxxxx is your student id, Na me is your name. This package should contain: your report, your code.**

4. **Check blackboard for ddl.**

THANKS