BHARATIYA VIDYA BHAVAN'S
SARDAR PATEL INSTITUTE OF TECHNOLOGY
MUNSHI NAGAR, ANDHERI (W), MUMBAI 400058

Electronics Engineering Department

Subject: EL43: Computer Organization and Architecture

Class: S.E ETRX
Staff Name: Manish M. Parmar
July 2019
Marks: - 100

Sem IV
ESE Reexam

Q.1 (a)

Answer:- (1) Diagram of ARM core.....[4 marks]
(2) Features and block justification.....[6 marks]

Q.1 (b)

Answer:- (1) Minimum five points of difference.....[10 marks]

Q.2 (a)

Answer:- (1) Draw the flow chart.....[2 marks]
(2)... Example.....[8 marks]

OR

Answer:- (1) Draw the flow chart.....[2 marks]
(2)... Example.....[8 marks]

Q.2 (b)

Answer:- (1) Instruction interpretation.....[5 marks]
(2) Instruction sequencing.....[5marks]

Q.3 (a)

Answer:- (1) Define and give the concept of control unit functions
(2) State two techniques of design of the control unit.
(3) State various techniques of Microprogrammed control unit design.....[3 marks]
(4) Design one of the technique with diagram.....[7 marks]

OR

Answer:- (1) Define and give the concept of control unit functions
(2) State two techniques of design of the control unit.
(3) State various techniques of Hardwired control unit design.....[3 marks]
(4) Design one of the technique with diagram.....[7 marks]

Q.3 (b)

Answer:- (1) RISC and CISC definition.....[2 marks]
(2) Give 6 to 8 points of difference with examples.....[8 marks]

Q.4 (a)

Answer:- (1) LRU replacement policy.....[5 marks]
(2) FIFO replacement policy.....[5 marks]

OR

Answer:- (1) Segmentation concept.....[5 marks]
(2) Paging concept.....[5 marks]

Q.4 (b)

Answer:- (1) Necessity of cache memory.....[3 marks]
(2) Definition of various terms.....[3 marks]
(3) Factors affecting Hit rate.....[4 marks]

Q.5 (a)

Answer:- (1) Define Hazard.....Instruction Hazard..... [4 marks]
(2) Data Hazard.....[3 marks]
(3) Structural Hazard..... [3 marks]

Q.5 (b)

Answer:- (1) Interrupt driven I/O.....[5 marks]
(2) DMA I/O..... ..[5 marks]