

Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India (Autonomous College Affiliated to University of Mumbai)

End Semester Examination (Reexam)

January 2020

Max.Marks: 60

Class: S.E.

Course Code: EL43

Name of the Course: Computer Organization and Architecture

Duration: 60 Min

Semester: IV

Branch: Electronics

SYNOPTIC

Q 1.)		Mark	CO'
a)	Cache memory concepts: cache hit and cache miss. 2 Marks (1 Mark for each)	S	S
a)	Calculation 1 Mark (No mark for formula) $t_A = Ht_1 + (1-H)t_2 = 0.9*200 \text{nS} + 0.1*800 \text{nS}$	3	CO4
b).	Any three differentiations points between polling I/O and interrupt I/O		
c)	Computer organization definition 1 Mark		COS
	Computer architecture definition 1 Mark		COI
	Computer classification parameters 1 Mark		171
d)	Definition 1 Mark		
	Calculation 2 Marks		
	N=6		
	P=0.1		
	$I_1 = D D_1^{-1}$	3	CO
	$\left(\frac{1-P}{1}+\frac{P}{N}\right)^{-1}$		
	Speedup = $(0.9+0.1/6)^{-1}$	To the same	
Q 2)			
a)	Draw a neat diagram for interfacing 8 bit processor with 16 bit address line to memory of size		
	16K x 8 bits using two chips of 8 KB.		
	Neat Diagram 3 Marks		
b)	Explanation of Micro programming 2 Marks		COS
	Example of Micro Programming 2 Marks		
c)	Part A		
	Diagram 2 Marks		
	Calculation of number of bits 1 Mark		
	Look up method with diagram 2		
		5	CO
	Or		
	Part B		
	Explain need of Cache replacement 1 Mark		
	List of Replacement methods 1 Marks		
	Example 3 Marks		
	L'Adilipie 3 Ivial KS		

41	1 1111 /3		U	1004
	Algorithm	1 Mark		
	Initialization	1 Mark		
	(0.5 mark for each correct	step) X 6 = 3 Marks		
	Correct Answer	1 Mark		
		or		
	Part B			
	Algorithm	1 Mark		
	Initialization	1 Mark		
	(0.5 mark for each correct step) X 6 = 3 Marks			
	Correct Answer	1 Mark		
b)	Diagram 2 Marks		(COL
	Explanation 4 Marks		- 6	COI
Q 4)				
a)	One mark for one point X 6 6 Marks			
	CISC	RISC		9816
	The original microprocessor ISA	Redesigned ISA that emerged in		
		the early 1980s		
	Instructions can take several clock cycles	Single-cycle instructions		
	Hardware-centric design	Software-centric design		
	- the ISA does as much as	- High-level compilers take on		
	possible using hardware	most of the burden of coding		
	circuitry	many software steps from the		000
	Many officiant was of DANAAL	programmer	6	CO3
	More efficient use of RAM than RISC	Heavy use of RAM (can cause bottlenecks if RAM is limited)		
	Complex and variable length	Simple, standardized	Parine:	
	May support microcode (micro-	Only one layer of instructions		
	programming where	Only one layer of histractions		
	instructions are treated like			
	Large number of instructions	Small number of fixed-length		
	Large number of instructions	Instructions		
	Compound addressing modes	Limited addressing modes		
b)	Explain BUS arbitration in detail.			
	What is bus arbitration 1 Mark			
	Need of bus arbitration 1 Mark			CO5
	Methods of bus arbitration 4 Mark (Any two methods)			
Q 5)				
a)	Express (27.4274) in IEE	E 754 floating point number representation.		1
a)	2 mark for representation		2	CO2
b)	Example with diagram 4	Marks (2 Marks each)	4	CO3
·c)	Write a short note of Flynr		1	1003
c)	Bases for classification 1 Mark			
	List Classification 1 Mark			
	Each type with example 4 Marks			
	or			CO6
	Explain Hazards in pipe-lining.			1
	Explain riazards in pipe-ining. Explain with example what is pipe lining 2 Marks			
	Hazard with diagram and details 4 Marks			
	Truzura with diagram and C	T IVIAI NO		

41

1 till L.