Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination

May – 2019

Max. Marks: 60 **Duration: 3 Hours**

Class:SE **Semester: IV**

Course Code:EL43 **Branch:ETRX**

Name of the Course: Computer Organization and Architecture

Instruction:

(1) All questions are compulsory

(2) Draw neat diagrams

(3) Assume suitable data if necessary

Q No.		Max. Marks	CO
Q.1 (A)	Define the terms: Cache Hit and Cache Miss. Calculate the effective memory access time if M1: 100nS access time(Including Hit detection) M2: 800nS access time(Including Miss penalty) Time to transfer block from M2 to M1 is 600 ns and Hit ratio of 0.85.	03	CO4
Q.1 (B)	What is the necessity of DMA? Support your answer with the help of suitable diagram.	03	CO5
Q.1 (C)	Define computer organization and architecture and list parameters for classification of computers.	03	CO1
Q.1 (D)	State Amdahl's law and calculate speed up factor if number of processors used is 5 and 10 percentage of instructions are executed in parallel.	03	CO1
Q.2 (A)	Draw a neat diagram for interfacing 8 bit processor with 16 bit address line to memory of size 32K x 8 bits using two chips of 16 KB.	03	CO4
Q.2 (B)	Explain concept of Nano programming with help of suitable example.	04	CO3
Q.2 (C)	A 32 bit processor has 32 bit memory address lines. It has 16KB of Cache memory. The computer follows 8-way set associative mapping with each Cache line being of size 64 bits. Show memory address format and explain the process of look up with neat diagrams.	05	CO4
	OR		
Q.2 (C)	What are the different schemes to replace memory block in Cache memory. Explain in detail with help of suitable example.	05	CO4
Q.3 (A)	Solve (12)H x (-6)H using Booths algorithm. (H-Hexadecimal)	06	CO2
	OR		
Q.3 (A)	Using restoring division algorithm solve $(1212)_3/(121)_3$.	06	CO2
Q.3 (B)	With help of neat diagram explain architecture of ARM processor.	06	CO1
Q.4 (A)	Compare and contrast RISC and CISC architectures.	06	CO3
Q.4 (B)	Explain BUS arbitration in detail.	06	CO5

Q.5 (A)	Express (25.4224) in IEEE 754 floating point number representation.	02	CO2
Q.5 (B)	Explain any two addressing modes of IA-32 with examples.	04	CO3
Q.5 (C)	Write a short note of Flynn's classification..	06	CO6
	OR		
Q.5 (C)	Explain Hazards in pipelining.	06	CO6