Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

Re Examination Synoptic

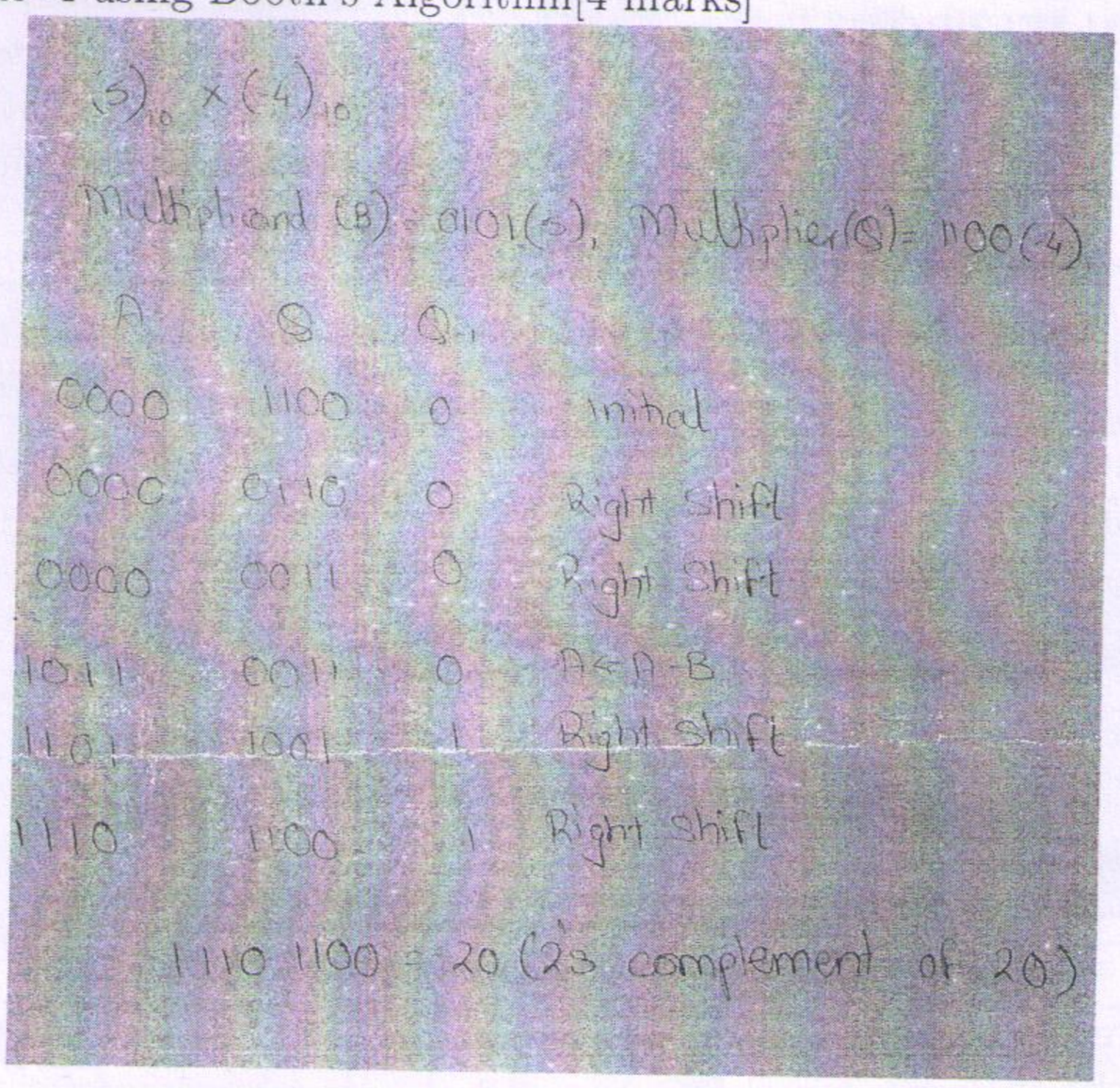
January 2020

Max. Marks: 60 **Duration: 3 Hrs.**

Class: SE **Semester:IV**

Course Code: CE44/IT42 **Branch: Computer/IT**

Name of the Course: Computer Organization and Architecture

Q. No.		Max. Marks
Q.1 A	Write a short note on "The Von Neumann Machine". Diagram- 2 marks Explanation - 4 marks	6
Q.1 B	What are the Requirements of Embedded Systems? Explain Possible Organization of an Embedded System Requirements of Embedded Systems[2 marks] Possible Organization of an Embedded System[4 Marks]	6
Q.2 A	Draw the flowchart and Multiply 5 x -4 using Booth's Algorithm Flowchart of Booth's Algorithm[2 marks] Multiply 5 x -4 using Booth's Algorithm[4 marks]  **OR** Draw the flowchart of Restoring and Non Restoring Division Algorithm Flowchart of Restoring [3 marks] Flowchart of Non Restoring Division Algorithm [3 Marks]	6

<table>
<tr><td>Q.2 B</td><td>How IEEE 754 Floating point represents number in Single and Double Precision? Give one example of each.
Single Precision Format[1 Marks]
Example[2 marks]
Double Precision Format[1 Marks]
Example[2 marks]</td><td>6</td></tr>
<tr><td>Q.3 A</td><td>How data flow occurs in Indirect cycle and Interrupt Cycle?
Data flow occurs in Indirect cycle diagram[1 marks]
Explanation [2 marks]
Data flow occurs in Indirect cycle diagram[1 marks]
Explanation [2 marks]</td><td>6</td></tr>
<tr><td>Q.3 B</td><td>What are the features of RISC and CISC Processor. Why is the need of RISC processor?
Features of RISC Processor [2 Marks]
Features of CISC Processor [2 Marks]
Need of RISC processor[2 Marks]

OR

What are the functions of Control Unit? What are the control signals associated with control Unit?
Functions of Control Unit[3 Marks]
Control signals associated with control Unit[3 Marks]</td><td>6</td></tr>
<tr><td>Q.4 A</td><td>Distinguish between the semiconductor types of memory (RAM, PROM, EPROM, EEPROM) with respect to any four relevant points [For e.g., Category(read only/write only), erasure, Write mechanism, Volatility,etc.]
for each distinguishing points [2 marks] so total [8 marks]

Semiconductor Memory Types
<table><tr><th>Memory Type</th><th>Category</th><th>Erasure</th><th>Write Mechanism</th><th>Volatility</th></tr><tr><td>Random-access memory (RAM)</td><td>Read-write memory</td><td>Electrically, byte-level</td><td>Electrically</td><td>Volatile</td></tr><tr><td>Read-only memory (ROM)</td><td rowspan="2">Read-only memory</td><td rowspan="2">Not possible</td><td>Masks</td><td rowspan="4">Nonvolatile</td></tr><tr><td>Programmable ROM (PROM)</td><td rowspan="3">Electrically</td></tr><tr><td>Erasable PROM (EPROM)</td><td rowspan="3">Read-mostly memory</td><td>UV light, chip-level</td></tr><tr><td>Electrically Erasable PROM (EEPROM)</td><td>Electrically, byte-level</td></tr><tr><td>Flash memory</td><td>Electrically, block-level</td></tr></table></td><td>8</td></tr>
<tr><td>Q.4 B</td><td>What are the drawbacks of Programmed and Interrupt-Driven I/O?
Drawbacks of Programmed I/O[2 marks]
Drawbacks of Interrupt-Driven I/O[2 marks]</td><td>4</td></tr>
</table>

Q.5 A

Consider a main memory with five page frames and the following sequence of page references: 3, 8, 2, 3, 9, 1, 6, 3, 8, 9, 3, 6, 2, 1, 3.
Which one of the following is true with respect to page replacement policies First-In-First-out (FIFO) and Least Recently Used (LRU)?

a. Both incur the same number of page faults
b. FIFO incurs 2 more page faults than LRU
c. LRU incurs 2 more page faults than FIFO
d. FIFO incurs 1 more page faults than LRU

3 marks for each of the algorithms

Number of frames = 5

FIFO

According to FIFO, the page which first comes in the memory will first goes out.

Request	3	8	2	3	9	1	6	3	8	9	3	6	2	1	3
Frame 5						1	1	1	1	1	1	1	1	1	1
Frame 4					9	9	9	9	9	9	9	9	2	2	2
Frame 3			2	2	2	2	2	2	8	8	8	8	8	8	8
Frame 2		8	8	8	8	8	8	3	3	3	3	3	3	3	3
Frame 1	3	3	3	3	3	3	6	6	6	6	6	6	6	6	6
Miss/Hit	Miss	Miss	Miss	Hit	Miss	Miss	Miss	Miss	Miss	Hit	Hit	Hit	Miss	Hit	Hit

Number of Page Faults = 9

Number of hits = 6

LRU

According to LRU, the page which has not been requested for a long time will get replaced with the new one.

Request	3	8	2	3	9	1	6	3	8	9	3	6	2	1	3
Frame 5						1	1	1	1	1	1	1	2	2	2
Frame 4					9	9	9	9	9	9	9	9	9	9	9
Frame 3			2	2	2	2	2	2	8	8	8	8	8	1	1
Frame 2		8	8	8	8	8	6	6	6	6	6	6	6	6	6
Frame 1	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
Miss/Hit	Miss	Miss	Miss	Hit	Miss	Miss	Hit	Hit	Miss	Hit	Miss	Hit	Miss	Miss	Hit

Number of Page Faults = 9

Number of Hits = 6

The Number of page faults in both the cases is equal therefore the Answer is option (a).

	Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size. a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag. b. Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag. a. Address format: Tag = 20 bits; Line = 6 bits; Word = 6 bits. Number of addressable units = 2^{32} bytes; number of blocks in main memory = 2^{26}; Number of lines in cache = 2^6 = 64; size of tag = 20 bits. b. Address format: Tag = 26 bits; Word = 6 bits. Number of addressable units = 2^{32} bytes; number of blocks in main memory = 2^{26}; Number of lines in cache = undetermined; size of tag = 26 bits. 3 marks for each part	6
Q.5 B	What are the different pipeline hazards? Explain each of them. Resource hazards - 2 marks Data hazards - 2 marks Control hazards - 2 marks	6