Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India
(Autonomous College Affiliated to University of Mumbai)

End Semester Examination

August 2021(Summer Term)

Max. Marks: 60 Duration:130 min.
Class: S.Y. Semester: III
Course Code: CS203/IT203 Branch: COMP,IT
Name of the Course: Computer Architecture and Organization

Instruction:
(1) All questions are compulsory
(2) Draw neat diagrams
(3) Assume suitable data if necessary

Q. No.		Max. Marks	CO-BL-PI
1 a)	A hard disk with a transfer rate of 10 M bytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz. and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?	8	6-3-2.2.4
b)	Why I/O devices cannot be connected directly to the system bus? What are the important functions of I/O system? Explain the Programmed I/O. OR What is the need of standardization of buses? What are the salient features of PCI and SCSI bus?	7	6-2-2.2.2
2 a)	Draw the flowchart for restoring division algorithm. Solve (17) ÷(3) using restoring division algorithm. OR What is the bit pair recoded multiplier for -27(minus 27) ? Solve 10 multiplied by -7 (10 * -7) using bit pair recoding or modified Booth's algorithm.	9	2-3-2.1.3
b)	What are the advantages and disadvantages of microprogrammed control unit? Explain the Wilkes's microprogrammed control unit. OR What are the RISC and CISC processors? What are the	6	3-3-2.2.2

	advantages and disadvantages of RISC and CISC processors?		
3a)	Give the steps for micro-operation for following instructions i) ADD R_0, 20H ii) MOV R_0, 20H	8	3-3-2.2.3
b)	What is virtual memory? Why is it necessary to implement virtual memory? Explain the virtual to physical address translation process using paging with example.	7	4-2-2.2.3
4 a)	Consider a direct mapped cache of size 16 KB with block size 128 bytes. The size of main memory is 256 KB. Find the number of bits in the tag, line and word/line offset in main memory address.	7	4-3-2.2.3
b)	Consider a pipeline having 4 phases with duration 60, 70, 90 and 80 ns. Given latch delay is 10 ns. Calculate- i) Pipeline cycle time ii) Non-pipeline execution time iii) Speed up ratio iv) Pipeline time for 1000 tasks	8	5-3-2.2.3