Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination (Reexam)

January – 2020

Max. Marks: 60 Duration: 3 Hours

Class:SE Semester: IV

Course Code:EL43 Branch:ETRX

Name of the Course: Computer Organization and Architecture

Instruction:

(1) All questions are compulsory

(2) Draw neat diagrams

(3) Assume suitable data if necessary

Q No.		Max. Marks	CO
Q.1 (A)	Discuss cache memory conepts in terms of cache hit and cache miss. Calculate the effective memory access time if M1: 200nS access time(Including Hit detection) M2: 800nS access time(Including Miss penalty) Time to transfer block from M2 to M1 is 500 ns and Hit ratio of 0.9.	03	CO4
Q.1 (B)	Compare and contrast polling I/O and interrupt driven I/O data transfer methods.	03	CO5
Q.1 (C)	What is the difference between the terms Computer Organization and Computer Architecture? Justify with any three parameters.	03	CO1
Q.1 (D)	Calculate speed up factor if number of processors used is 6 and 10 percentage of instructions are executed in parallel.	03	CO1
Q.2 (A)	Draw a neat diagram for interfacing 8 bit processor with 16 bit address line to memory of size 16K x 8 bits using two chips of 8 KB.	03	CO4
Q.2 (B)	Explain concept of Micro programming with help of suitable example.	04	CO3
Q.2 (C)	A 32 bit processor has 32 bit memory address lines. It has 32KB of Cache memory. The computer follows 8-way set associative mapping with each Cache line being of size 64 bits. Show memory address format and explain the process of look up with neat diagrams. OR	05	CO4
Q.2 (C)	Cache memory requires the replacement of memory blocks. Give reasons. Also list various replacement methods.	05	CO4
Q.3 (A)	Solve (11)H x (-5)H using Booths algorithm. (H-Hexadecimal) OR	06	CO2
Q.3 (A)	Using restoring division algorithm solve $(2112)_3/(211)_3$	06	CO2
Q.3 (B)	Each ARM processor follows the basic ARM core architecture. Discuss the ARM core data flow diagram justifying the necessity of each block.	06	CO1

Q.4 (A)	Compare and contrast Von Neumann and Harwards architectures.	06	CO3
Q.4 (B)	In multiprocessors systems, the problem of bus contention generally occurs. What are the methods to resolve this bus contention? Discuss in detail.	06	CO5
Q.5 (A)	Express (27.4274) in IEEE 754 floating point number representation.	02	CO2
Q.5 (B)	For 80386 and pentium architecture, discuss with examples, Direct addressing and Based Indexed addressing modes.	04	CO3
Q.5 (C)	Computer architectures in parallel domain has been classified according to Flynn. Discuss all the categories.	06	CO6
	OR		
Q.5 (C)	Define the terms: Data Hazard, Instruction Hazard and Structural Hazards in ARM processor (Pipelined version).	06	CO6