

Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India (Autonomous College Affiliated to University of Mumbai)

End Semester Examination (Make-up) July - 2019

Max. Marks: 60

Class:SE

Course Code:EL43

Duration: 3 Hours Semester: IV

Branch:ETRX

Name of the Course: Computer Organization and Architecture

Instruction:

(1) All questions are compulsory

(2) Draw neat diagrams

(3) Assume suitable data if necessary

Q No.		7.5	0.0
		Max.	CO
Q.1 (A)	Calculate number of external connections required for memory of	Marks 04	
	size 1024 x 8 Bytes. Also draw memory interface diagram.	04	CO4
Q.1 (B)	With help of block diagram explain DMA controller.	04	CO5
		-	000
	OR		
Q.1 (B)	What are the different blocks of I/O module and what are their functions?	04	CO5
Q.1 (C)	List and explain driving factors behind design for performance	04	COI
Q.2(A)	What is Micro programmed Control Unit . Draw suitable diagram	06	CO3
00/51	to support your answer.	00	003
Q.2 (B)	A 8 bit processor has 16 bit address lines. It has 4 KB of cache	06	CO4
	memory. The computer follows direct mapping with each cache line		001
	being of size 32 bit show memory address format and explain the		
02(1)	process of look up with neat diagrams.		
Q.3 (A)	Perform (2)*(31) using Booth's multiplication algorithm.	06	CO2
	OR		
00/11			
Q.3 (A)	Using Non Restoring division algorithm solve (31)/(4).	06	CO2
Q.3 (B)	Write short note on Instruction formats and basic instruction cycle.	06	CO3
$\frac{Q.4(A)}{Q.4(B)}$	Write short note on register architecture of ARM processor	04	CO1
Q.4 (B)	Perform (67)base8+(71)base8 and write answer in form (X)S (S = Base 7).	02	CO ₂
Q.4 (C)	Compare different types of Bus Arbitration Techniques.	06	CO5
	OR		
Q.4 (C)	What are different types of bus? Support your answer with suitable	06	COF
	diagrams and/or examples.	00	CO ₅
Q.5 (A)	Compare and contrast Von Neuman and Harvard Architecture	06	CO1
Q.5 (B)	What are the different stages in six stage pipelining. Support your	0.0	CO6
	answer with suitable example and timing diagram.	00	000