Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination – Re examination

July – 2019

Max. Marks: 100 Duration: 3 Hours

Class:SE Semester: IV

Course Code:EL43 Branch:ETRX

Name of the Course: Computer Organization and Architecture

Instruction:

(1) All questions are compulsory

(2) Draw neat diagrams

(3) Assume suitable data if necessary

Q No.		Max. Marks	CO
Q.1 (A)	With neat block diagram, explain architectural features of an ARM.	10	CO1
Q.1 (B)	Compare and contrast Von Neumann and Harvards architecture. Also list driving factors behind design for performance.	10	CO1
Q.2 (A)	Draw the flow chart and explain non restoring algorithm with an example.	10	CO2
	OR		
Q.2 (A)	Draw the flow chart and explain Booths algorithm with an example.	10	CO2
Q.2 (B)	Explain instruction interpretation and sequencing in detail.	10	CO3
Q.3 (A)	Draw and explain microprogrammed control unit.	10	CO3
	OR		
Q.3 (A)	Draw and explain hardwired control unit.	10	CO3
Q.3 (B)	Compare and contrast RISC and CISC architectures.	10	CO3
Q.4 (A)	Discuss LRU and FIFO page replacement policies.	10	CO4
	OR		
Q.4 (A)	Compare and contrast paging and segmentation techniques to implement virtual memory.	10	CO4
Q.4 (B)	What is the necessity of cache memory? Explain the terms: Cache Hit, Cache Miss and Hit Rate. State the factors which contributes to Hit rate.	10	CO4
Q.5 (A)	Explain different types of pipeline hazards.	10	CO6
Q.5 (B)	Explain interrupt driven I/O and DMA I/O mapping techniques.	10	CO5