Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination

May 2019

Max.Marks: 60 **Duration:**60 Min

Class: S.E. **Semester:** IV

Course Code: EL43 **Branch:** Electronics

Name of the Course: Computer Organization and Architecture

SYNOPTIC

Q 1.)		Marks	CO's
a)	Definitions 2 Marks (1 Mark for each) Calculation 1 Mark (No mark for formula) $t_A=Ht_1+(1-H)t_2=0.85*100nS + 0.15*800nS = 85nS + 120nS= 200\ nS$	3	CO4
b)	Requirement of DMA 1 Mark Example 2 Marks	3	CO5
c)	Computer organization definition 1 Mark Computer architecture definition 1 Mark Computer classification parameters 1 Mark	3	CO1
d)	Definition 1 Mark Calculation 2 Marks N=5 P=0.1 $\left(\frac{1-P}{1}+\frac{P}{N}\right)^{-1}$ Speedup = $(0.9+0.1/5)^{-1}$= 1.08	3	CO1
Q 2)			
a)	Draw a neat diagram for interfacing 8 bit processor with 16 bit address line to memory of size 32K x 8 bits using two chips of 16 KB. Neat Diagram 3 Marks	3	CO4
b)	Explanation of Nano programming 2 Marks Example of Nano Programming 2 Marks	4	CO3
c)	**Part A** Diagram 2 Marks Calculation of number of bits 1 Mark Look up method with diagram 2 27 Bits TAG | 3 Bits for selecting set | 2 Bits for word as Cache line is 64 bit Or Part B Explain need of Cache replacement 1 Mark List of Replacement methods 1 Marks Example 3 Marks	5	CO4

<table>
<tr><td>Q 3
a)</td><td>Part A
Algorithm 1 Mark
Initialization 1 Mark
(0.5 mark for each correct step) X 6 = 3 Marks
Correct Answer 1 Mark
or
Part B
Algorithm 1 Mark
Initialization 1 Mark
(0.5 mark for each correct step) X 6 = 3 Marks
Correct Answer 1 Mark</td><td>6</td><td>CO2</td></tr>
<tr><td>b)</td><td>Diagram 2 Marks
Explanation 4 Marks</td><td>6</td><td>CO1</td></tr>
<tr><td>Q 4)</td><td></td><td></td><td></td></tr>
<tr><td>a)</td><td>One mark for one point X 6 6 Marks
<table>
<tr><th>CISC</th><th>RISC</th></tr>
<tr><td>The original microprocessor ISA</td><td>Redesigned ISA that emerged in the early 1980s</td></tr>
<tr><td>Instructions can take several clock cycles</td><td>Single-cycle instructions</td></tr>
<tr><td>Hardware-centric design

– the ISA does as much as possible using hardware circuitry</td><td>Software-centric design

– High-level compilers take on most of the burden of coding many software steps from the programmer</td></tr>
<tr><td>More efficient use of RAM than RISC</td><td>Heavy use of RAM (can cause bottlenecks if RAM is limited)</td></tr>
<tr><td>Complex and variable length instructions</td><td>Simple, standardized instructions</td></tr>
<tr><td>May support microcode (micro-programming where instructions are treated like small programs)</td><td>Only one layer of instructions</td></tr>
<tr><td>Large number of instructions</td><td>Small number of fixed-length instructions</td></tr>
<tr><td>Compound addressing modes</td><td>Limited addressing modes</td></tr>
</table></td><td>6</td><td>CO3</td></tr>
<tr><td>b)</td><td>Explain BUS arbitration in detail.
What is bus arbitration 1 Mark
Need of bus arbitration 1 Mark
Methods of bus arbitration 4 Mark (Any two methods)</td><td>6</td><td>CO5</td></tr>
<tr><td>Q 5)</td><td></td><td></td><td></td></tr>
<tr><td>a)</td><td>Express (25.4224) in IEEE 754 floating point number representation.
2 mark for representation</td><td>2</td><td>CO2</td></tr>
<tr><td>b)</td><td>Example with diagram 4 Marks (2 Marks each)</td><td>4</td><td>CO3</td></tr>
<tr><td>c)</td><td>Write a short note of Flynn's classification.
Bases for classification 1 Mark
List Classification 1 Mark
Each type with example 4 Marks
or
Explain Hazards in pipe-lining.
Explain with example what is pipe lining 2 Marks
Hazard with diagram and details 4 Marks</td><td>6</td><td>CO6</td></tr>
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