Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

Re Examination

July 2019

Max. Marks: 100 | **Duration: 3 Hrs**

Class: SE | **Semester: IV**

Course Code: IT42 | **Branch: IT**

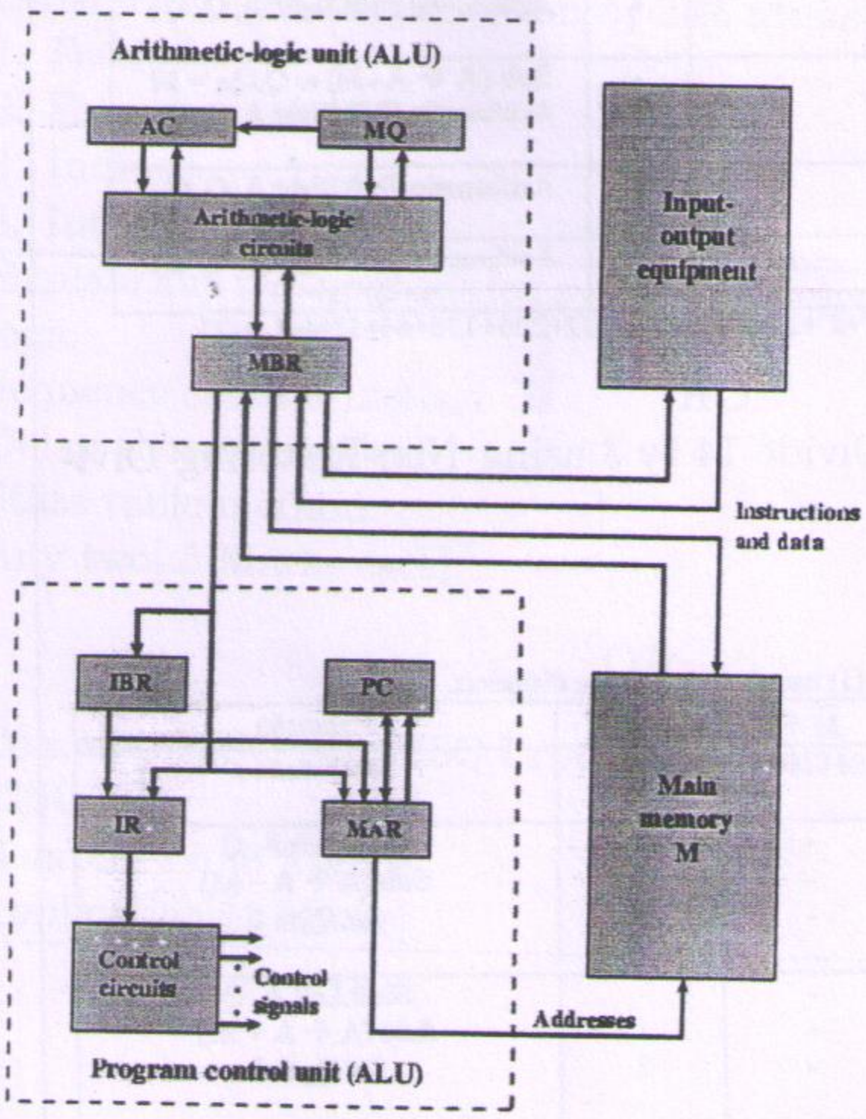
Name of the Course: Computer Organization and Architecture

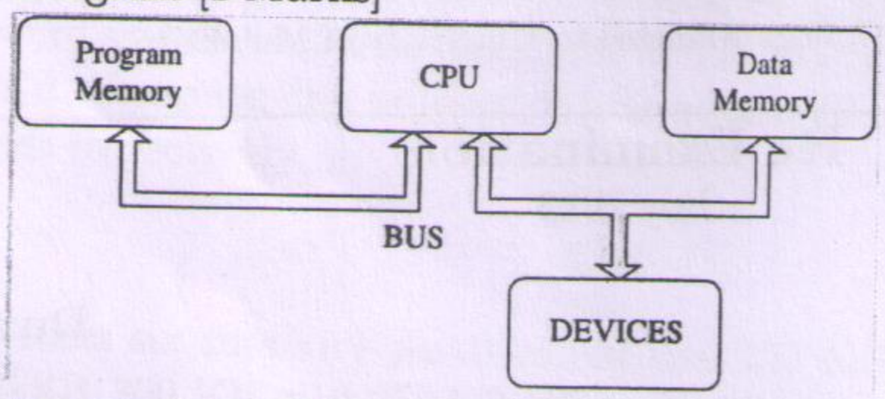
Instructions:

(1) All questions are compulsory

(2) Assume suitable data if necessary

(3) Draw neat diagram wherever required.

Q No.		Max. Marks	CO
Q.1 A	With neat diagram, describe the general structure of IAS computer. Diagram [4 Marks]  Description of ALU [2 Marks] Description of Control Unit[2 Marks] Description of I/O[1 Marks] Description of Main Memory[1 Marks]	10	CO1

Q.1 B.	Describe Harvard Architecture. Compare it with Von Neumann Architecture. Diagram [2 Marks]  Description of Harvard Architecture[4 Marks] Comparison[4 Marks]	10	CO1
Q.2 A.	Draw the flowchart and Multiply 9 x -3 using Booth's Algorithm Flowchart [4 Marks] Calculation [6 Marks]	10	CO2

Example: Multiply 9 x -3 = -27 using Booth Algorithm
+3 = 00011, -3 = 11101 (2's complement of +3)

A	Q	Q_{-1}	Add (M)	Sub ($\overline{M}$ +1)	Count	Remarks
00000	1110	0	01001	10111	5	Initialization
10111 11011	11101 1110	0 1	- -	- -	- 4	Sub (A ← A - M) as Q_0Q_{-1} = 10 Arithmetic Shift Right A, Q, Q_{-1}
00100 00010	11110 0111	1 0	- -	- -	- 3	Add (A ← A + M) as Q_0Q_{-1} = 01 Arithmetic Shift Right A, Q, Q_{-1}
11001 11100	01111 1011	0 1	- -	- -	- 2	Sub (A ← A - M) as Q_0Q_{-1} = 10 Arithmetic Shift Right A, Q, Q_{-1}
11110	0101	1	-	-	1	Arithmetic Shift Right A, Q, Q_{-1} as Q_0Q_{-1} = 11
11111	00101	1	-	-	0	Arithmetic Shift Right A, Q, Q_{-1} as Q_0Q_{-1} = 11

Result in AQ = 11111 00101 = $-2^9+2^4+2^2+2^0$ = -512+256+128+64+32+4+1 = -27

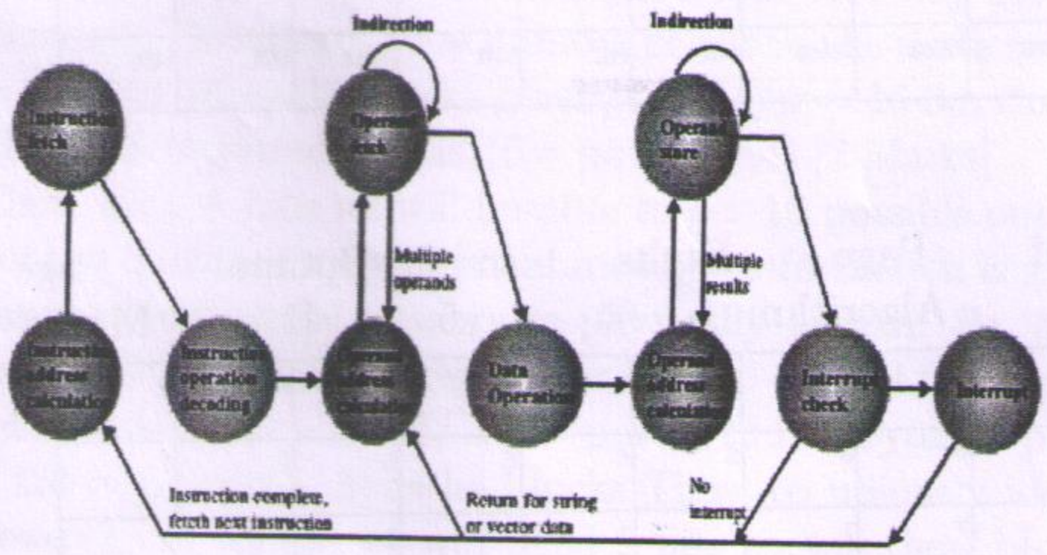
OR

Draw the flowchart and Divide 14 by 3 using Non-Restoring Division algorithm.
Flowchart [4 Marks]
Calculation [6 Marks]

Example: Divide 1110 (14) by 0011 (3) using non-restoring division.

A	Q	M	$\overline{M}$ +1	Count	Remarks
00000	1110	00011	11101	4	Initialization
00001 11110 11110	110□ 110□ 1100	- - -	- - -	- - 3	Shift Left A, Q Sub (A ← A – M) Set Q_0 to 0
11101 00000 00000	100□ 100□ 1001	- - -	- - -	- - 2	Shift Left A, Q Add (A ← A + M) Set Q_0 to 1
00001 11110 11110	001□ 001□ 0010	- - -	- - -	- - 1	Shift Left A, Q Sub (A ← A – M) Set Q_0 to 0
11100 11111 11111	010□ 010□ 0100	- - -	- - -	- - 0	Shift Left A, Q Add (A ← A + M) Set Q_0 to 0
00010	0100	-	-	-	Add (A ← A + M)

Quotient in Q = 0011 = 3
Remainder in A = 00010 = 2

Q.2 B.	How IEEE 754 Floating point represents number in Single and Double Precision? Give one example of each. Single Precision Format[2 Marks] Example[3 marks] Double Precision Format[2 Marks] Example[3 marks]	10	CO2
Q.3 A.	Explain different stages of Instruction cycle.Draw the Instruction cycle state diagram. Instruction cycle state diagram [4 Marks]  Different stages of Instruction cycle[6 marks] 1. Fetch 2. Execute 3. Indirect 4. Interrupt	10	CO3
Q.3 B.	Explain any two methods for systematic design of hardwired control logic Sequence counter method Delay element method State table method Any two[5 Marks each] **OR** Compare RISC and CISC Processor. What are the applications of RISC Comparison [6 Marks] Applications[4 Marks]	10	CO3

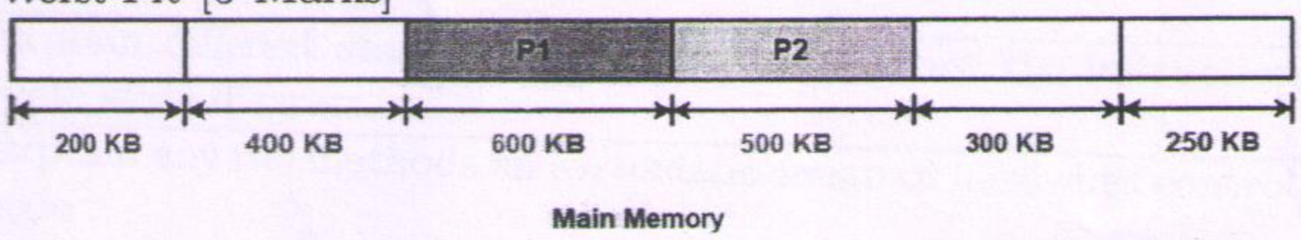
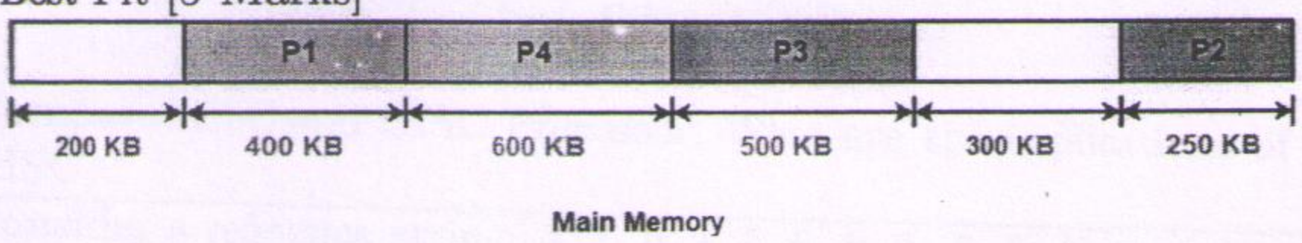
Q.4 A.	Consider a reference string: 4, 7, 6, 1, 7, 6, 1, 2, 7, 2. the number of frames in the memory is 3. Find out the number of page faults respective to Optimal Page Replacement Algorithm and LRU Page Replacement Algorithm.	10	CO4

Request	4	7	6	1	7	6	1	2	7	2
Frame 3			6	6	6	6	6	2	2	2
Frame 2		7	7	7	7	7	7	7	7	7
Frame 1	4	4	4	1	1	1	1	1	1	1
Miss/Hit	Miss	Miss	Miss	Miss	Hit	Hit	Hit	Miss	Hit	Hit

[4 Marks]
Number of Page Faults in Optimal Page Replacement Algorithm = 5 [1 Marks]

Request	4	7	6	1	7	6	1	2	7	2
Frame 3			6	6	6	6	6	6	7	7
Frame 2		7	7	7	7	7	7	2	2	2
Frame 1	4	4	4	1	1	1	1	1	1	1
Miss/Hit	Miss	Miss	Miss	Miss	Hit	Hit	Hit	Miss	Miss	Hit

[4 Marks]
Number of Page Faults in LRU = 6 [1 Marks]

Q.4 B.	Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB. Compute the number of bits in the TAG, SET and WORD fields respectively. According to the question it is given that No. of bytes in a word= 1byte No. of words per block of memory= 128 words Total size of the cache memory= 8 KB So the Cache size/(no. words per block* size of 1 word) = 8KB/(128*1) =64[2 Marks] Since, it is given that the computer has a 4 way set associative memory. Therefore, Total number of sets in the cache memory given = number of cache blocks given/4 = 64/4 = 16 So, the number of SET bits required = 4 as 16= power(2, 4).[2 Marks] Thus, with 4 bits we will be able to get 16 possible output bits As per the question only physical memory information is given we can assume that cache memory is physically tagged. So, the memory can be divided into 16 regions or blocks. Size of the region a single set can address = 1MB/ 16 = power(2, 16)Bytes = power(2, 16) / 128 = power(2, 9) cache blocks Thus, to uniquely identify these power(2, 9) blocks we will need 9 bits to tag these blocks. Thus, TAG= 9 Cache block is 128 words so for indicating any particular block we will need 7 bits as 128=power(2,7). Thus, WORD = 7. Hence the answer will be (TAG, SET, WORD) = (9,4,7). [6 marks] **OR** Consider six memory partitions of size 200 KB, 400 KB, 600 KB, 500 KB, 300 KB and 250 KB. These partitions need to be allocated to four processes of sizes 357 KB, 210 KB, 468 KB and 491 KB in that order. Perform the allocation of processes using Worst Fit Algorithm and Best Fit Algorithm. Worst Fit [5 Marks]  Best Fit [5 Marks] 	10	CO4
Q.5 A.	What are the different types of Bus allocation Policies Fixed priority [2.5 Marks] Rotating priority [2.5 Marks] Fair policies [2.5 Marks] Hybrid policies [2.5 Marks]	10	CO6

Q.5 B.	Explain Data hazards with example. What are the types of data hazards? Data hazards with example[4 Marks] Read after write (RAW), or true dependency[2 Marks] Write after read (WAR), or antidependency[2 Marks] Write after write (WAW), or output dependency[2 Marks] **OR** Explain Flynn's Classification in detail. Single instruction, single data stream - SISD [2.5 Marks] Single instruction, multiple data stream - SIMD [2.5 Marks] Multiple instruction, single data stream - MISD [2.5 Marks] Multiple instruction, multiple data stream- MIMD [2.5 Marks]	10	CO5