Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination

July 2019

SYNOPTIC

Max. Marks: 60 **Duration: 3 Hrs**

Class: SE **Semester: IV**

Course Code: CE44/IT42 **Branch: Computer/IT**

Name of the Course: Computer Organization and Architecture

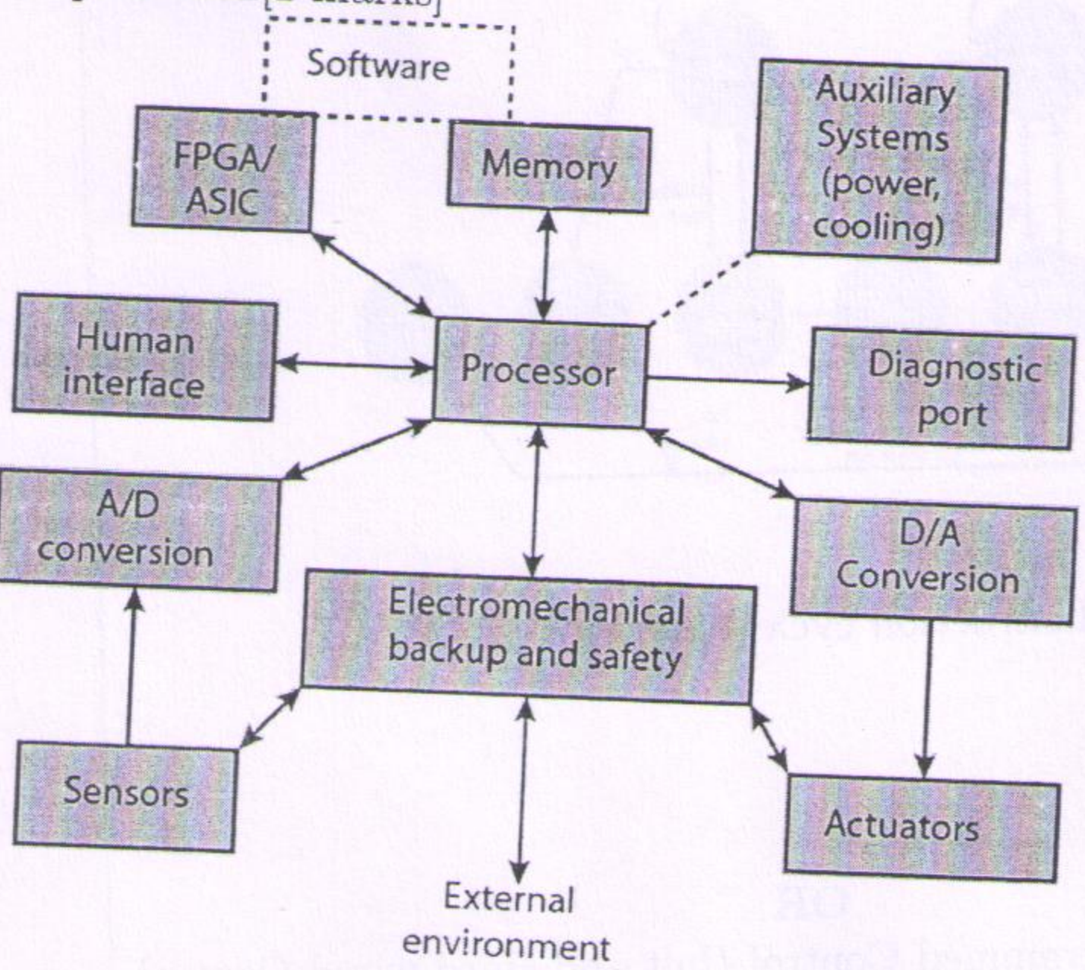
Instructions:

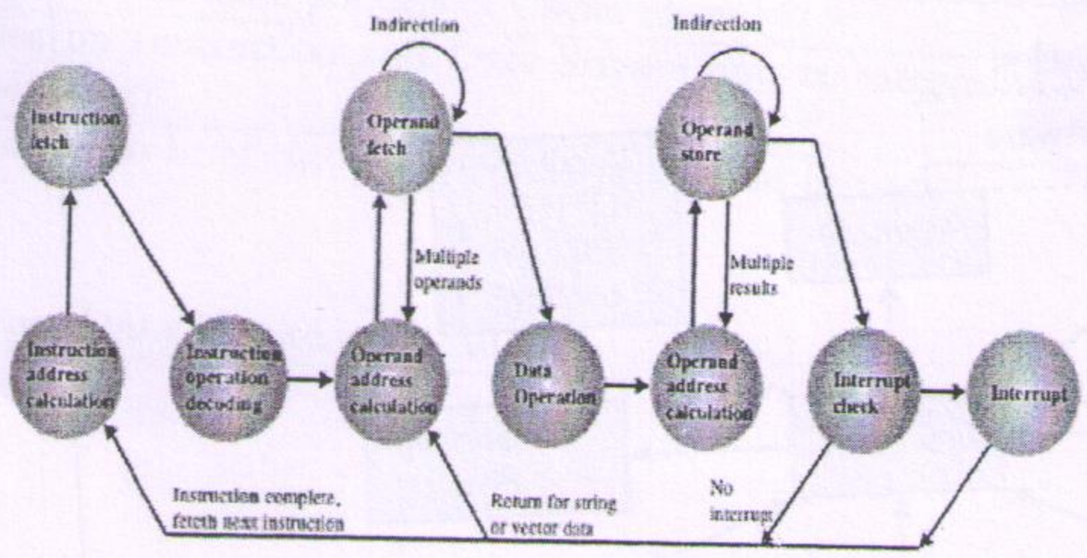
(1) All questions are compulsory

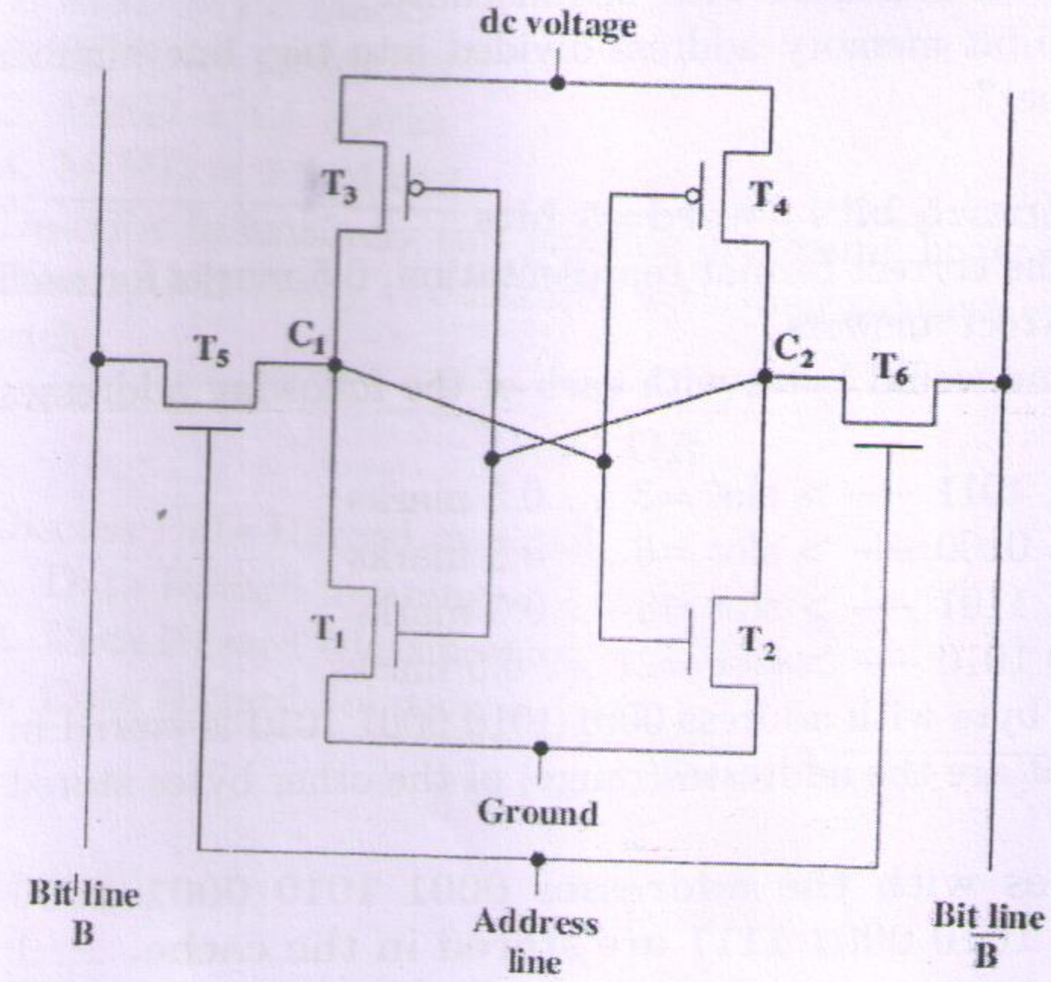
(2) Assume suitable data if necessary

(3) Draw neat diagram wherever required.

Q No.		Max. Marks	CO
Q.1 A	What are the different requirements of Embedded Systems? Explain possible organization of Embedded system with diagram. Different requirements [2 Marks] 1.Safety, reliability, real-time, flexibility, legislation 2.Lifespan 3.Environmental conditions 4.Static v dynamic loads 5.Slow to fast speeds 5.Computation v I/O intensive 6.Discrete event v continuous dynamics Diagram[2 marks] Explanation[2 marks]	5	CO1



Q.1 B.	What is Multicore Architecture? Explain how it is useful to improve the performance computer system. **Solution:** 1. Diagram = 2 Marks 2. Performance improvement of computer system by three solutions like Pipelining, Superscalar and Simaltaneous Multithreading = 3 Marks	5	
Q.2 A.	Draw the flowchart for Booth's Multiplication algorithm. Solve the following example using Booth's Multiplication algorithm - Muliplicand = (13) and Multiplier = 5 1. Flowchart = 1 Mark 2. Correct Binary Representation of 13 = 0 1 1 0 1 and 5 = 0 0 1 0 1 = 1 Mark 3. Application of Booths Algorithm and Correct Result = 65 = 0 0 0 1 0 0 0 0 0 1 = 2 Marks	5	CO2
Q.2 B.	Represent 28.125 in IEEE 754 Single Precision format and Double Precision format. Conversion[1 Marks] Single Precision format[2 marks] 0 10000011 110000100... Double Precision format[2 marks] 0 10000000011 110000100..	5	CO2
Q.3 A.	Explain about various Processor Registers. Describe following 5 Processor Register = 1 Mark for each PC, MAR, MBR, IR, Accumulator	5	CO3
Q.3 B.	Draw the Instruction cycle state diagram. Explain different stages of Instruction cycle. Instruction cycle state diagram [2 Marks]  Different stages of Instruction cycle[4 marks] 1. Fetch 2. Execute 3. Indirect 4. Interrupt **OR** Compare Microprogrammed Control Unit and Hard-wired Control Unit. Mention Advantages and Disadvantages of each. Comparison[4 Marks] Advantages and Disadvantages of each [2 Marks]	6	CO3

	Enlist any four features of CISC. Enlist any 4 features 1 Mark for each.	4	CO3
4 A.	Explain the cell structure of SRAM. Diagram - 2 marks  Explanation - 2 marks	4	CO4

Q.4 B.	Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. a. How is a 16-bit memory address divided into tag, line number and byte number? **Answer:** **tag=8 bits; line=5 bits ; word=3 bits** 0.5 marks for the correct format representation, 0.5 marks for each of the three correct answers b. Into what line would bytes with each of the following addresses be stored? 0001 0001 0001 1011 −− > slot =3 .... 0.5 marks 1100 0011 0011 0100 −− > slot =6 .... 0.5 marks 1101 0000 0001 1101 −− > slot =3 .... 0.5 marks 1010 1010 1010 1010 −− > slot =21 .... 0.5 marks c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses(range) of the other bytes stored along with it? **Answer: Bytes with the addresses 0001 1010 0001 1000 through 0001 1010 0001 1111 are stored in the cache.** .... 1 mark d. How many total bytes of memory can be stored in the cache? .... 1 mark **OR** Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size. a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units of main memory, number of blocks in main memory, number of lines in cache, size of tag. **Answer:-** **Address format: Tag=20 bits, Line=6 bits Word=6 bits** **Number of addressable units=**$2^{s+w} = 2^{32} bytes$ **Number of blocks in main memory=**$2^s = 2^{26}$ **Number of lines in cache** $2^r = 2^6 = 64$ **size of tag=20 bits** 3 mrks if all the results are correct, otherwise 0.5 marks will be reduced for each incorrect answer. b. Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag. **Answer:-** **Address format : Tag=9 bits, Set=17 bits Word=6 bits** **Number of addressable units=**$2^{s+w} = 2^{32} bytes$ **Number of blocks in main memory=**$2^s = 2^{26}$ **Number of lines in set** $k = 4$ **Number of sets in cache=** $2^d = 2^{17}$ **; number of lines in cache=**$k * 2^d = 2^{19}$ **size of tag=9 bits** 3 mrks if all the results are correct, otherwise 0.5 marks will be reduced for each incorrect answer.	6	
Q.4 C.	Describe the write policies of Cache memory? Explanation of write back policy - 2 marks Explanation of write through policy - 2 marks	4	CO4

	Based on Instruction and Data Stream how to categorize Parallel Processing? Description of following Flynn's Classification with Diagram 1. SISD = 1.5 Marks 2. SIMD = 1.5 Marks 3. MISD = 1.5 Marks 4. MIMD = 1.5 Marks	6	CO6
Q.5 B.	Describe in brief any two pipeline processing hazards. Description of any two hazards with their solution = 2.5 Marks for each **OR** Discuss Data Hazard in detail. 1. Data Hazard meaning = 2 Mark 2. Data Hazard Classification = 2 Marks 3. Data Hazard Solution = 1 Mark	5	CO5