Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination

May 2019

Max.Marks:60 **Duration:** 3 hours

Class: SE **Semester:** IV

Course Code: EL43 **Branch:** Electronics

Name of the Course: Computer Organization and Architecture

Synoptic

Q No		Max. Marks
Q 1 a)	Calculate number of external connections required for memory of size 1024 x 8 Bytes. Also draw memory interface diagram. Number of adress line 10 Number of Data Line 8 Power Supply 2 — 2 Marks Chip select 1 Read/Write 1 Inteface Diagram — 2 Marks	4
Q 1 b)	Block diagram of DMA controller — 1 Mark Description of Each module in short — 3 Marks or Block diagram of I/O Module — 1 Mark Description of Each module in short — 3 Marks	4
Q 1 c)	List — 1 Mark Description of each point (3X1) — 3 Marks	4
Q 2 a)	Diagram of micro programmed controller — 2 Marks	6

<table>
<tr><td></td><td>Description of each module with in it
Working</td><td>2 Marks
2 Marks</td><td></td></tr>
<tr><td>Q 2 b)</td><td>Calculation using formula
Mapping Diagram
Addressing format and look up
<table><tr><td>Tag=4 Bits</td><td>Cache line=10 Bits</td><td>Word=2 Bits</td></tr></table></td><td>2 Marks
2 Marks
2 Marks</td><td>6</td></tr>
<tr><td>Q 3 a)</td><td>Algorithm flowchart
Solving as per algorithm (5 Steps 1 mark each)
or
Algorithm flowchart
Solving as per algorithm (5 Steps 1 mark each)</td><td>1 Mark
5 Marks

1 Mark
5 Marks</td><td>6</td></tr>
<tr><td>Q 3 b)</td><td>Instruction formats explanation
Example
Basic instruction cycle explanation
Example</td><td>2 Marks
1 Mark
2 Marks
1 Mark</td><td>6</td></tr>
<tr><td>Q 4 a)</td><td>Register architecture diagram
Description</td><td>1 Mark
3 Marks</td><td>4</td></tr>
<tr><td>Q 4 b)</td><td>$(67)_8+(71)_8$
$(X)_S$</td><td>1 Mark
1 Mark</td><td>2</td></tr>
<tr><td>Q 4 c)</td><td>3 type of Bus Arbitration Techniques
(2 Marks for each comparison)
It should have
Diagram
Working
Advantages/Disadvantages
or
Any three types of bus (2 Marks Each)
Diagram And (1 Mark)
Explaination (1 Mark)</td><td>6 Marks</td><td>6</td></tr>
</table>

Q 5 a)	Von Neuman and Harvard Architecture **HARVARD ARCHITECTURE** / **VON-NEUMANN/PRINCETON ARCHITECTURE** This architecture consists of separate program and code memory. / It consists of common program and code memory. Execution of instructions are faster, because fetching of code and data are separate. / Execution of instructions is relatively slow ,because not possible to fetch code and data simultaneously. Execution of instruction takes less instruction (machine) cycle. / Execution of instruction takes more instruction (machine) cycle. Use RISC processor / Use CISC processor This is greater amount of parallelism / This is no need to have parallelism Chip design is complex because of separate memory. / The largest advantages is that it simplifies the chip design because only one memory is accessed. Eg: General microcontrollers (PIC), Special DSPs / E.g. Motorola -68HC11 microcontroller 8085 8086 MC6800 One mark for each point (6 Points x 1 Mark) There can be more points apart from these	6 Marks	6
Q 5 b)	Diagram of six stage pipe lining Description of what each stage Example Explanation Timing Diagram and explanation	1 Mark 2 Marks 1 Mars 2 Marks	6