Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination (Make-up)

July 2019

Max. Marks: 60 **Duration: 3 Hrs**

Class: SE **Semester: IV**

Course Code: CE44/IT42 **Branch: Computer/IT**

Name of the Course: Computer Organization and Architecture

Instructions:

(1) All questions are compulsory

(2) Assume suitable data if necessary

(3) Draw neat diagram wherever required.

Q No.		Max. Marks	CO
Q.1 A	What are the different requirements of Embedded Systems? Explain possible organization of Embedded system with diagram.	5	CO1
Q.1 B.	What is Multicore Architecture? Explain how it is useful to improve the performance of computer system.	5	CO1
Q.2 A.	Draw the flowchart for Booth's Multiplication algorithm. Solve the following example using Booth's Multiplication algorithm - Muliplicand = (13) and Multiplier = 5	5	CO2
Q.2 B.	Represent 28.125 in IEEE 754 Single Precision format and Double Precision format.	5	CO2
Q.3 A.	Explain about various Processor Registers.	5	CO3
Q.3 B.	Draw the Instruction cycle state diagram. Explain different stages of Instruction cycle. **OR** Compare Microprogrammed Control Unit and Hard-wired Control Unit. Mention Advantages and Disadvantages of each.	6	CO3
Q.3 C.	Enlist any four features of CISC.	4	CO3
Q.4 A.	Explain the cell structure of SRAM.	4	CO4

Q.4 B.	Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. a. How is a 16-bit memory address divided into tag, line number and byte number? b. Into what line would bytes with each of the following addresses be stored? 0001 0001 0001 1011 1100 0011 0011 0100 1101 0000 0001 1101 1010 1010 1010 1010 c. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses(range) of the other bytes stored along with it? d. How many total bytes of memory can be stored in the cache? **OR** Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size. a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units of main memory, number of blocks in main memory, number of lines in cache, size of tag. b. Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in set, number of sets in cache, number of lines in cache, size of tag.	6	CO4
Q.4 C.	Describe the write policies of Cache memory?	4	CO4
Q.5 A.	Based on Instruction and Data Stream how to categorize Parallel Processing?	6	CO6
Q.5 B.	Describe in brief any two pipeline processing hazards. **OR** Discuss Data Hazard in detail.	5	CO5