Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination

May 2019

Max. Marks: 60 **Duration: 3 Hrs**

Class: SE **Semester: IV**

Course Code: CE44/IT42 **Branch: Computer/IT**

Name of the Course: Computer Organization and Architecture

Instructions:

(1) All questions are compulsory

(2) Assume suitable data if necessary

(3) Draw neat diagram wherever required.

Q No.		Max. Marks	CO
Q.1 A	What are the four main functions of a computer? Explain with the help of a diagram.	5	CO1
Q.1 B.	What are the approaches to achieve the Performance/speed of the processor? What are the issues when the clock speed and logic density increases?	5	CO1
Q.2 A.	To solve the following problem use Restoring Division algorithm. Divisor = 3 & Dividend = 17 **OR** To solve the following problem use Non-Restoring Division algorithm. Divisor = 4 & Dividend = 18	5	CO2
Q.2 B.	How IEEE 754 Floating point represents number in Single and Double Precision? Give one example of each.	5	CO2
Q.3 A.	Compare Hardwired and Microprogrammed Control Unit design methods	5	CO3
Q.3 B.	Draw the diagram for Branch Control Logic: Two Address Fields and explain Microinstruction Sequencing techniques. **OR** What are the registers involved for microoperations? Mention the sequence of microoperations for different Instruction Cycle.	6	CO3
Q.3 C.	Why there is need of RISC? What are its features and its benefits?	4	CO3
Q.4 A.	What are the differences between EPROM and EEPROM? (Please write differences with respect to relevant points).	4	CO4

Q.4 B.	A set-associative cache has a block size of four 16-bit words and a set size of 2. The cache can accommodate a total of 4096 words. The main memory size that is cacheable is 64Kx32 bits. A.How many bits are needed to represent the TAG, SET and WORD fields? B.Design the cache structure and show(by drawing diagram) how the processor's addresses are interpreted. (No explanation is required.) **OR** A computer has a 256 KB, 4-way set associative, write back data cache with block size of 32 bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit. A. How many bits are there in the tag field of an address. B. What is the size of the cache tag directory? (Size of Cache directory is the number of lines in cache times the number of bits.)	6	CO4
Q.4 C.	A process references five pages, A, B, C, D, and E, in the following order: A; B; C; D; A; B; E; A; B; C; D; E Assume that the replacement algorithm is first-in-first-out and find the number of page transfers during this sequence of references starting with an empty main memory with three page frames. Repeat for four page frames. (Page frames at every instance of the page reference should be shown clearly).	4	CO4
Q.5 A.	What is the effect of a Conditional Branch on Instruction Pipeline Operation? How Six stage CPU Instruction pipeline is used to overcome branches and interrupts?	6	CO6
Q.5 B.	Explain any one implementation strategy for Centralized Arbitration scheme **OR** Explain I/O-to-Memory transfer through processor.	5	CO5