Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India
(Autonomous College Affiliated to University of Mumbai)

End Semester Examination
July 2022

Max. Marks: 60 **Class: S.E.** **Course Code: ET201/EC201**	**Duration: 120 mins** **Semester: III (DSE)** **Branch: ETRX & EXTC**

Name of the Course: Computer Architecture and Organization

Instruction:
(1) Draw neat diagrams
(2) Assume suitable data if necessary
(3) Write proper question numbers in the answer sheet

Q No	QUESTIONS	Max Marks	CO
1(a)	Consider the execution of a program that results in the execution of 2 million instructions on a 400-MHz processor. The program consists of four major types of instructions. The instruction mix and the CPI for each instruction type are given below based on the result of a program trace experiment: Find the (a) Average CPI and (b) MIPS rating	4	CO1
1(b)	Suppose that a task makes extensive use of floating-point operations, with 40% of the time is consumed by floating-point operations. With a new hardware design, the floating-point module is speeded up by a factor of K. Calculate the overall speedup and maximum speed possible.	4	CO1
2(a)	Perform Restoring division on (+15) / (-4). (Show proper steps and final answer properly) **OR** Use the Booth algorithm to multiply +15 (multiplicand) by -15 (multiplier). (Show proper steps and final answer properly)	6	CO2

Instruction Type	CPI	Instruction Mix (%)
Arithmetic and logic	1	60
Load/store with cache hit	2	18
Branch	4	12
Memory reference with cache miss	8	10

2(b)	Show how the following binary floating-point additions are performed (where significands are truncated to 4 decimal digits). Show the results in normalized form a) $5.566 \times 10^2 + 7.777 \times 10^2$ b) $3.344 \times 10^1 + 8.877 \times 10^{-2}$	6	CO2
3(a)	Enumerate the generation of control signals PCin and Zout using hardwired control signal generation method for the given below instructions (i) BZ label (ii) ADD R1, LOCA (iii) STORE LOCA, R1	10	CO3
3(b)	In the concept of n-stage pipeline, the performance improvement has been observed to be by the facto n. Prove this fact by deriving the relation of Speed Up Factor. Are there any factors which can affect or degrade the pipeline processor's performance?	6	CO5
4(a)	It is required to design Direct Mapped Cache Subsystem with the following specifications: a. Main Memory Size of 4GB b. Block Size of 8 Bytes c Cache Memory Size of 32 KB d. Line Size of 8 Bytes Answer the following: 1) Address Interpretation by Main Memory 2) Address Interpretation by Cache Memory 3) Design of Line Entry 4) Conceptual Diagram of the System **OR** It is required to design Two-way associative Mapped Cache Architecture with the following specifications: a. Main Memory Size of 4 GB b. Block Size of 8 Bytes c Cache Memory Size of 32 KB d. Line Size of 8 Bytes Answer the following: 1) Address Interpretation by Main Memory 2) Address Interpretation by Cache Memory 3) Design of Line Entry 4) Conceptual Diagram of the System	8	CO3 CO4

4(b)	An application program has 2000 instructions accessed from cache memory and 300 instructions from the main memory. While accessing main memory, three wait states are necessary per instruction. Calculate (1) Hit Rate (2) Miss Rate (3) Average number of wait states that are experienced during the execution of the program	4	CO3 CO4
5(a)	Devise the mechanism to implement the concept of virtual memory through segmentation. Support your answer by taking a typical processor with address translation procedure.	6	CO3 CO4
5(b)	In Polling I/O and Interrupt I/O, there is one pitfall (drawback). Identify this with an example and suggest the solution and describe the solution in detail with neat diagram.	6	CO6