Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

Re Examination (2018-19)

January 2020

Max. Marks: 60 Duration: 3 Hrs.

Class: SE Semester:IV

Course Code: CE44/IT42 Branch: Computer/IT

Name of the Course: Computer Organization and Architecture

Instructions:

(1) All questions are compulsory

(2) Assume suitable data if necessary

(3) Draw neat diagram wherever required.

Q. No.		Max. Marks	CO-BL-PI
Q.1 A	Write a short note on "The Von Neumann Machine".	6	1-2-2.2.2
Q.1 B	What are the Requirements of Embedded Systems? Explain Possible Organization of an Embedded System	6	1-2-2.2.2
Q.2 A	Draw the flowchart and Multiply 5 x -4 using Booth's Algorithm **OR** Draw the flowchart of Restoring and Non Restoring Division Algorithm	6	2-2-2.1.3
Q.2 B	How IEEE 754 Floating point represents number in Single and Double Precision? Give one example of each.	6	2-3-2.3.1
Q.3 A	How data flow occurs in Indirect cycle and Interrupt Cycle?	6	3-2-2.2.2
Q.3 B	What are the features of RISC and CISC Processor. Why is the need of RISC processor? **OR** What are the functions of Control Unit? What are the control signals associated with control Unit?	6	3-2-2.2.4 3-2-2.2.2
Q.4 A	Distinguish between the semiconductor types of memory (RAM, PROM, EPROM, EEPROM) with respect to any four relevant points [For e.g., Category(read only/write only), erasure, Write mechanism, Volatility,etc.]	8	4-2-2.2.4
Q.4 B	What are the drawbacks of Programmed and Interrupt-Driven I/O?	4	5-2-2.4.3

Q.5 A	Consider a main memory with five page frames and the following sequence of page references: 3. 8, 2, 3, 9, 1, 6, 3, 8. 9, 3, 6, 2, 1, 3. Which one of the following is true with respect to page replacement policies First-In-First-out (FIFO) and Least Recently Used (LRU)? a. Both incur the same number of page faults b. FIFO incurs 2 more page faults than LRU c. LRU incurs 2 more page faults than FIFO d. FIFO incurs 1 more page faults than LRU OR Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size. a. Assume a direct mapped cache with a tag field in the address of 20 bits. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag. b. Assume an associative cache. Show the address format and determine the following parameters: number of addressable units, number of blocks in main memory, number of lines in cache, size of tag.	6	4-3-2.4.1
Q.5 B	What are the different pipeline hazards? Explain each of them.	6	6-2-2.2.2