Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination

May 2019

SYNOPTIC

Max. Marks: 60 **Duration: 3 Hrs**

Class: SE **Semester: IV**

Course Code: CE44/IT42 **Branch: Computer/IT**

Name of the Course: Computer Organization and Architecture

Instructions:

(1) All questions are compulsory

(2) Assume suitable data if necessary

(3) Draw neat diagram wherever required.

Q No.		Max. Marks	CO
Q.1 A	What are the four main functions of a computer? Explain with the help of a diagram. Synoptic:- • Data processing • Data storage • Data movement • Control 4 marks for the explanation of each functions. 1 mark for proper diagram.	5	CO1
Q.1 B.	What are the approaches to achieve the Performance/speed of the processor? What are the issues when the clock speed and logic density increases? Approaches to achieve the Performance/speed of the processor[3 Marks] 1. Increase hardware speed of processor 2. Increase size and speed of caches 3.Change processor organization and architecture Parallelism Issues when the clock speed and logic density increases[2 Marks] 1. Power 2. RC delay 3. Memory latency	5	CO1

Q.2 A.	To solve the following problem use Restoring Division algorithm. Divisor = 3 & Dividend = 17 **Synoptic:** M = 3 = 00011 [1 M] Q = 17 = 10001 [1 M] For following correct table [3 M]	5	CO2

Steps	A	Q
Initial	00000	10001
LS	00001	0001_
A-M	11110	00010
A+M	00001	00010
LS	00010	0010_
A-M	11111	00100
A+M	00010	00100
LS	00100	0100_
A-M	00001	01001
LS	00010	1001_
A-M	11111	10010
A+M	00010	10010
LA	00101	0010_
A-M	00010	00101
	Remainder = 2	Quotient = 5

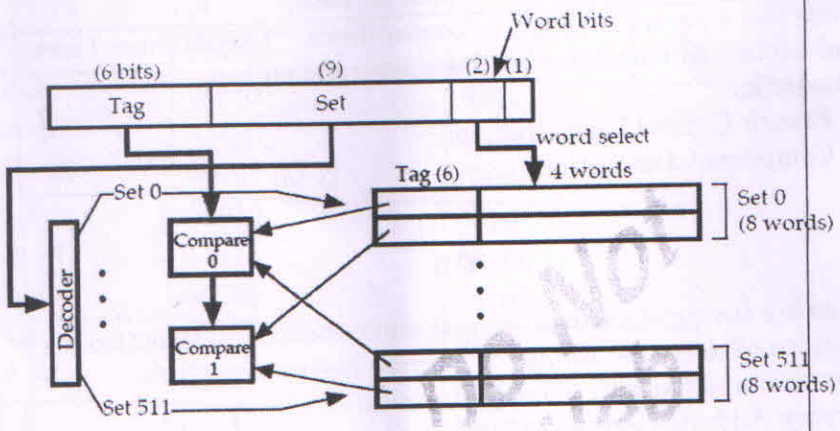
OR

To solve the following problem use Non-Restoring Division algorithm.
Divisor = 4 & Dividend = 18
Synoptic:
M = 4 = 00100 [1 M]
Q = 10010 [1 M]
For following correct table [3 M]

Steps	A	Q
Initial	00000	10010
LS	00001	0010_
A-M	11101	00100
LS	11010	0100_
A+M	11110	01000
LS	11100	1000_
A+M	00000	10001
LS	00001	0001_
A-M	11101	00010
LS	11010	0010_
A+M	11110	00100
A+M (Restore)	00010	00100
	Remainder = 2	Quotient = 4

Q.2 B.	How IEEE 754 Floating point represents number in Single and Double Precision? Give one example of each. Single Precision Format[1 Marks] Example[1.5 marks] Double Precision Format[1 Marks] Example[1.5 marks]	5	CO2
Q.3 A.	Compare Hardwired and Microprogrammed Control Unit design methods **Synoptic:** Any 5 points [1 Mark for each]	5	CO3
Q.3 B.	Draw the diagram for Branch Control Logic: Two Address Fields and explain Microinstruction Sequencing techniques. **Synoptic:** 1. Branch Control Logic diagram [3 M] 2. Component Description [3 M] **OR** What are the registers involved with microoperations? Mention the sequence of microoperations for different Instruction Cycle. Registers involved with microoperations[2 Marks] Memory Address Register (MAR) Memory Buffer Register (MBR) Program Counter (PC) Instruction Register (IR) Sequence of microoperations for different Instruction Cycle.[1 Marks for each Instruction Cycle]	06	CO3
Q.3 C.	Why there is need of RISC? What are its features and its benefits? Need of RISC [1 M] Features [2 M] benefits [1 M]	4	CO3
Q.4 A.	What are the differences between EPROM and EEPROM? (Please write differences with respect to relevant points). Synoptic:- any 4 relevant distinguishing points - 4 mark	4	CO4

Q.4 B.	A set-associative cache has a block size of four 16-bit words and a set size of 2. The cache can accommodate a total of 4096 words. The main memory size that is cacheable is 64Kx32 bits. A.How many bits are needed to represen the TAG, SET and WORD fields? B.Design the cache structure and show(by drawing diagram) how the processor's addresses are interpreted. (No explanation is required.)	6	CO4



Synoptic:- 3 marks to find the number of bits needed to represent the TAG, SET and WORD fields. 2 marks for diagram showing the cache mapping organization.

OR

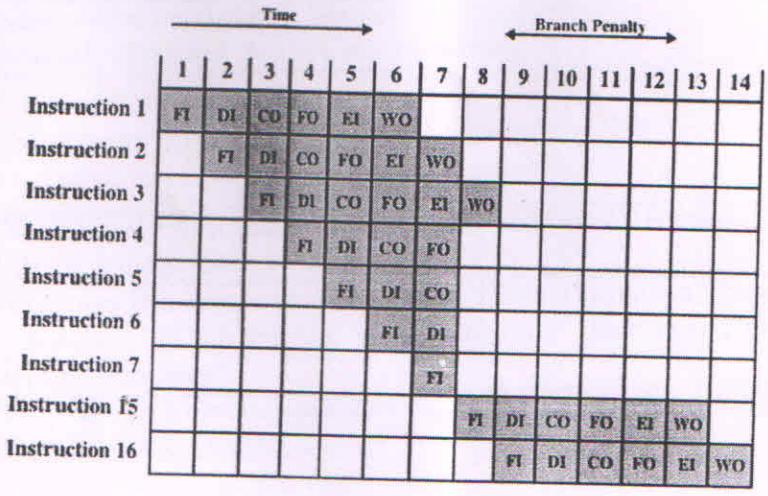
A computer has a 256 KB, 4-way set associative, write back data cache with block size of 32 bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

A. How many bits are there in the tag field of an address.

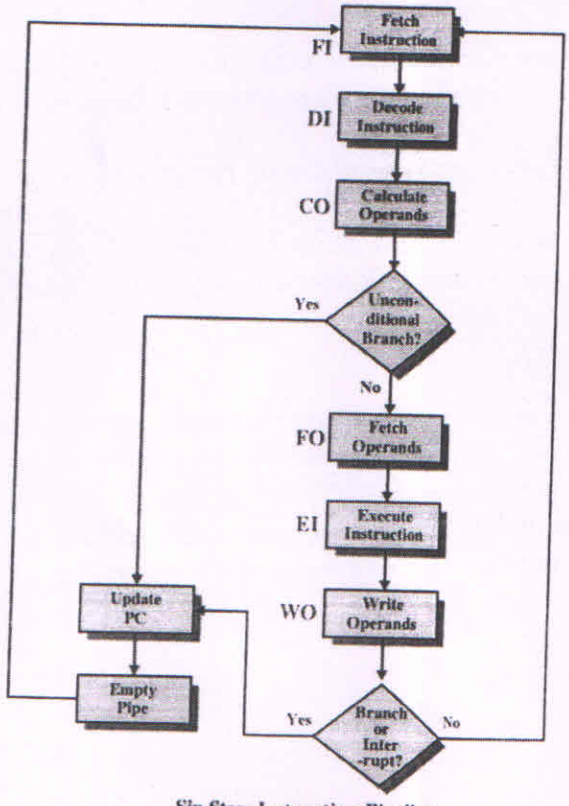
B. What is the size of the cache tag directory? (Size of Cache directory is the number of lines in cache time the number of bits.)

Synoptic:- Given- Cache memory size = 256 KB ,Set size = 4 blocks
Block size = 32 bytes, Number of bits in physical address = 32 bits
Number of Bits in Block Offset-
We have- Block size= 32 bytes= $2^5 bytes$
Thus, Number of bits in block offset = 5 bits
Number of lines in cache= Cache size / Line size
= 256 KB / 32 bytes = 2^{18} bytes / 2^5 bytes = 2^{13} lines
Number of sets in cache= Number of lines in cache / Set size
= 2^{13} lines / 2^2 lines
= 2^{11} sets
Thus, Number of bits in set number = 11 bits
Number of Bits in Tag-Number of bits in tag = Number of bits in physical address – (Number of bits in set number + Number of bits in block offset)
= 32 bits - (11 bits + 5 bits) = 32 bits - 16 bits = 16 bits
4 marks for finding correct number of bits in the tag field. formulae should be written correctly. There should be correct interpretation of given data, otherwise marks will be deducted accordingly.
Size of tag directory = Number of lines in cache x Size of tag = 2^{13} x (16 bits + 2 valid bits + 1 modified bit + 1 replacement bit) = 2^{13} x 20 bits = 163840 bits
2 marks for finding correct number of bits

Q.4 C.	A process references five pages, A, B, C, D, and E, in the following order: A; B; C; D; A; B; E; A; B; C; D; E Assume that the replacement algorithm is first-in-first-out and find the number of page transfers during this sequence of references starting with an empty main memory with three page frames. Repeat for four page frames. (Page frames at every instance of the page reference should be shown clearly). Synoptic: - 9 transfers for three frames - 2 marks will be given and 10 transfers for four frames- 2 marks Step by step page allocation to correct frames should be shown	4	CO4
Q.5 A.	Diagrams 4 Marks Description 2 marks	6	CO6



The Effect of a Conditional Branch on Instruction Pipeline Operation



Six-Stage Instruction Pipeline

Q.5 B.	Explain the any one implementation strategy for Centralized Arbitration scheme **Synoptic:** Any of the scheme Da sy Chaining / Independent Request 1. Diagram [2 M] 2. Description [3 M] **OR** Explain I/O-to-Memory transfer through processor. **Synoptic:** 1. Programmed I/O [2.5 M] 2. Interrupt-driven I/O [2.5 M]	5	CO5