Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination

January 2022

Max. Marks: 60 **Duration: 2 Hrs**
Class: S.E. **Semester: III**
Course Code: ET201/EC201 **Branch: Electronics/ EXTC**
Name of the Course: Computer Architecture and Organization

Instruction:

(1) All questions are compulsory
(2) Draw neat diagrams
(3) Assume suitable data if necessary

Q No.		Max. Marks	CO-BL
Q.1 (a)	Perform Non Restoring division on (-16) / (+7). (Show proper steps and final answer properly) OR Perform +16 X (-17) using Booth's algorithm. (Show proper steps and final answer properly)	06	2-3
Q.1 (b)	Show how CPU performs floating point computation on these numbers (Shows all the steps according to algorithm) -0.7236 + 0.1394	06	2-3
Q.2 (a)	Compare horizontal, vertical and diagonal micro programmed encoding with respect to any example. OR Explain the data flow of Indirect cycle with diagram using the instruction of 8086 processor ADD AX, [SI]	06	3-2
Q.2 (b)	List down the control signal generation of instruction "ADD LOCA, R0" using single bus organization. Assume the instruction stored in memory and write the control signal with respect to time stamps from fetch stage.	06	3-2
Q.3 (a)	Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. a. Which processor has the highest performance expressed in instructions per second? b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions. c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?	06	1-3

Q.3 (b)	Benefits of Pipelining concept are well appreciated in the architecture designer's fraternity. But, these benefits are realized only if one significant condition is satisfied. Mention and justify this condition. There are some barriers in satisfying this condition. Discuss in detail these barriers (also known as hazards).	06	5-2
Q.4 (a)	Design Direct Mapped Cache Architecture with the following specifications: a. Main Memory Size of 1GB b. Block Size of 32 Bytes c Cache Memory Size of 64 KB d. Line Size of 32 Bytes Answer the following: 1) Address Interpretation by Main Memory 2) Address Interpretation by Cache Memory 3) Design of Line Entry 4) Conceptual Diagram of the System OR Design Two way associative Mapped Cache Architecture with the following specifications: a. Main Memory Size of 1GB b. Block Size of 32 Bytes c Cache Memory Size of 64 KB d. Line Size of 32 Bytes Answer the following: 1) Address Interpretation by Main Memory 2) Address Interpretation by Cache Memory 3) Design of Line Entry 4) Conceptual Diagram of the System	08	3,4-3
Q.4 (b)	Typically, main memory is always implemented using DRAM instead of SRAM even though DRAM's memory access time is too large. Justify by comparing between these two types of memory.	04	3-2
Q.5 (a)	As an illustration, 80386 uses the concept of virtual memory through paging technique that uses virtual address of 48 bits. You are supposed to devise the mechanism for translating this virtual address to its 32 bits physical address. The answer must consist of all the necessary steps and depicted through neat diagram.	08	3,4-3
Q.5 (b)	Compare and contrast Interrupt I/O method with DMA I/O method.	04	6-2