Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058. India

(Autonomous College Affiliated to University of Mumbai)

Mid Semester Examination

October 2022

Max. Marks: 20 Duration: 60 Min

Class: S.E. Semester: III

Course Code: CS203/AI203/EC201/DS203 Branch: All division

Name of the Course: Computer Architecture and Organisation Date:18/10/2022

Instruction:

(1) All questions are compulsory

(2) Draw neat diagrams

(3) Assume suitable data if necessary

Q No.		Max. Marks	CO-BL-PI
Q.1	Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2. a. Which processor has the highest performance expressed in instructions per second? b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions. c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?	05	1-3-1.4.1
Q.2	Multiply (-13) * (-6) using Booth's Algorithm Also draw the Flowchart of Booth's Algorithm.	05	1-3-2.4.1
Q.3	Describe the states of instruction and draw its finite state diagram (FSM) showing the possible flow of data-path in any instruction.	04	3-2-1.4.1
Q.4	Devise hypothetical data path using single bus organization (neat diagram essential) and answer the following: (a) Conceptual difference and necessity of Visible register PC and Hidden register MAR (b) For an instruction ADD R2,LOCA (Direct addressing mode), devise control step sequence with proper time steps.	06	3-2-1.4.1