

Logic families

Digital Integrated Circuits

Digital systems like digital measuring instruments, computers or microprocessor chips require hundred of logic gates in the form of switches. If mechanical switches or relays are used in such systems, the operation will be quite complex, will require more power and also size increases. These difficulties are overcome by using semiconductor technology and their components such as diodes, transistors, MOSFETs instead of mechanical switches. These semiconductor devices are much faster and they are manufactured on a single chip or in a single package. Integrated semiconductor ICs have significant advantages over normal discrete circuits such as small size, light weight, low power consumption, high speed and reliability.

Using advanced photographic techniques a manufacturer can produce miniature circuits on the surface of a chip (a small piece of semiconductor material.) The finished material network is so small you need a microscope to see the connections. Such a circuit is called an integrated circuit (IC) because the components (transistors, diodes, resistors) are an integral part of the chip. This is different from a discrete circuit in which the components are individually connected during assembly.

Small scale integration (SSI) refers to ICs with fewer than 12 gates on the

same chip: Medium scale integration (MSI) means 12 to 100 gates per chip. Large scale integration (LSI) refers to more than 100 gates less than 1000 gates per chip. Very large scale integration (VLSI) refers to more than 1000 gates per chip.

The two basic technologies for manufacturing digital ICs are bipolar and MOS or unipolar. Bipolar technology uses bipolar transistors on a chip & is preferred for SSI & MSI because it is faster.

MOS technology uses unipolar devices (MOSFETs) & dominates the LSI field because more MOSFETs can be packed on the same chip area.

A digital family is a group of compatible devices with the same logic levels & supply voltages. The word compatible means that you can connect the output of one device to the input of another.

Bipolar families

In the bipolar category we have these basic families:

DTL - Diode-transistor logic

TTL - Transistor-transistor logic

ECL - Emitter coupled logic

DTL uses diodes & transistors; these

design once popular, is now obsolete. Obsolete TTL uses transistors exclusively. It has become the most popular family of SSI & MSI chips. ECL, the fastest logic family, is used in high-speed applications.

MOS Families:—

In the MOS category we have these families:-

PMOS: p-channel MOSFET's

NMOS: n-channel MOSFET's

CMOS: Complementary MOSFET's

PMOS, the oldest & slowest type, is becoming obsolete. NMOS, dominates the LSI field & CMOS a push-pull arrangement of n- & p-channel MOSFET's, is extensively used where low power consumption is needed, as in pocket calculators.

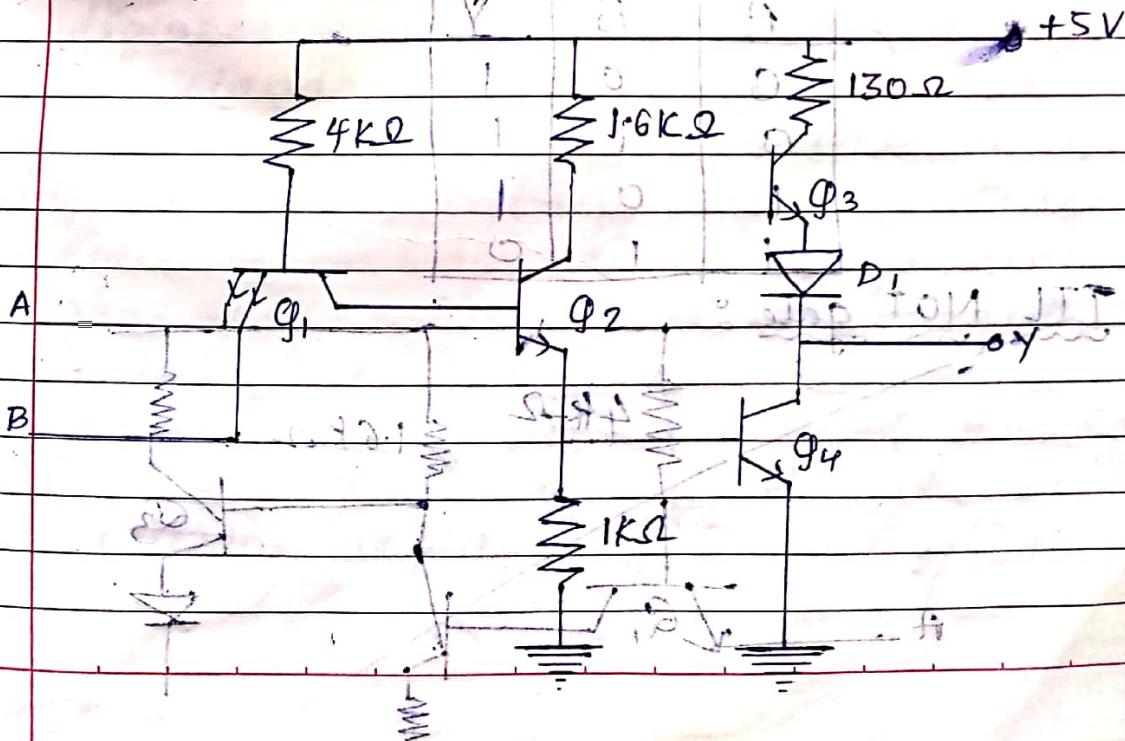
T400 devices:

The T400 series, the line of TTL circuits introduced by Texas Instruments in 1964, has become the most widely used of all bipolar IC's. The TTL family contains a variety of SSI & MSI chips that allow to build all kinds of digital circuits & systems.

Standard TTL

The figure below shows a TTL NAND gate. The multiple-emitter input transistor is typical of the gates & other devices in the 7400 series. Each emitter acts like a diode; therefore Q_1 & $4K\Omega$ resistor act like a 2-input AND gate.

The rest of the circuit inverts the signal so that the overall circuit acts like a 2-input NAND gate. The output transistors (Q_3 & Q_4) form a totem pole connection (one npn in series with another); this kind of output stage is typical of most TTL devices. With a totem-pole output stage, either the upper or lower transistor is on. When Q_3 is on, the output is high; when Q_4 is on, the output is low.



The input voltages A & B are either high (precedently grounded) or high (either if A or B go low, transistor Q1 will turn on). Therefore the collector voltage will be the voltage of Q2, which is cut off, cutting off Q4 after going into saturation & output Y will then be high.

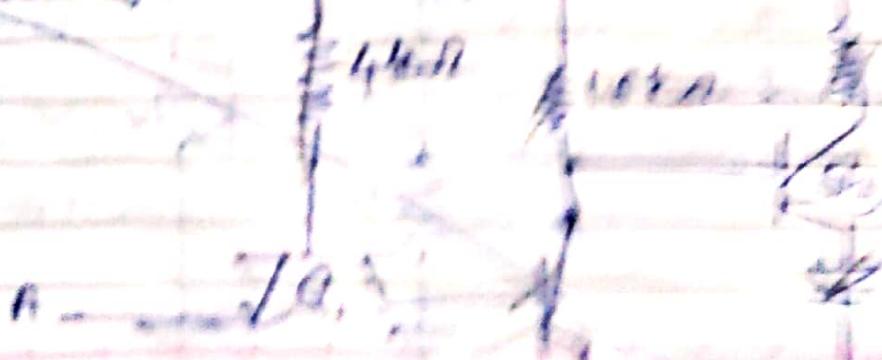
On the other hand, if A & B are both high, transistors Q1 & Q2 will conduct slightly. When the output is high, to prevent this, diode D1 is inserted in the output drop keeps the base-emitter voltage of Q2 pre-biased. In this way only Q4 conducts when the output is low.

Totem-pole inverters are used because they produce a low impedance output.

Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

The NOT gate:



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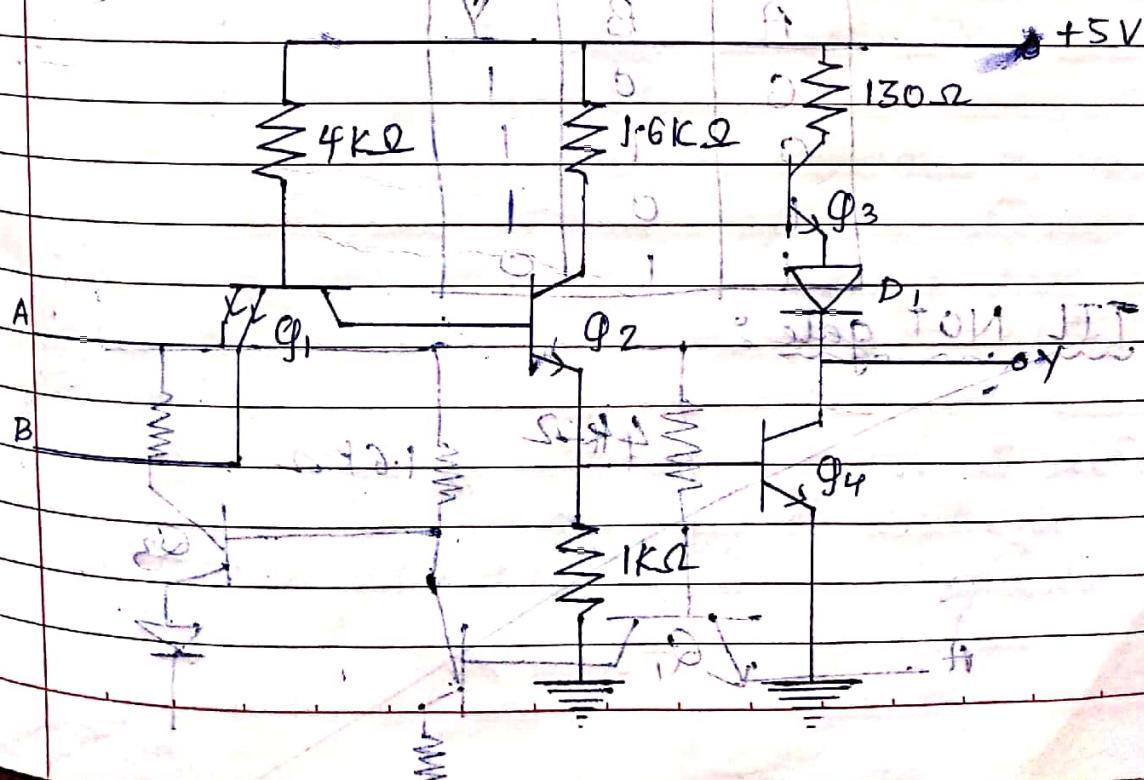
7400 devices:

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The input voltages A & B are either low (ideally grounded) or high (ideally +5V).

If A or B is low, transistor Q₁ conducts. Therefore its collector voltage i.e. base voltage of Q₂ reduces to almost zero. Q₂ cuts off, cutting off Q₄ also. Q₃ goes into saturation & output Y is therefore high.

On the other hand, when A & B are both high voltages, Q₁ cuts off & therefore Q₂ & Q₄ go into saturation. This results in a low output.

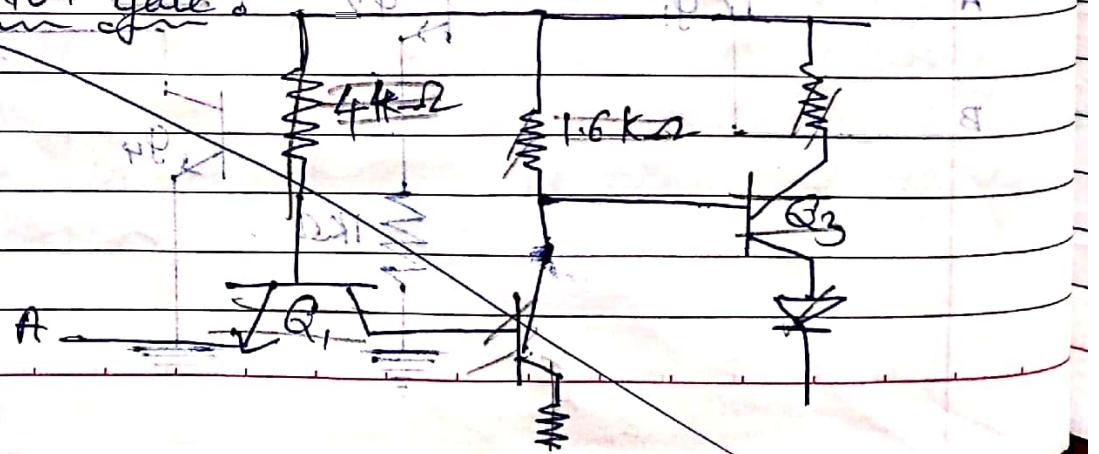
Without diode D₁ in the circuit, Q₃ will conduct slightly when the output is low. To prevent this, the diode is inserted so its voltage drop keeps the base-emitter diode of Q₃ reverse biased. In this way, only Q₄ conducts when the output is low.

Totem-pole transistors are used because they produce a low impedance output.

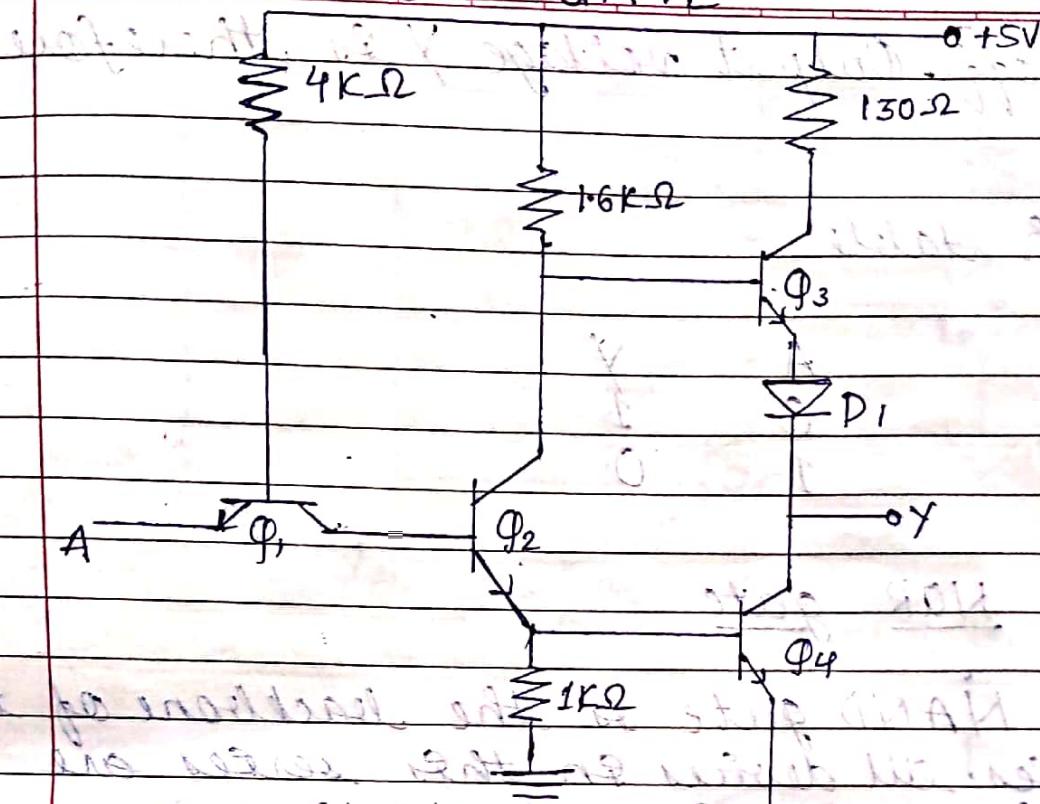
Truth Table

	A	B	Y
	0	0	1
	0	1	1
	1	0	1
	1	1	0

TTL NOT gate:



TTL NOT GATE



NOT gate has a single input and single output. Therefore, instead of the multiple-emitter input transistor Q_1 in the circuit of a standard TTL, we have a single-emitter input transistor Q_1 shown in the above figure. The rest of the circuit is same as standard TTL NAND.

With input voltage A low, Q_1 conducts, cutting off Q_2 & hence Q_4 . Collector voltage of Q_2 being high, Q_3 goes into saturation. Output voltage y is therefore high.

With input voltage A high, Q_1 cuts off, saturating Q_2 & hence Q_4 . Collector voltage of Q_2 being low,

: Q_3 cuts off. Output voltage Y is therefore low.

Truth table:

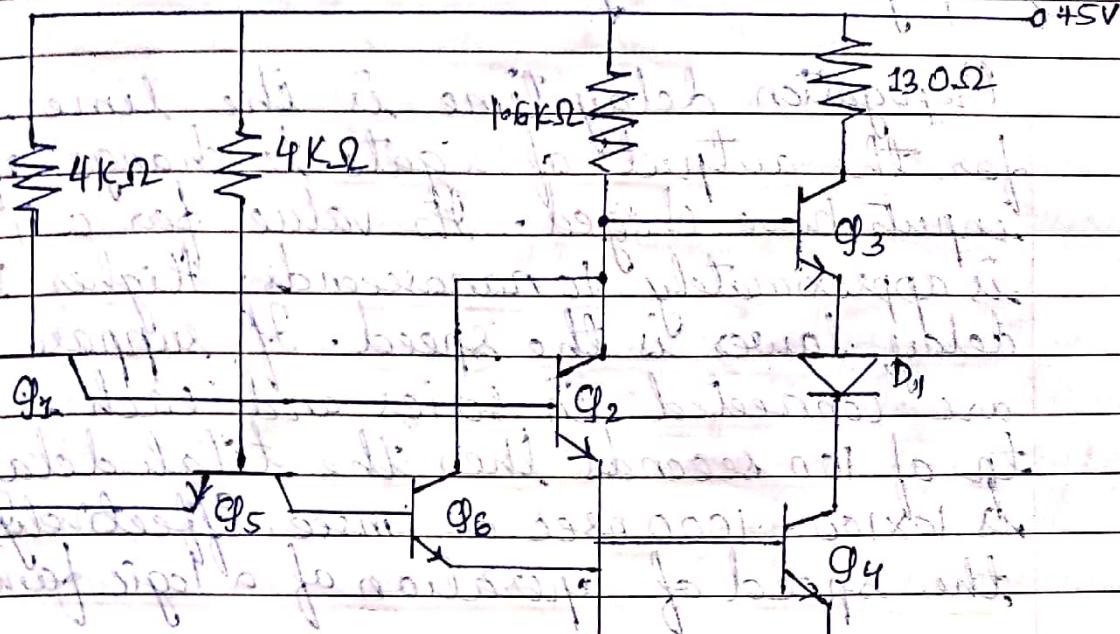
A	Y
0	1
1	0

TTL NOR gate

The NAND gate is the backbone of the 7400 series. All devices in this series are derived from the 2-input NAND-gate.

To produce 3-, 4- & 8-input NAND gates, the manufacturer uses 3-, 4-, 8-emitter input transistors. Because they are so basic, NAND gates are the least expensive devices in the 7400 series.

To get other logic functions the manufacturer modifies the basic NAND-gate design. For instance, the figure below shows a 2-input NOR gate. Here Q_5 & Q_6 have been added to basic NAND gate design. Since Q_2 & Q_6 have in parallel, we get the OR function, which is followed by inversion to get the NOR function.



When A & B are both low, then
transistors Q₁ & Q₅ conduct. This cuts off
Q₂ & Q₆, base voltage for Q₃ is 0. Therefore
high & it conducts. Q₄ is cut off; Output
voltage Y is hence high.

If A or B is high, Q₁ or Q₅ is
cut off forcing Q₂ or Q₆ to turn on. When
this happens, Q₄ saturates & Q₃ cuts off.
Output voltage Y is therefore low.

Truth Table:

A	B	Y
0	0	1
1	0	0

1) Propagation Delay Time:

Propagation delay time is the time it takes for the output of a gate to change after the inputs have changed. Its value for a TTL gate is approximately 10 nanoseconds. Higher the propagation delay, lower is the speed. If suppose 100 gates are connected in series and each is producing 10ns delay, then the total delay time is $10 \times 100 = 1000$ nsec or 1 μsec. Effectively, it limits the speed of operation of a logic family.

2) Power dissipation:

A standard TTL gate has a power dissipation of about 10 milliwatts (mW). It may vary from this value because of signal levels, tolerance, etc, but on the average it is 10mW per gate.

Low power dissipation is desirable because this will mean less heat generation and problems of cooling; power supply cast can be avoided. Power equals the product of supply voltage and device current. For example, a gate takes 2 mA current and is operated with 5V supply, then its power dissipation is calculated as $2 \times 10^{-3} \times 5 = 10\text{mW}$.

3) Figure of merit:

This characteristic indicates the total performance or quality of a family. If resistance of the circuit is increased to reduce the current or power dissipation, then the propagation delay increases. If however, we try to

reduce the propagation delay (to make it faster) by reducing the resistance, then more current is drawn by the gate, which increases the power dissipation. Therefore both these characteristics power dissipation and propagation delay are expressed in terms of figure of merit.

If GM is defined as the product of propagation delay and power dissipation of the gate. Figure of merit in the case of a standard TTL gate is $10\text{ nsec} \times 10\text{ mW} = 100$ Picoulombs. The lowest figure of merit indicates the best performance.

4) Current & Voltage parameters

V_{IL} : Low level Input voltage

$V_{IL,MAX}$: Maximum low level Input voltage = 0.8 V for TTL devices (worst case). i.e. Input voltage in the range 0V to 0.8V is a valid low state input for TTL devices.

V_{IH} : High level Input voltage

$V_{IH,MIN}$: Minimum high level Input voltage = 2V for TTL devices (worst case high input), i.e. Input voltage in the range 2V to 5V is a valid high state input.

If input voltage is greater than $0.8V$ & less than $2V$, the output state is unpredictable. i.e. there is no guarantee that it will produce the correct output voltage.

V_{OL} - Low level Output Voltage

V_{OLMAX} - Maximum low level output terminal voltage = $0.4V$ for TTL devices
i.e. worst case low output.

Output voltage in the range $0V$ to $0.4V$ is a valid low state output.

V_{OH} - High level Output voltage

V_{OHMIN} Minimum high level output voltage = $2.4V$ i.e. worst case holding high output. Output voltage in the range $2.4V$ to $5V$ is a valid high state output.

Any output between $0.4V$ & $2.4V$ is intermediate / invalid.

SV

5V

2V

2.4V

0.8V

0.4V

TTL input profile

TTL output profile

Valed
high
input

Valed
high
output

Invaled

Invaled

0V

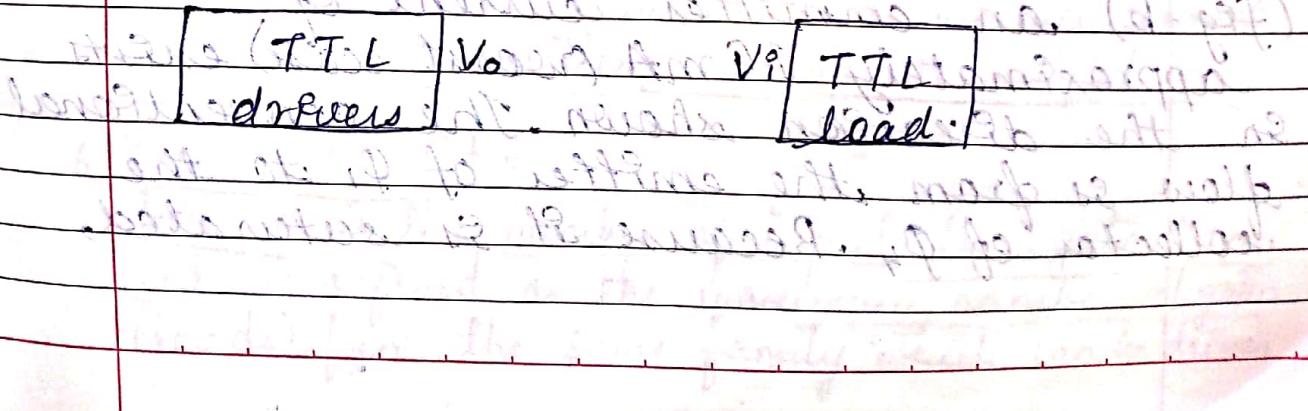
0V

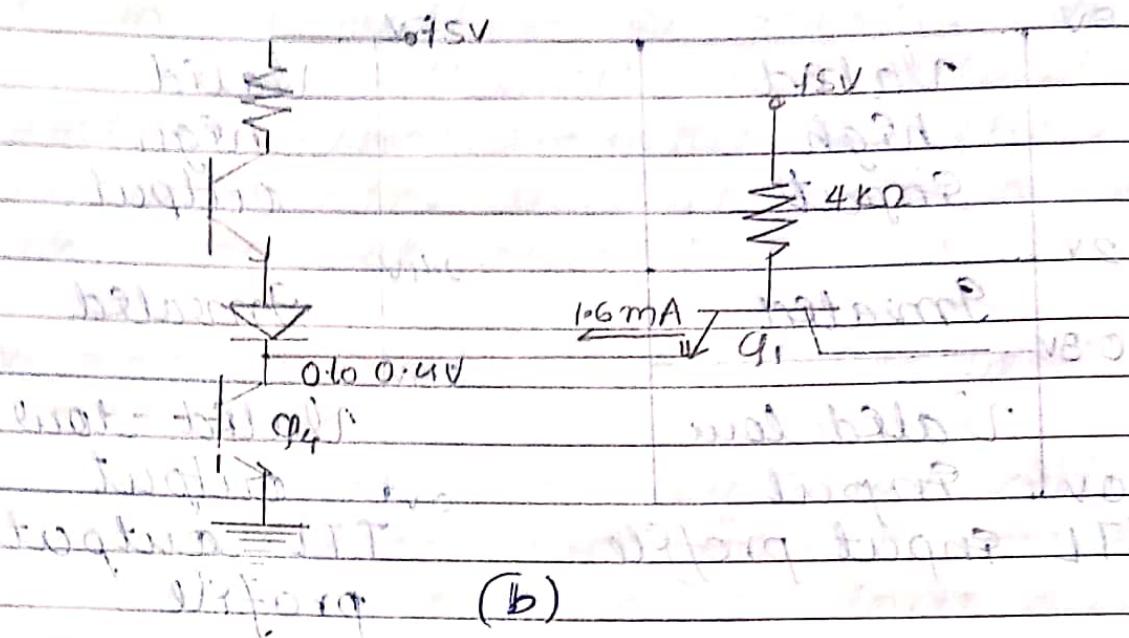
Valed low
0V input

Valed low
0V output

⑤ Current sinking, current sourcing

As TTL devices are compatible, the output of one TTL device is suitable for driving the input of another TTL device. For instance, the figure (a) below shows one TTL device driving another. The first device is called a driver & the second, a load. Figure (b) shows the output stage of the TTL driver connected to the input stage of the TTL load. The driver output is shown in the low state. Similarly, figure (c) shows a high TTL output





When a standard TTL output is low (fig. 6) an emitter current of approximately 1.6 mA (worst case) exists in the direction shown. The conduction flow is from the emitter of Q_1 to the collector of Q_4 . Because Q_1 is saturated,

Q_4 acts as a current source so conventional current flows through Q_4 to ground like water flowing down a sink.

However, when the standard TTL output is high (Fig. (c)), a reverse collector current of $40\ \mu A$ (worst case) exists in the direction shown. Conventional current flows out of Q_3 to the emitter of Q_1 . In this case, Q_3 is acting "as a source".

Data sheets list the worst-case input currents:

$$I_{I1,\text{MAX}} = -1.6\text{mA} \quad I_{I4,\text{MAX}} = 40\mu\text{A}$$

The minus sign indicates that the conventional current is out of the device; a plus sign means the conventional current is into the device.

Data sheets indicate that any 7400 series device can sink up to 16mA , designated

$I_{OL,\text{MAX}} = 16\text{mA}$ and can source up to $400\mu\text{A}$, designated $I_{OH,\text{MAX}} = -400\mu\text{A}$.

Since the maximum output currents are 10 times larger than the input currents, we can connect up to 10 TTL emitters to any TTL output.

6) Fan in - Fan out =

Fan in is the number of inputs to a gate. Fan out is defined as the maximum number of gates (loads) from the same family which can be driven.

reliably. In case of TTL format is 10, that is maximum 10 TTL gates can be connected to the output terminal of a TTL gate.

7) Noise Immunity: (X) Deleted

Noise immunity is defined as the maximum noise voltage a device can withstand without making a false change in output.

In the worst case, there is a difference of 0.4V between the driver output voltages and required load input voltages. For eg, the worst case low values are

$$V_{OL\text{MAX}} = 0.4V \text{ driver output}$$

$$V_{IL\text{MAX}} = 0.8V \text{ load input}$$

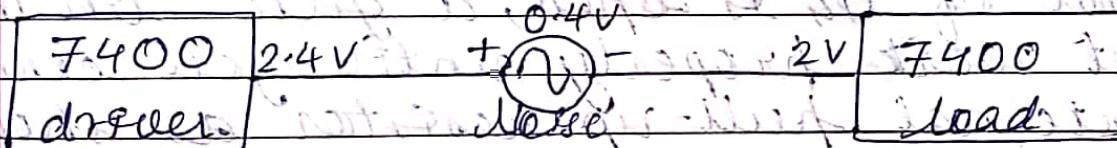
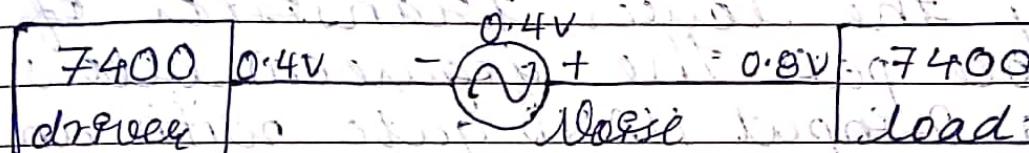
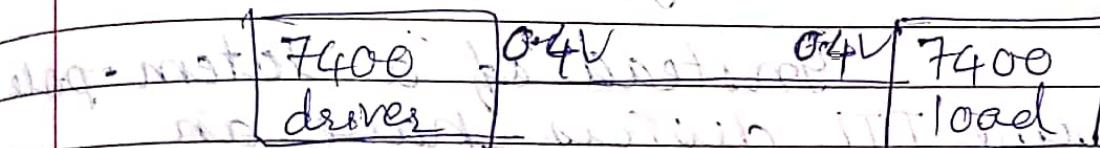
Similarly, the worst-case high values are

$$V_{OH\text{MIN}} = -2.4V \text{ driver output}$$

$$V_{IH\text{MIN}} = -2V \text{ load input}$$

In either case, the difference is 0.4V. This difference is called noise immunity. It represents built-in protection against noise. Protection against noise is necessary because the connecting wires between a TTL driver and load is equivalent to a small antenna that picks up stray noise signals. For eg. the figure (a) below shows a low output from the TTL driver and load is equivalent to a small antenna that picks up stray noise signals. For eg. the figure (a) below shows a low output from the TTL driver. If no noise voltage is induced on the connecting wire, the input voltage to the TTL load is 0V, as shown. In a noisy environment, however,

it is possible to have 0.4V of induced noise on the connecting wire for either the low state (fig b) or the high state (fig c). Either way, the TTL load has an input that is on the verge of being unpredictable. The slightest additional noise voltage may produce a false change in the output state of the TTL load.



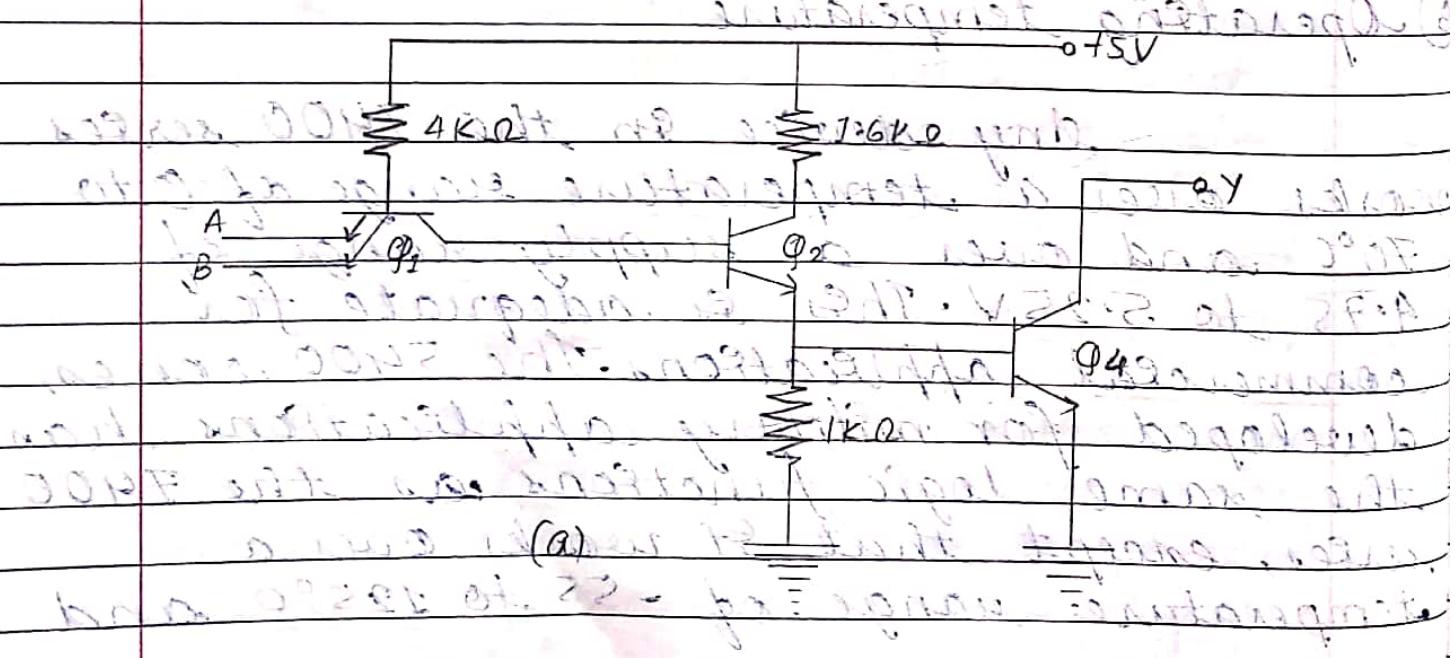
② Operating temperature

Any device in the 7400 series works over a temperature range of 0 to 70°C and over a supply range of 4.75 to 5.25V. This is adequate for commercial applications. The 5400 series, developed for military applications, has the same logic functions as the 7400 series, except that it works over a temperature range of -55 to 125°C and

over a supply range of 4.5 to 5.5 V. Although 5400 series devices can replace 7400 series devices, they are rarely used commercially because of their much higher cost.

Open-Collector Gates (Deleted) (X)

Instead of a totem-pole output, some TTL devices have an open-collector output. This means they use only the lower transistor of a totem-pole pair. The figure (a) below shows a 2-input NAND gate with an open-collector output. Because the collector of Q₄ is open, a gate like this will not work properly until you connect an external pull-up resistor as is shown in figure (b).



$+5V$

Pull-up resistor

(b)

 ϕ_4 $+5V$

Pull up

(c)



Transistor logic level



The outputs of open-collector gates can be wired together & connected to a common pull-up resistor. For instance, Fig. (c) above shows 3 TTL devices connected to the pull up resistor. This is known as Wire-OR. A connection like this has the advantage of combining the output of 3 devices without using a single OR gate. The combining is done by a direct combination of 3 outputs to the lower end of the common pull up resistor. This is very useful when many devices are wire-ORed together.

The disadvantage of open-collector gates is their slow switching speed.

Tri-state logic (Deleted) (X)

In normal logic circuits there are two states of the outputs, LOW & HIGH. If the output is not in the LOW state, it is definitely in the other state (HIGH). Similarly, if the output is not in the high state, it is definitely in the low state. In complex digital systems like microcomputers & microprocessors, a number of gate outputs may be required to be connected to a common

line which is referred to as a bus which in turn may be required to drive a number of gate inputs. When a number of gate outputs are connected to the bus, we encounter some difficulties. These are:

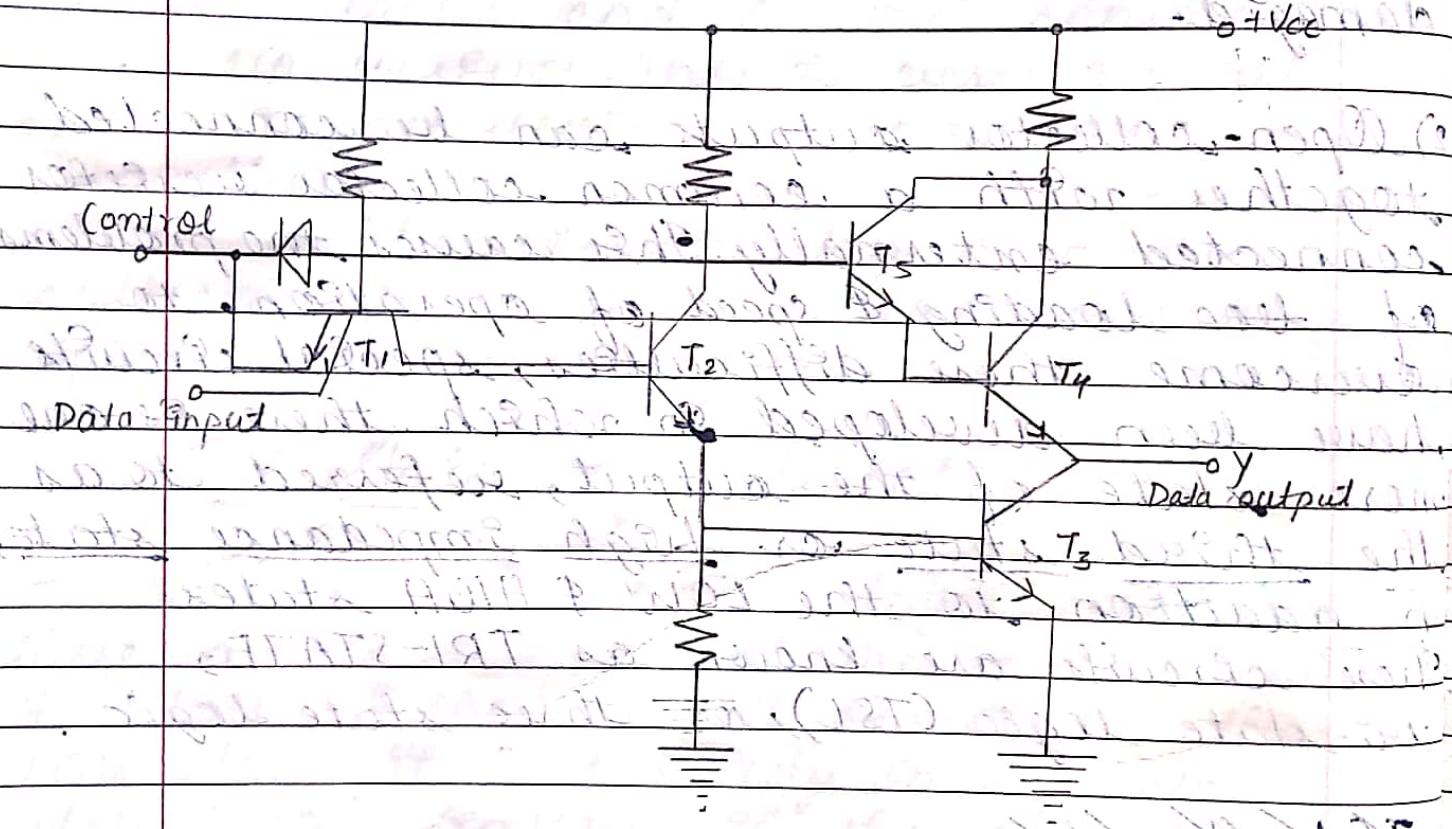
- (1) Totem-pole outputs cannot be connected together because of very large current gain drawn from the supply & consequent heating of the IC's junctions may get damaged.
- (2) Open-collector outputs can be connected together with a common collector-resistor connected externally. This causes the problems of ~~too~~ loading & speed of operation, to overcome these difficulties, special circuits have been developed in which there is one more state of the output, referred to as the third state or high impedance state, in addition to the LOW & HIGH states. These circuits are known as TRI-STATE, tri-state logic (TSL), or three state logic.

TSV Converter

TSL

Inverter

A TSL inverter circuit with tri-state output is shown below. When the control input is low (0), the drive is removed from T_3 & T_4 . Hence both T_3 & T_4 are cut off & the output is in the third state. When the control input is high, the output is logic 0 or 1 depending on the data input.



Working:

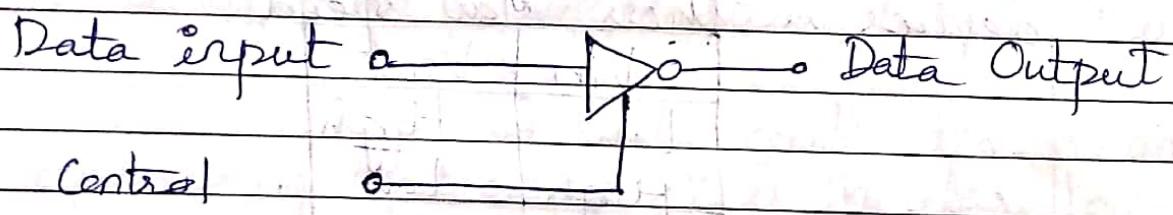
If the control or enable input is low, T_1 conducts cutting off T_2 and hence T_3 . The base of T_5 is also grounded through the diode and hence T_5 is also turned off. With T_5 off, T_4 is cut off. This low control input has thus created a high impedance path from the output terminal.

to $+V_{cc}$ as well as to the ground. This means that the output terminal is isolated and in effect, the TTL gate is disconnected from V_{cc} . The input has no control over V_{cc} .

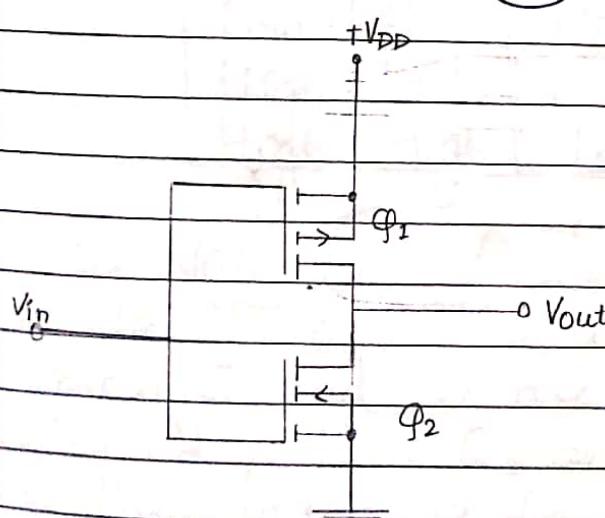
A high control or enable input allows the normal NOT operation of the TTL gate.

The output V_{cc} of this TTL gate now has 3 outputs states: 1, 0 and isolates i.e. OFF. The truth table of a TSL inverter, along with its symbol is shown below.

Data Input	Control	Data Output
0	0	High-Z
1	0	High-Z
0	1	1
1	1	0



CMOS inverter: ~~(X) Deleted~~



Q_1 is p-channel MOSFET and Q_2 is an n-channel device. They form a push-pull arrangement and hence when one device is on, the other is off.

P-channel MOSFET is connected as a load in series with n-channel to form a complimentary pair known as CMOS inverter.

Working:

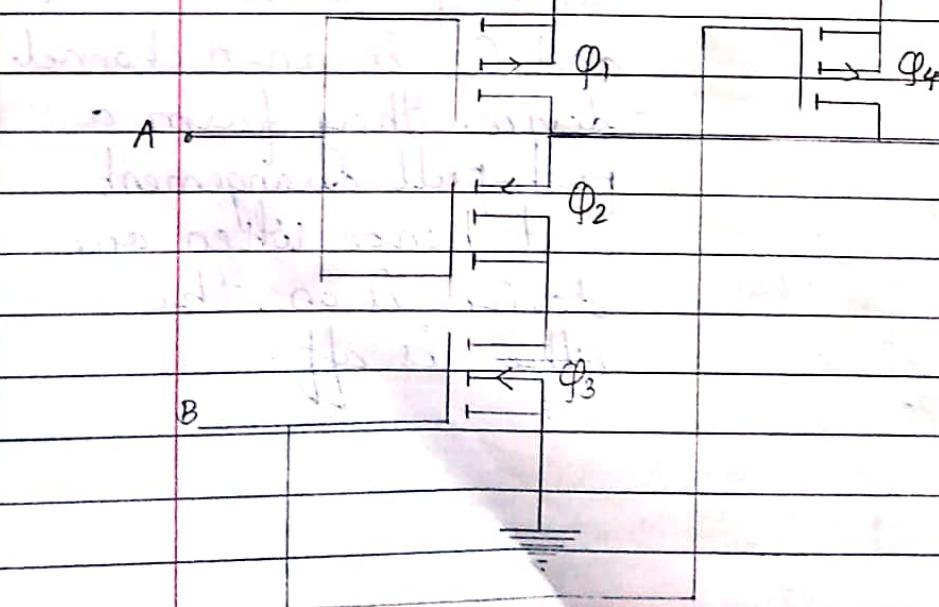
When $V_{in} = 0$, Q_2 is off but Q_1 is on. This means the output voltage is high. On the other hand, when $V_{in} = 10$ ie high, Q_2 is on and Q_1 is off. In this case, output voltage is low.

Current through the circuit is very small equal to leakage current in nF because one transistor is on and the other OFF. Power consumption is therefore very small in nW. This is its advantage. Drawback of CMOS devices is their slow speed.

V_{in}	V_{out}
Low	High
High	Low

(X) Deleted

CMOS NAND



The figure shows CMOS NAND gate. Q_1 and Q_2 form one complimentary connection; Q_3 and Q_4 form another. The output is pulled upto the supply voltage when either Q_1 and Q_4 is conducting. The output is pulled down to ground only when Q_2 and Q_3 are conducting.

Working:

(i) A is low, B is low. Since A is low, Q_1 is conducting and Q_2 is off. With B low, Q_4 is on and Q_3 off. Q_1 and Q_4 conducts and output Y is therefore high.

(ii) A low, and B high. For this combination, Q_1 is conducting but Q_4 is off. Output Y is hence high.

(iii) A high, B low. For this combination; Q_1 and Q_3 are off and Q_2 , Q_4 conducts. Output Y is high since Q_4 is conducting.

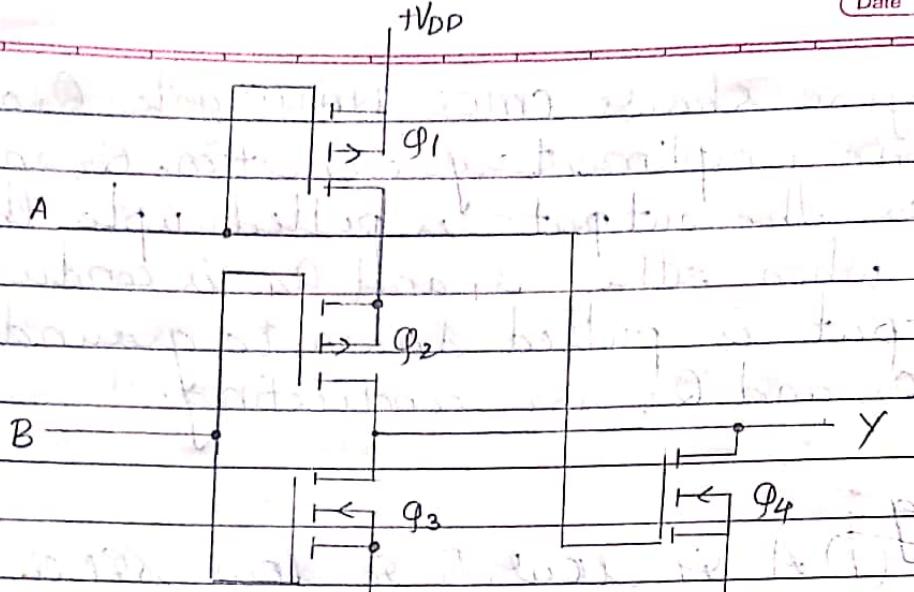
(iv) A high, B high. For this combination Q_2 and Q_3 are conducting and output Y is therefore low.

A	B	Y
Low	Low	High
Low	High	High
High	Low	High
High	High	Low

CMOS NOR ~~Deleted~~

In the above CMOS circuit, the output goes high only when Q_1 and Q_4 are conducting. The output goes low, if either Q_2 or Q_3 are conducting. There are the following four cases.

(i) A low, B low, for both inputs low, Q_1 and Q_2 are conducting, Q_3 and Q_4 are cut off.

$+V_{DD}$ 

Q₁ will be off if A is low and Q₂ has no voltage. If A is high, Q₁ has an input current which is high. Since Q₁ is on, Q₂ has an input current which is high. Therefore, output Y is high.

(iv) At low A, B high & far there Q₁, Q₃ conduct. Q₂, Q₄ cuts off. Since Q₃ conducts, output Y is low.

(v) At high B, low A. For this Q₁, Q₂ conduct and Q₃, Q₄ cuts off. With Q₁ now conducting, output Y is low.

(vi) At high A, high B both Q₃ and Q₄ conduct and output Y is low.

A	B	Y
low	low	high
low	high	low. (X)
high	low	low
high	high	low

Q₁ and Q₂ are off at A low and B high.

Q₃ and Q₄ are on at A high and B low.