**NAME:** Adwait S Purao

**UID:** 2021300101

**Batch**:B2

**Experiment no.:**3

**AIM:**

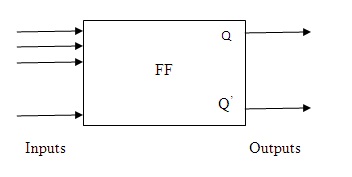
To design and implement gate level and MSI circuits of flip-flops.

**SOFTWARE REQUIRED**:

PROTEUS 8.6 Professional

**THEORY:**

***Introduction to flip-flops***:



The term "flip-flop" relates to the actual operation of the device, as it can be "flipped" to a logic set state or "flopped" back to the opposing logic reset state.

A flip-flop can be regarded as a memory storage device. It is used to store a binary digit .The two outputs of a flip-flop are Q and Q’ where Q is the complementary of Q’.A flip-flop is a bistable electronic circuit. If one stable state is Q=0,Q’=1 the other state is Q=1,Q’=0.The flip-flop has the ability to stay in one of the two possible states, after an input has been applied. Since the state does not change after the removal of input, the flip-flop is essentially a 1 bit memory storage device. When the flip-flop has it’s Q =0 its storing binary 0, when Q=1 it’s storing binary 1.

***Types of Flip-Flops***:

1. SR flip-flop

2. JK flip-flop

3. D flip-flop

4. T flip-flop

***APPLICATONS OF FLIP-FLOPS:***

* Counters
* Frequency dividers
* Shift Registers
* Storage Registers
* Bounce elimination switch
* Data Storage
* Data Transfer
* Latch
* Registers
* Memory

**PROCEDURE:**

1. Open Proteus, click on create new project.

2. In the third column from the left, click on the P icon on the top left .

3. Type required IC no. or gate and select it and click ok and it would appear in the list.

4. In the same way bring Logic probe and Logic toggle to the list.

5. Click on the generator icon on the leftmost bar and then click on D CLOCK and it would come to the list.

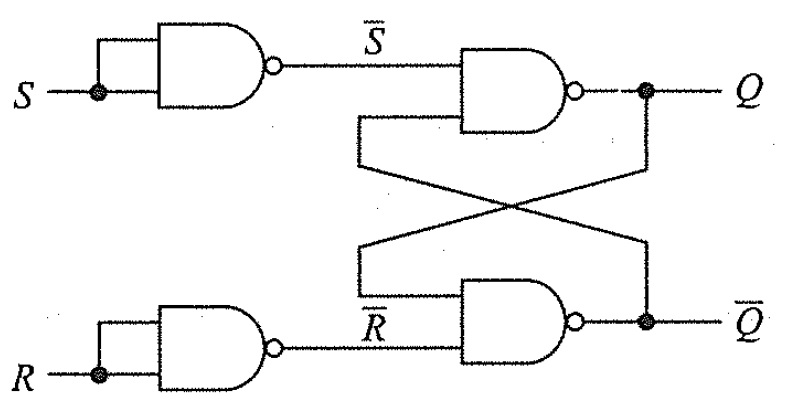
6. Make connections as shown in figures.

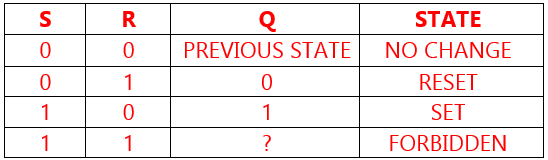
7. Click on the play icon and run the simulation.

**SR flip-flop:**

The SR flip flop stands for "Set-Reset" flip flop. The SR flip flop is a 1-bit memory bistable device having two inputs, i.e., SET and RESET. The SET input 'S' set the device or produce the output 1, and the RESET input 'R' reset the device or produce the output 0. The SET and RESET inputs are labeled as **S** and **R**, respectively. SR flip flop is a basic flip flop which provides feedback from both of its outputs back to its opposing input.

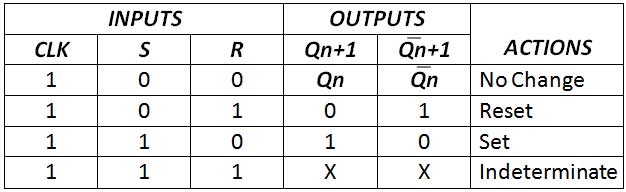
***Basic SR flip-flop***



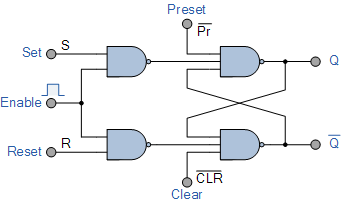


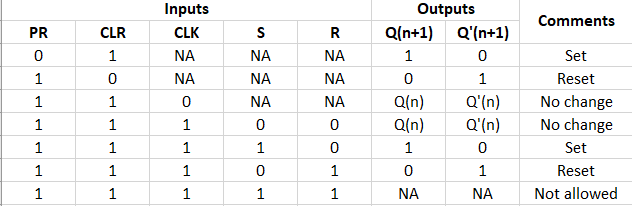
***Clocked SR flip-flop***





***Preset-Clear SR flip-flop***





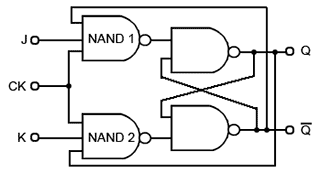
**JK Flip-flop:**

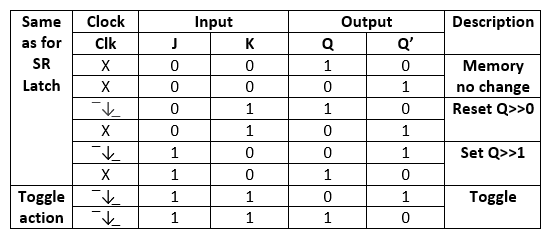
The [JK flip flop](https://www.javatpoint.com/jk-flip-flop-in-digital-electronics) is one of the most used flip flops in digital circuits. The JK flip flop is a universal flip flop having two inputs 'J' and 'K'. In SR flip flop, the 'S' and 'R' are the shortened abbreviated letters for Set and Reset, but J and K are not. The J and K are themselves autonomous letters which are chosen to distinguish the flip flop design from other types.

The JK flip flop work in the same way as the SR flip flop work. The JK flip flop has 'J' and 'K' flip flop instead of 'S' and 'R'. The only difference between JK flip flop and SR flip flop is that when both inputs of SR flip flop is set to 1, the circuit produces the invalid states as outputs, but in case of JK flip flop, there are no invalid states even if both 'J' and 'K' flip flops are set to 1.

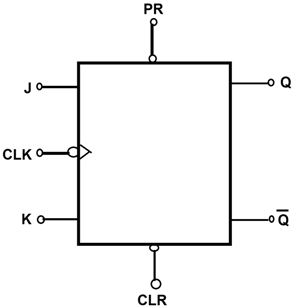
The JK Flip Flop is a gated SR flip-flop having the addition of a clock input circuitry. The invalid or illegal output condition occurs when both of the inputs are set to 1 and are prevented by the addition of a clock input circuit. So, the JK flip-flop has four possible input combinations, i.e., 1, 0, "no change" and "toggle".

***JK Flip-flop using gates***





***JK flip-flop using IC***

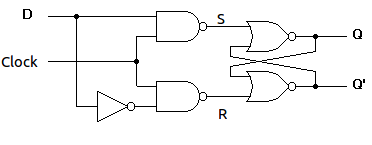


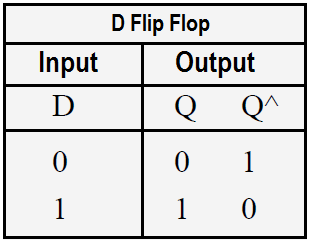
Truth table is same as previous JK flip-flop

***D Flip-flop***

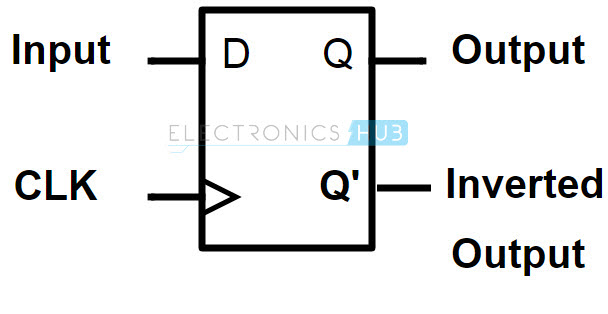
A D (or Delay) Flip Flop (Figure 1) is a digital electronic circuit used to delay the change of state of its output signal (Q) until the next rising edge of a clock timing input signal occurs. The **D Flip Flop** is by far the most important of all the clocked flip-flops. By adding an inverter (NOT gate) between the Set and Reset inputs, the S and R inputs become complements of each other ensuring that the two inputs S and R are never equal (0 or 1) to each other at the same time allowing us to control the toggle action of the flip-flop using one single D (Data) input.

Then this Data input, labelled “D” and is used in place of the “Set” signal, and the inverter is used to generate the complementary “Reset” input thereby making a level-sensitive D-type flip-flop from a level-sensitive SR-latch as now S = D and R = not D as shown.





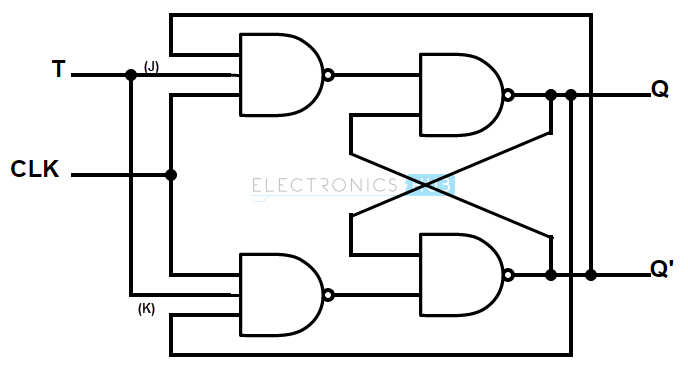
***DTFF***



Truth table same as D flip-flop

***T Flip-flop***

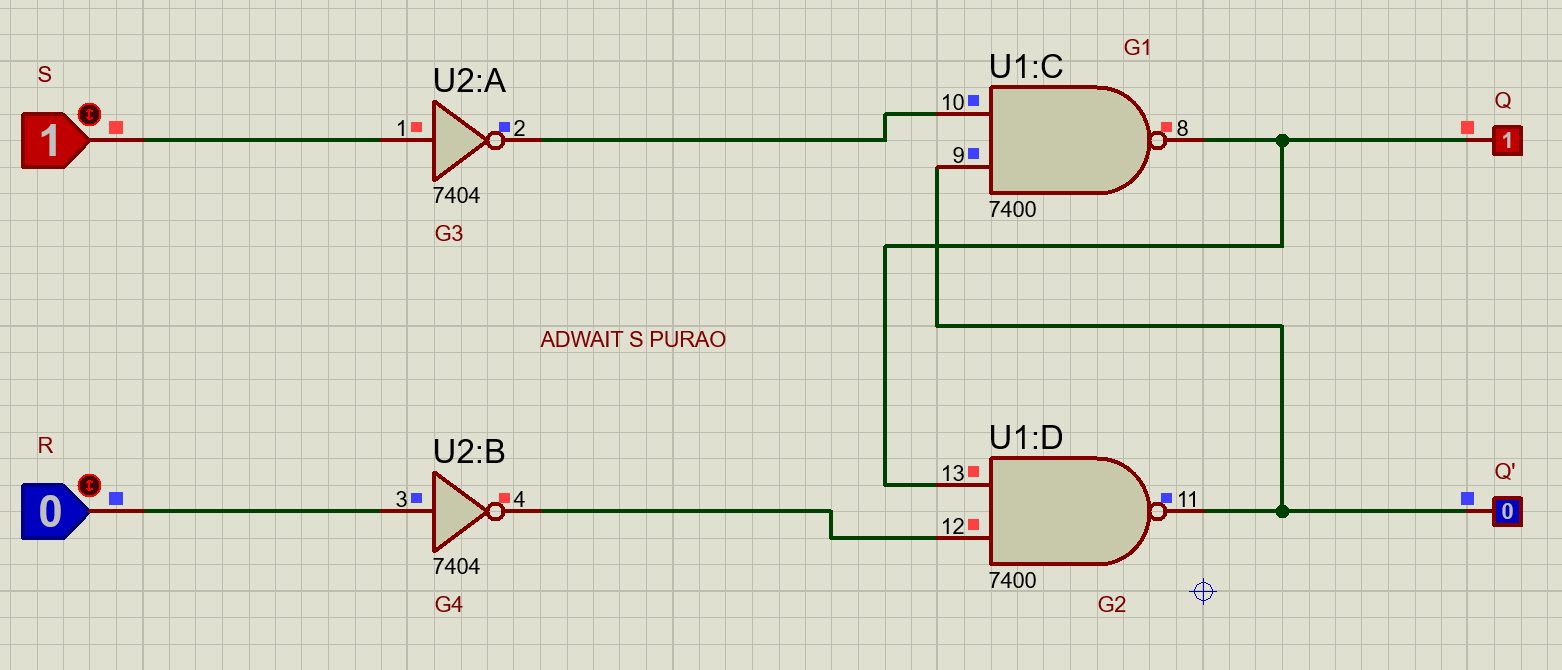
In T flip flop, "T" defines the term "Toggle". In [SR Flip Flop](https://www.javatpoint.com/sr-flip-flop-in-digital-electronics), we provide only a single input called "Toggle" or "Trigger" input to avoid an intermediate state occurrence. Now, this flip-flop work as a Toggle switch. The next output state is changed with the complement of the present state output. This process is known as "Toggling"'. The "T Flip Flop" is toggled when the set and reset inputs alternatively changed by the incoming trigger. The "T Flip Flop" requires two triggers to complete a full cycle of the output waveform. The frequency of the output produced by the "T Flip Flop" is half of the input frequency.





* **Results and observations**:

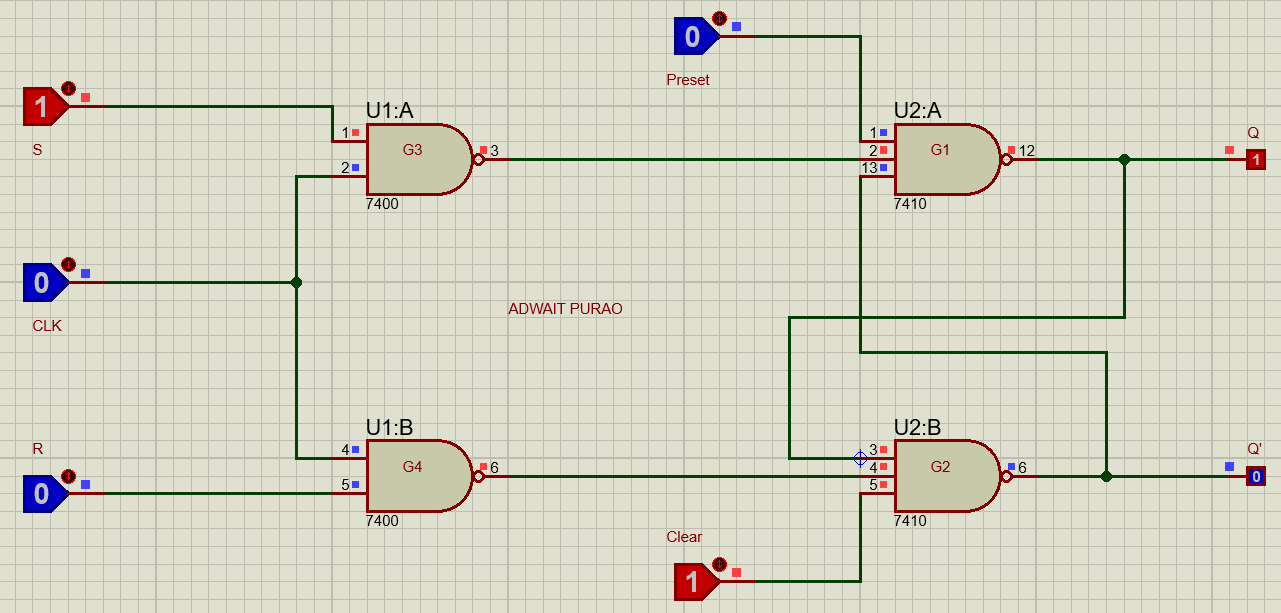
***Basic SR flip-flop***

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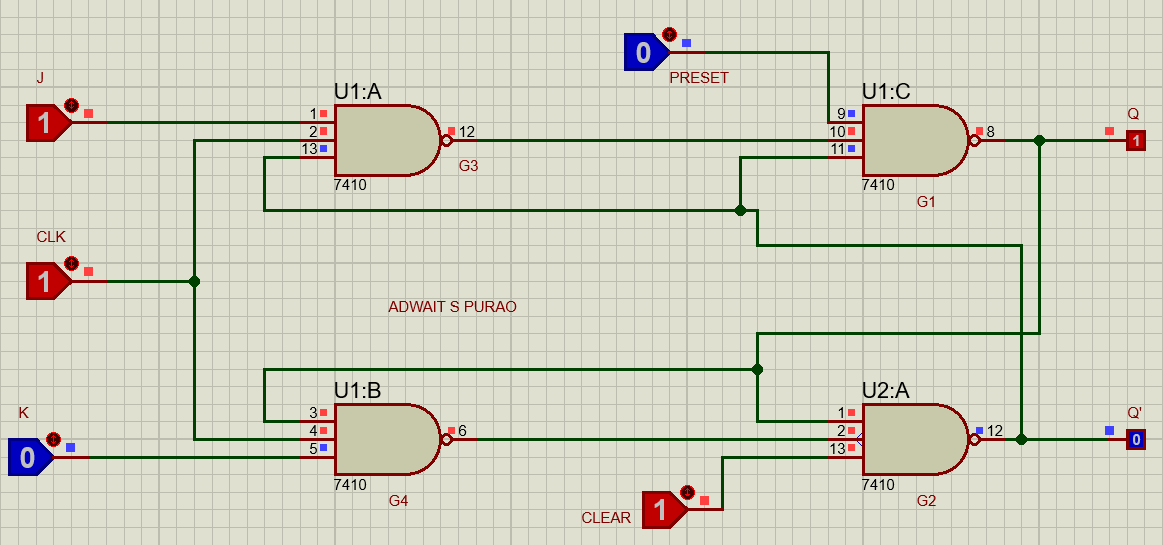
***Clocked SR flip-flop***

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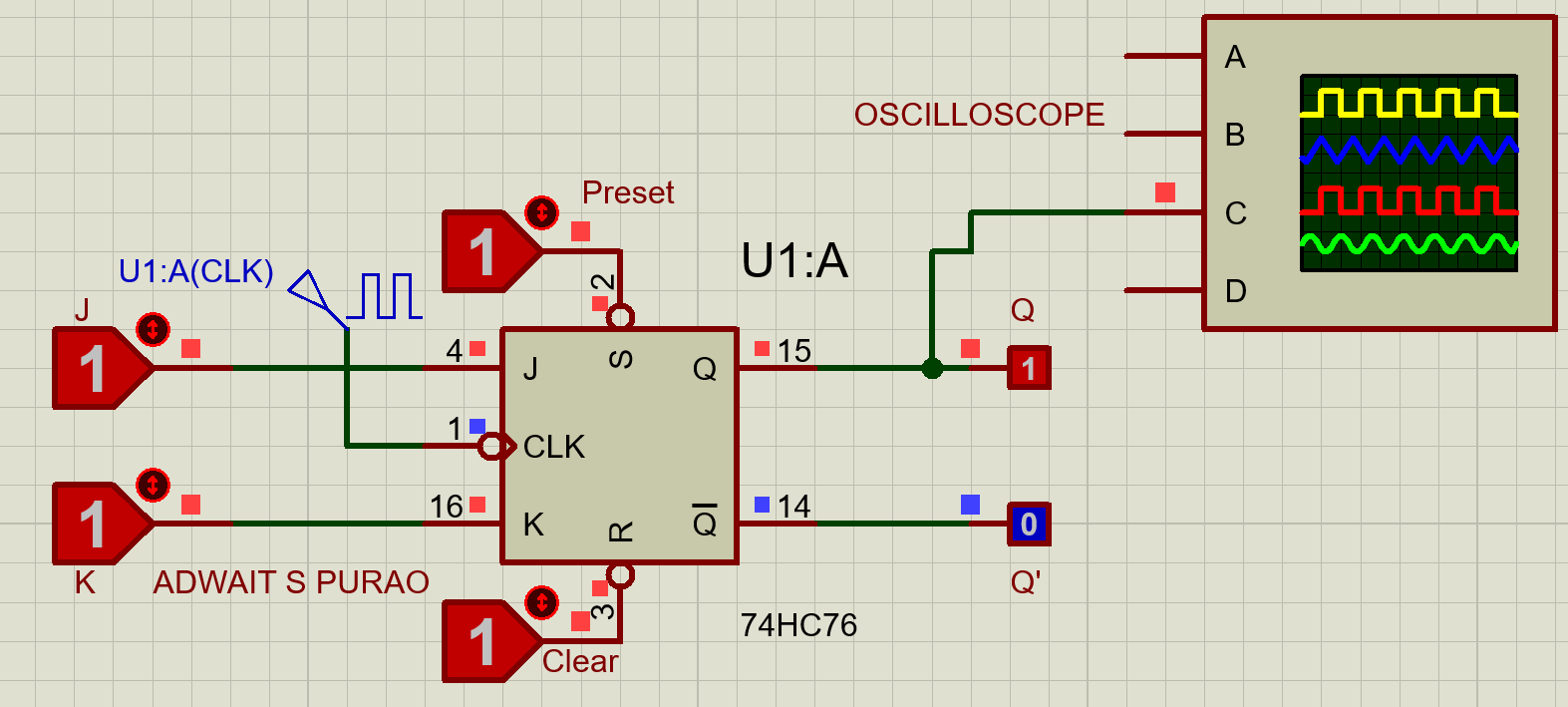
***Preset-Clear SR flip-flop***

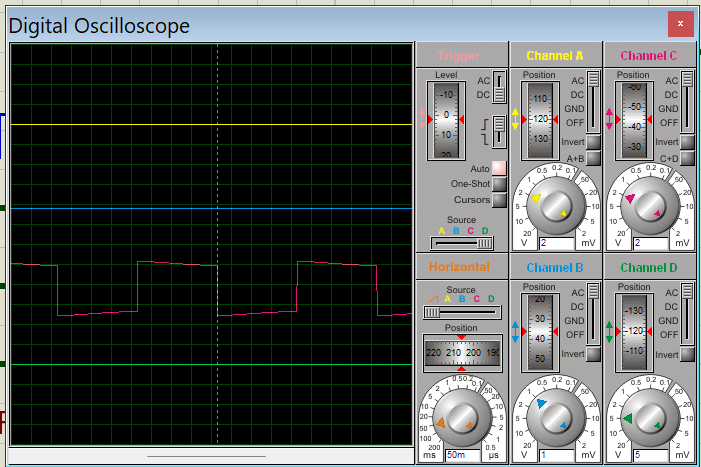
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* ***JK Flip-flop using gates***

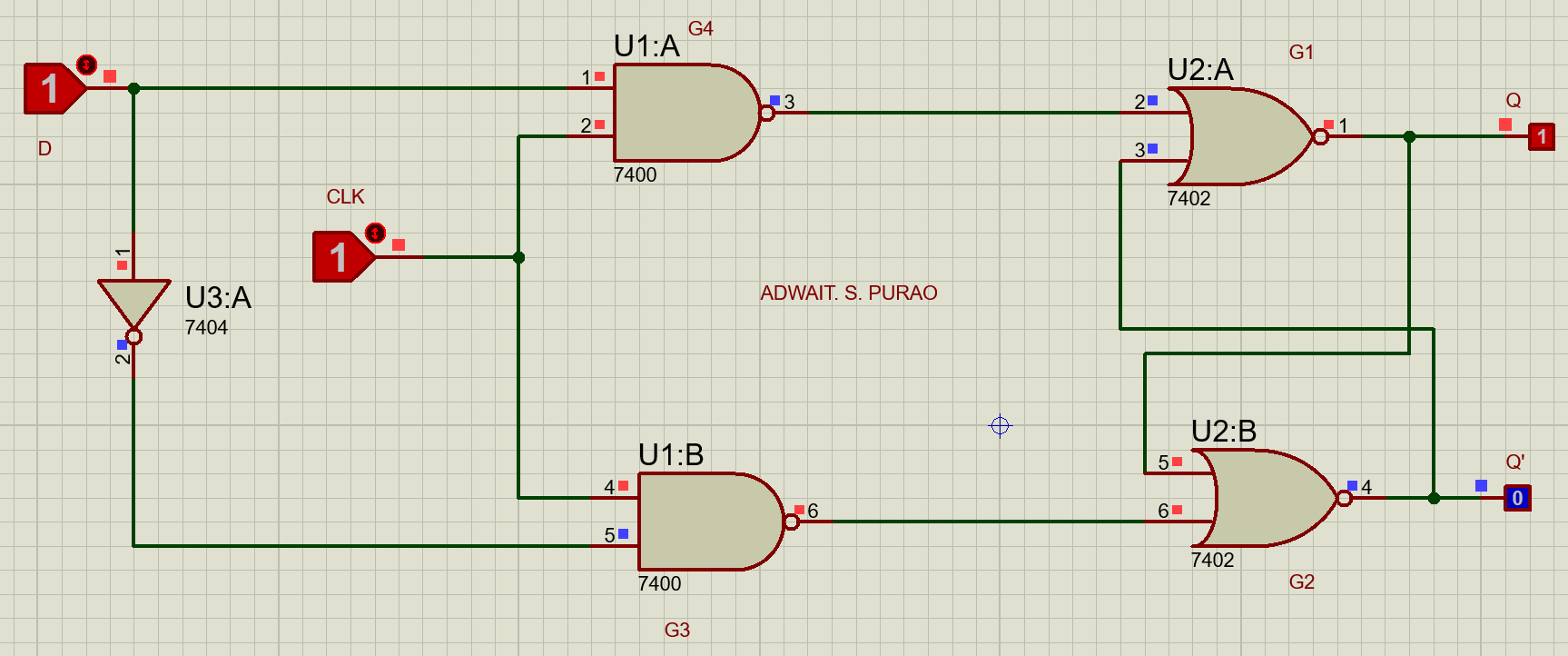
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* ***JK flip-flop using IC 74HC76***

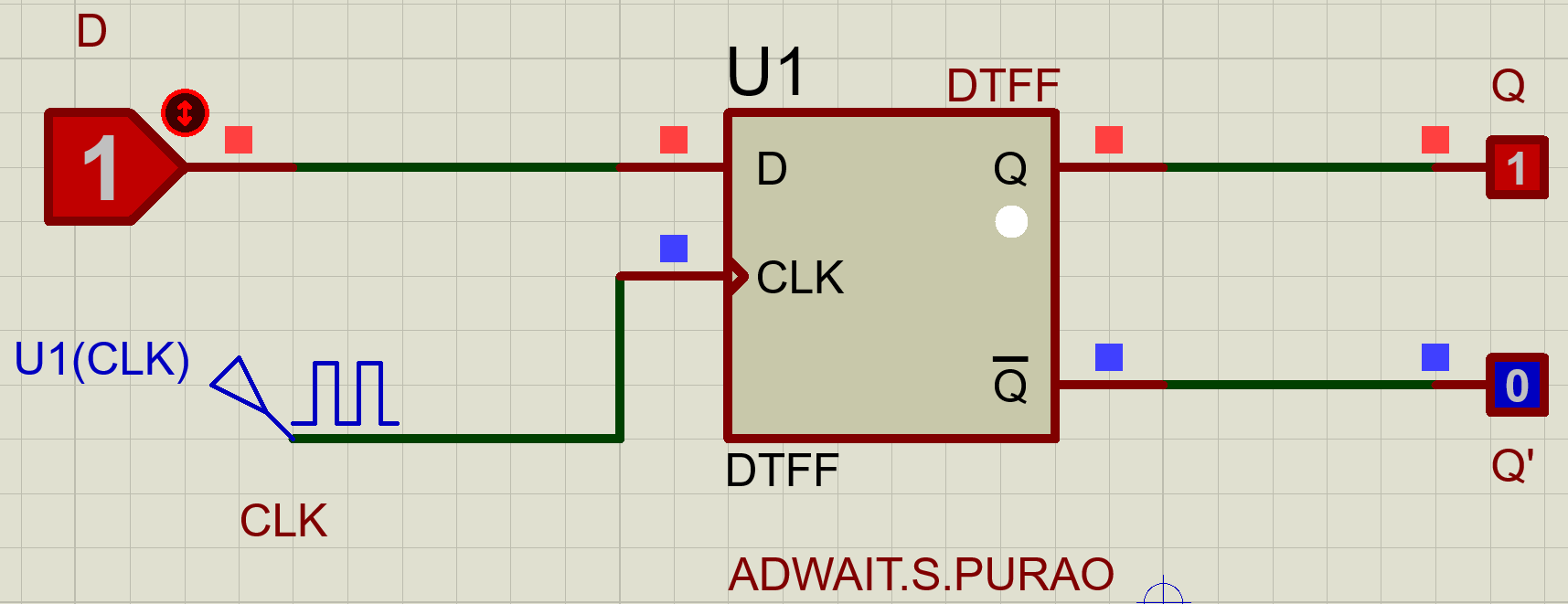
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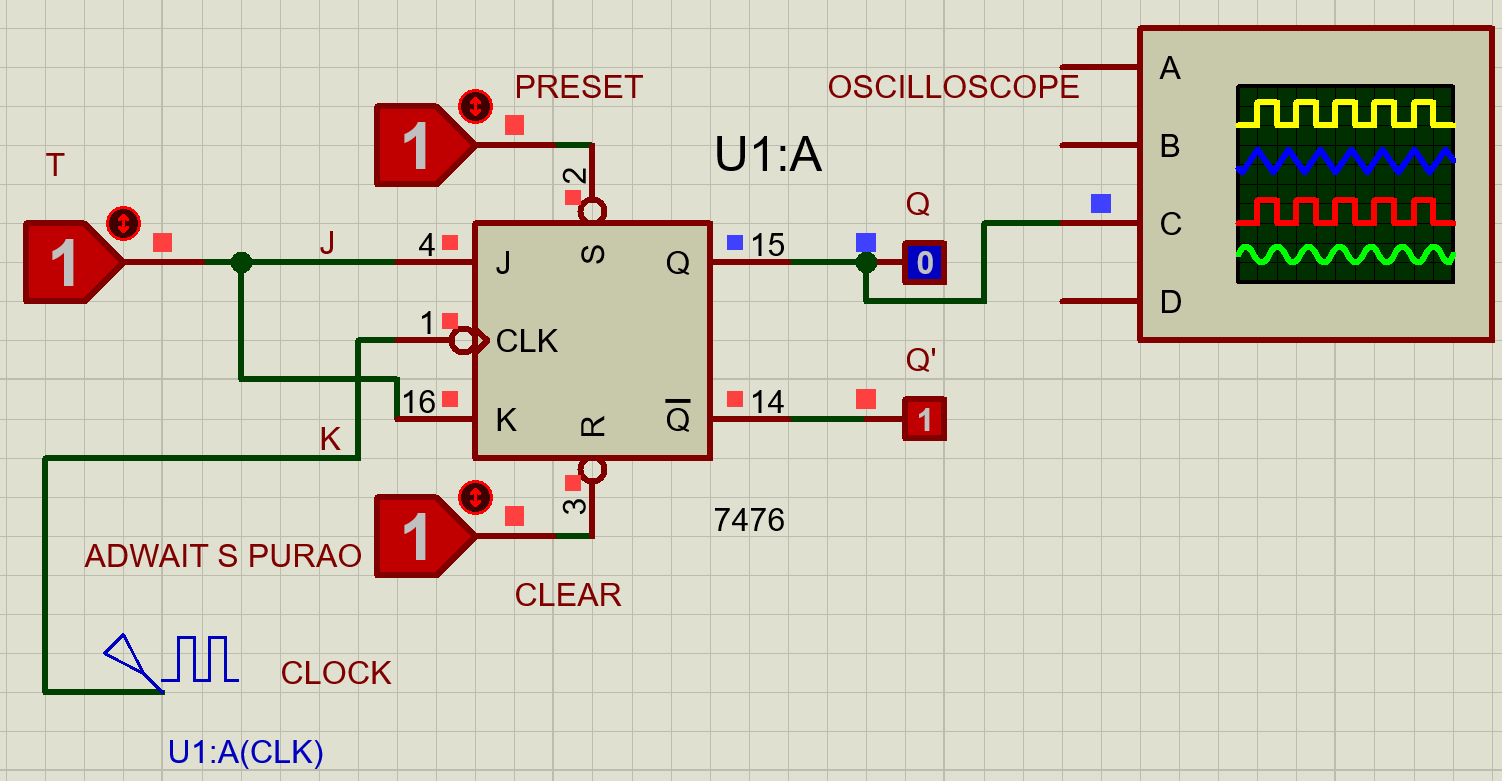
* ***D Flip-flop***

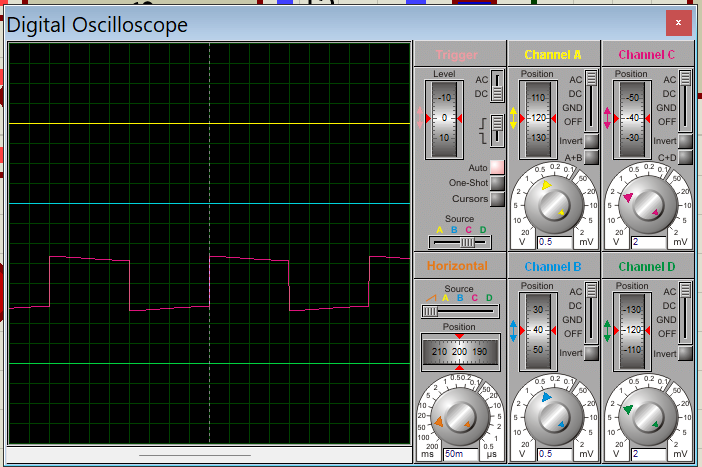
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* ***DTFF***

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* ***T Flip-flop***

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**CONCLUSION:**

