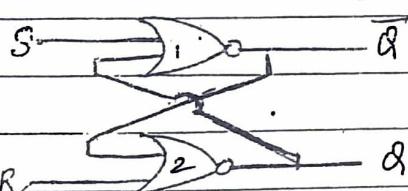


FF

①

Flipflops

A FF can be regarded as a memory device. It is used to store a binary digit. The two outputs of the FF are Q and \bar{Q} , where \bar{Q} is the complement of Q . A FF is a bistable electronic circuit ie it has two stable states. If one stable state is $Q=0, \bar{Q}=1$, the other stable state is $Q=1, \bar{Q}=0$. The FF has the ability to stay in one of the 2 possible states after an input has been applied. Since the state does not change following the removal of the input, the FF is essentially a 1-bit memory or storage device. When the FF has its Q output equal to 0, we can regard it as storing the binary 0 and when the Q output = 1, it is said to store the binary 1.

Simple RS FF using NOR :-

For an RS-FF, there are 2 input terminals SET (S), RESET (R) and two output terminals Q , \bar{Q} .

In the given circuit, the output of one NOR gate serves as one of the inputs to the other NOR gate.

Suppose the inputs to the FF are $S=1, R=0$. One input to NOR-1 is high and hence its output goes low. For NOR-2, both inputs are low, giving output high. ie $Q=1, \bar{Q}=0$.

A '1' at the set input, SETS the flip flop ie makes $Q=1$. With the flip flop in the state $Q=1, \bar{Q}=0$, suppose we make $S=0, R=0$. Inputs to NOR-1 are 0 and 1, giving output $\bar{Q}=0$. For NOR-2, inputs are both 0, giving $Q=1$.

i.e no change in the output is obtained for $S=0, R=0$. The FF simply remains in its previous state.

Suppose $S=0, R=1$. One input to NOR-2 is high and

2

hence output of NOR-2 goes low. Both inputs are therefore low for NOR-1 and its output goes high, ie $Q=0, \bar{Q}=1$. Thus a '1' at the RESET input, RESETS the FF ie makes $Q=0$.

Suppose $S=R=1$. The outputs of both the gates will try to go to the low state. In other words, both Q and \bar{Q} equal 0 at the same time. But this is against the basic definition of a FF that requires Q to be the complement of \bar{Q} . So it is generally agreed never to impose this input condition ie FORBIDDEN.

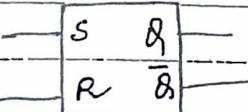
$S \ R \ Q \ \bar{Q}$

0 0 No change

0 1 0 1

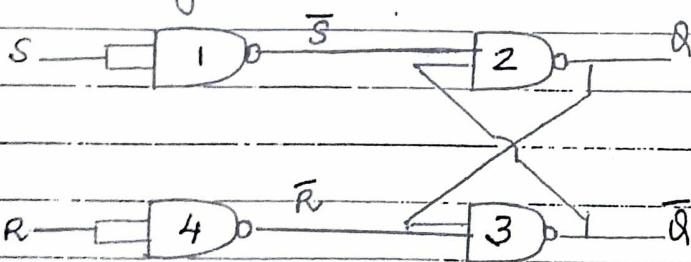
1 0 1 0

1 1 Forbidden



Symbol

RS FF using NAND



NANDs 1 and 4
are used as
inverters

The inputs to the
FF are S and R ,

outputs are Q and \bar{Q} .

Suppose the inputs are $S=1, R=0$, i.e. $\bar{S}=0, \bar{R}=1$.

One input to NAND-2 is 0 and hence its output ie Q becomes 1. Now all inputs to NAND-3 are 1, giving output $\bar{Q}=0$. Hence a '1' at the S input SETS the flip-flop ie gives $Q=1, \bar{Q}=0$.

Suppose the inputs are $S=0, R=0$, ie $\bar{S}=1, \bar{R}=1$.

3 (2)

Inputs to NAND-2 are 1 and 0 giving output $Q = 1$.

Inputs to NAND-3 are both 1, giving output $\bar{Q} = 0$.

i.e. $S=R=0$ results in no change in FF output.

Let $S=0, R=1$. Then $\bar{S}=1, \bar{R}=0$. One input to NAND-3 is 0 and hence output \bar{Q} becomes 1.

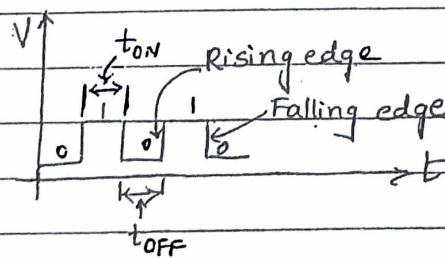
Both inputs to NAND-2 are 1, giving output $Q=0$.

For $S=0, R=1$, FF RESETS i.e. $Q=0, \bar{Q}=1$.

Let $S=R=1$. Then $\bar{S}=\bar{R}=0$. One input to both NAND-2 and NAND-3 is 0, giving both Q and \bar{Q} equal to 1 at the same time. But this is against the basic definition of a FF that requires Q to be the complement of \bar{Q} . So we never use the condition $S=R=1$.

Truth table	S	R	Q	\bar{Q}
	0	0	No change	
	0	1	0	1
	1	0	1	0
	1	1	Forbidden.	

Clock signals : A clock in a digital circuit is a square wave as shown below. Very often, clock is symmetrical i.e. $t_{on}=t_{off}$. The 0 to 1

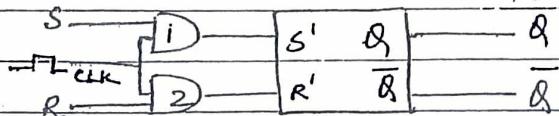


transition is called the rising edge or positive going edge while the 1 to 0 transition is called the falling edge or negative going

edge transition. Suppose a circuit contains a number of FFs. In order that all the FFs change state at the same time, a clock signal is fed at the input of each FF. When the

clock is low, the FFs do not change state. But when the clock goes high, all the FFs change state. Thus a clock is used for synchronizing different actions taking place in a digital circuit.

Clocked RS FF



The construction of a clocked RS FF is shown above.

In the above figure, the S and R inputs are connected to the set s' and reset R' inputs of a simple RS FF through 2 AND gates.

Suppose $S=1$, $R=0$. As long as the clock input is low, the outputs of both the AND gates will be low and there will be no change in the output of the FF. But when the clock goes high, output of AND1 ie s' becomes high and output of AND2 ie R' becomes low. For the input combination $s'=1$, $R'=0$, FF SETS.

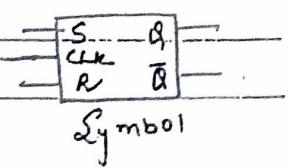
Let $S=0$, $R=0$. When clock goes high, outputs of both the AND gates are low ie $s'=R'=0$. This results in no change in FF condition ie FF remains in previous stable state.

Let $S=0$, $R=1$. With clock high, output of AND-2 becomes high and output of AND-1 is low. ie $s'=0$, $R'=1$, which results in RESET condition of FF, ie $Q=0$, $\bar{Q}=1$.

With $S=R=1$ and clock high, both s' and R' are high. This is the forbidden condition of the FF.

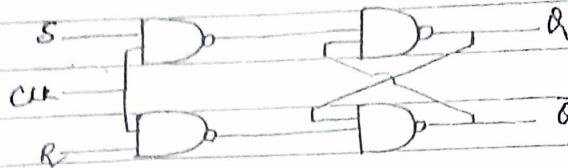
Truth table :

S	R	CLK	Q	\bar{Q}
0	1	1	0	1
0	0	1	No change	
1	0	1	1	0
1	1	1	Forbidden	

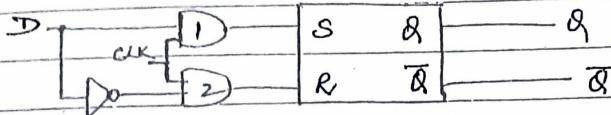


(3)

Clocked RS FF circuit using only NAND



Clocked J FF



Introducing an inverter on one of the input lines of a clocked RS FF, we have a J FF which requires only one input J , excluding clock. This inverter avoids the forbidden condition ($R=S=1$).

With $J=0$, if clock is low, both the AND gates produce low output. For $S=R=0$, FF retains its previous stable state. However, when clock is high, output of AND-1 is low and D output of AND-2 is high.

i.e. $S=0, R=1$. This results in the RESET condition of FF.
($Q=0, \bar{Q}=1$)

With $J=1$, clock high, output of AND-1 i.e. $S=1$ and output of AND-2 i.e. $R=0$. This combination SETS the FF ($Q=1, \bar{Q}=0$)

Truth table

D	clk	Q	\bar{Q}	D	Q
				clk	\bar{Q}
0	1	0	1		
1	1	1	0		

Symbol.

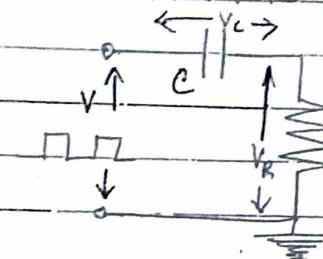
Level Clocked and Edge Triggered FFs :

FFs that change state on the positive going edge or the negative going edge of a clock signal are called edge triggered FFs. When the FF is triggered on the positive

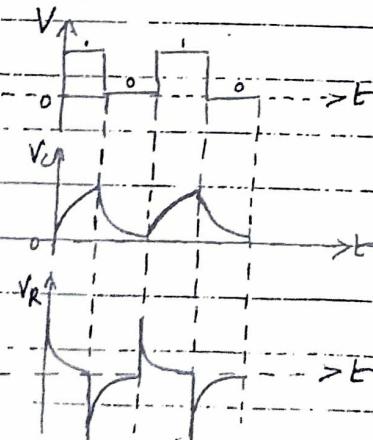
going edge of the clock, it is called a positively edge triggered FF and if the FF is triggered on the negative going edge of the clock, it is called a negatively edge triggered FF.

FFs that respond to the level of the clock, high or low are called level clocked FFs. When a circuit is level clocked, the output can change while the clock is high. With edge triggering, the output can change only on the rising or falling edge of the clock.

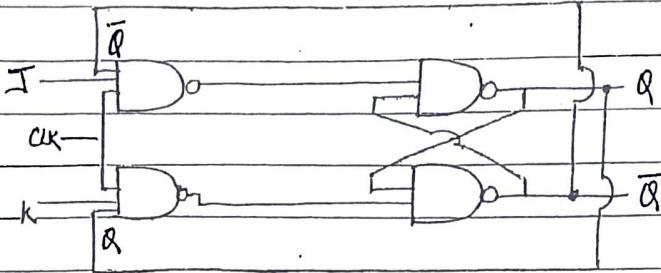
For constructing a edge-triggered FF, one has to introduce a differentiator network at the clock input of the FF. This network is shown below. When a



clock pulse is differentiated by a differentiating circuit, the horizontal parts of the clock are removed and only fast rising and falling spikes are created. The input and output waveforms of the circuit are shown below. The square wave is converted into positive and negative spikes, with a positive spike generated for a 0 to 1 transition and a negative spike for a 1 to 0 transition of the clock.



JK FF using NAND only

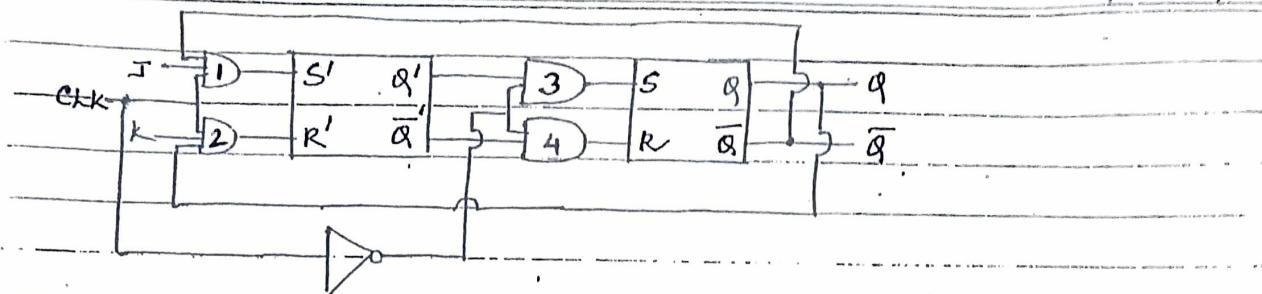


Race-around condition

This is a disadvantage of a JK FF. Consider a JK FF which is level clocked. For the input $J=K=1$, when the ^{1st clock pulse arrives and} clock goes high, suppose FF is SET. When the new Q and \bar{Q} outputs arrive at the inputs of the 2 AND gates, if the 1st clock pulse has not ended and clock is still high, FF will now get RESET. Hence we find that for the duration of the pulse i.e. for $clk=1$, the output oscillates between 0 and 1. At the end of the pulse ($clk=0$) the value of Q is uncertain. This is called a 'race-around' condition.

To avoid this race-around condition, JK FFs are never level clocked. We edge trigger a JK FF. Other FFs are either level clocked or edge triggered depending on their applications.

Master-Slave JK FF: - A circuit to avoid the race-around condition is called a JK Master-Slave FF. The figure below shows a cascade of 2 RS FFs with feedback from the output of the second (called the slave) to the input of the first (called the master). Suppose the FF is in the RESET state.



For the input $J=1, K=0$ and $CK=1$, the master toggles into the SET state i.e. $Q'=1, \bar{Q}'=0$. Nothing happens to the Q and \bar{Q} outputs (MS JK FF outputs) because the slave is inactive when clock is high. When clock goes low however, the slave is SET.

For the input $J=0, K=1$, master RESETS when clock is high. No changes occur in Q and \bar{Q} because slave is inactive then. However, when clock goes low, slave becomes active and RESETS.

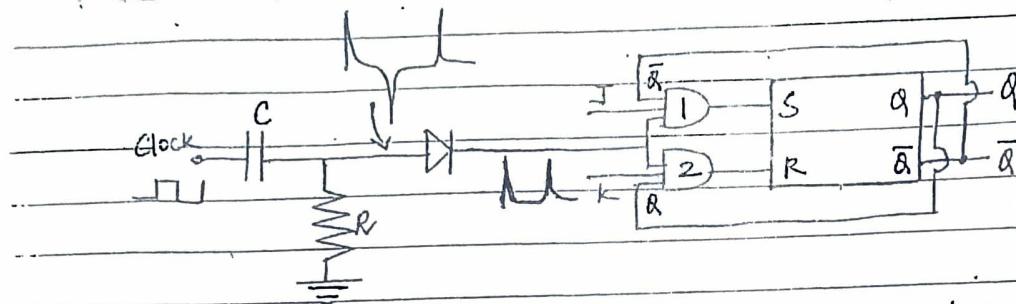
If $J=K=1$, the master toggles once while the clock is high and the slave then toggles once when the clock goes low. No matter what the master does, the slave copies it. If master toggles into the SET state when clock is high, slave also toggles into the SET state ^{but} when the clock goes low.

$J=K=0$ and clock high, does not change the master output. So, when clock is low, slave also does not change state.

J	K	CK	Q	\bar{Q}
0	0	1	No change	
0	1	1	0	1
1	0	1	1	0
1	1	1	Toggle.	

Edge triggered JK FF

(4)



Given above is a positively edge triggered JK FF. This FF triggers only when the clock makes a 0 to 1 transition. For every rising edge of a clock pulse a positive spike arrives at the clock input terminal of the FF. This FF is a modification of a clocked RS FF. The outputs Q and \bar{Q} are cross connected to the input of AND-2 and AND-1 respectively.

Suppose the FF is in the stable state $Q=0, \bar{Q}=1$. Let $J=1, K=0$. When the clock goes high, AND 1 has all its inputs high, whereas AND-2 has 2 inputs low. This results in $S=1, R=0$, which SETS the FF. ie gives $Q=1, \bar{Q}=0$.

With the FF now in the state $Q=1, \bar{Q}=0$, suppose J and K inputs are changed to 0 and 1 respectively. When clock goes high, AND 2 has all its inputs high while AND 1 has 2 inputs low. \therefore AND 2 output $R=1$ and AND 1 output $S=0$. This RESETS the FF. ie FF is switched to the stable state $Q=0, \bar{Q}=1$.

Suppose $J=K=0$. Both the AND gates are disabled even when clock goes high for this input combination.

$\therefore S=R=0$ and no change is observed in the FF outputs.

Suppose the FF is in the SET state and we make $J=K=1$. When the 1st clock pulse arrives and makes a 0 to 1 transition, AND 2 is enabled while

AND-1 is disabled. This gives $S=0$, $R=1$ and the FF RESETS. Now, with the FF RESET, for the 2nd clock pulse, AND-1 is enabled and AND-2 is disabled. $S=1$, $R=0$ and the FF SETS. Thus the FF continuously switches from one stable state to other, for every clock pulse arriving at its clock input i.e. the FF toggles and this condition is referred to as the TOGGLE condition of a JK FF.

Truth table

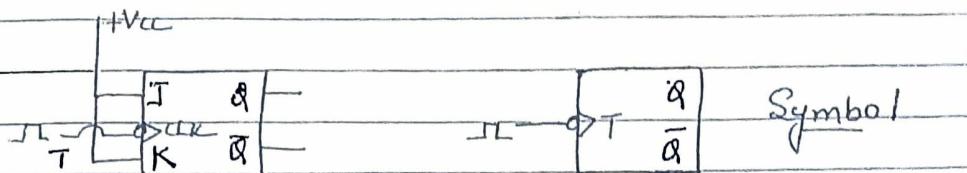
J	K	CLK	Q	\bar{Q}	
0	0	↑	No change		J Q
0	1	↑	0	1	\rightarrow CLK
1	0	↑	1	0	K \bar{Q}
1	1	↑	Toggle		Symbol

Note: For a negatively edge triggered FF, introduce a inverter (after the differentiator network), followed by a diode. In this case, FF triggers for a negative transition of the clock, a positive spike arrives at the clock terminal and triggers the FF. Truth table and symbol of a negatively edge triggered JK FF is shown below.

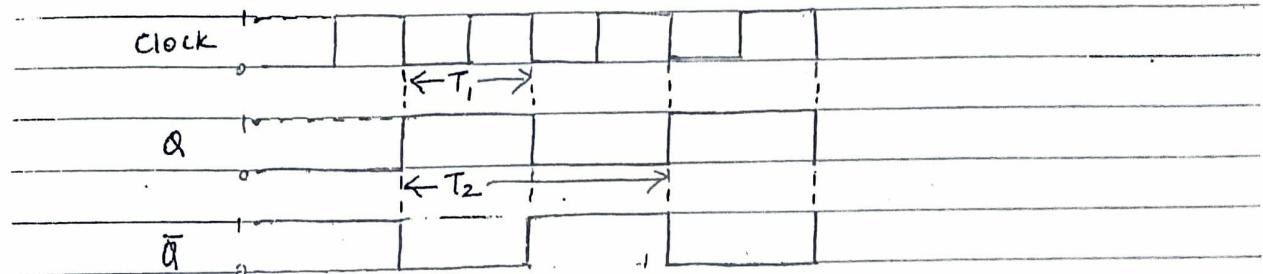
J	K	CLK	Q	\bar{Q}	
0	0	↓	No change		J Q
0	1	↓	0	1	\rightarrow CLK
1	0	↓	1	0	K \bar{Q}
1	1	↓	Toggle		Symbol

T FF :- (Toggle FF)

This FF has connections similar to the JK FF except that T and K inputs are both maintained high. The ff has only one active input ie the clock input (T).

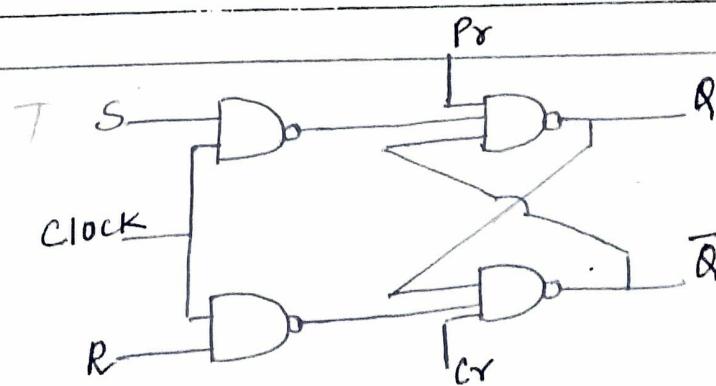


A T FF is an edge-triggered FF. If it is an negatively edge triggered FF, then the output will change state whenever the clock makes a 1 to 0 transition. Suppose the FF is in the stable state $Q=0$, $\bar{Q}=1$ and 4 clock pulses are fed at the input. The output waveforms are as follows



From these waveforms, we find that output period (T_2) is twice the clock period (T_1) ie output frequency is one-half the clock frequency. Hence a T FF is said to function as a divide by 2 circuit.

Preset and Clear terminals in a clocked RS FF



In most FFs, the clear or reset operation may be done by applying a low voltage to the clear input of the FF, while maintaining the preset input high. ie $Cr=0$, $Pr=1$.

If the FF is to be set, then apply a low voltage to the preset input, with clear input high. ie $Pr=0$, $Cr=1$.

The action of these inputs is independent of clock. ie their action is seen even when the clock is low. Hence preset, clear inputs are called direct or asynchronous inputs ie. not in synchronism with the clock.

However, once the state of the FF is established using these inputs, they must be maintained high so that normal working of the FF can take place when a CLK arrives.

In the circuit of a clocked RS FF shown above, if $Pr=0$, $Cr=1$ then immediately $Q=1$ & $\bar{Q}=0$. FF is SET without the help of clock.

If $Pr=1$, $Cr=0$, then \bar{Q} becomes 1 and $Q=0$. FF is RESET. If $Pr=1$, $Cr=0$ is maintained, the FF will not respond to changes in S & R. Hence make $Pr=1$, $Cr=1$ (normal working of FF)

CLK	Pr	Cr	Q
0	0	1	1
1	0	1	1
0	1	0	0
1	1	0	0

Normal, dependent on R, S inputs.
Ambiguous, never to be maintained