Sardar Patel Institute of Technology

Bhavan's Campus, Munshi Nagar, Andheri (West), Mumbai-400058, India

(Autonomous College Affiliated to University of Mumbai)

End Semester Examination

May 2019

Max. Marks: 60 **Duration: 3 Hrs**

Class: TE **Semester:VI**

Course Code: CE61 **Branch: Computer**

Name of the Course: System Programming and Compiler Construction

Instructions:

(1) All questions are compulsory

(2) Assume suitable data if necessary

(3) Draw neat diagram wherever required.

Q No.		Max. Marks	CO
Q.1 A	Write an algorithm for pass1 of SIC/XE assembler.	6	CO2
Q.1 B.	Describe the features of Sun OS linkers for SPARC systems. **OR** Explain the design(with the help of example) and algorithm of an absolute loader .	6	CO1
Q.2 A.	List machine independent macro features. Explain any one.	6	CO2
Q.2 B.	Consider the following grammar representing a paragraph written in English Language. $P \rightarrow SR/S$ $R \rightarrow bSR/bS$ $S \rightarrow WbS/W$ $W \rightarrow L * W/L$ $L \rightarrow id$ where P(Start Symbol), R,S,W and L are non-terminals and b, * and id are terminals. A. Determine whether the above grammar is an operator grammar or not(State reason). If not, convert into operator grammar, if possible. B. Construct an operator precedence table for the above grammar by considering precedence and associativity(left or right) of the terminals. C. Parse an input string "id*idbid". Clearly show the contents of stack, current input symbol and action taken at each step. **OR** Construct the LALR parsing table for the following grammar:- $S \rightarrow E$ $E \rightarrow E + (E)$ $E \rightarrow int$ where S and E are non-terminals and +, (,) and int are terminals.	08	CO3
Q.3 A.	Give example cases of all types of conflicts with respect to SLR(1) grammar.	5	CO3

Q.3 B.	Write a short note on input buffering in lexical analysis with example.	4	CO3
Q.4 A.	How syntax tree is created for 4-b+c? Explain with the help of Syntax Directed Definition. **OR** Generate an assembly code for the following intermediate code snippet using code generation algorithm: $d = (a-b)+(a-c)+(a-c)$ Register R0, R1 are the only registers available. Assume ST, MOV, ADD and SUB are the instruction opcodes which have two operands only. For e.g. Mov R0,a means that memory address of a(source) is copied in register R0(destination). Assumptions for the other instruction opcodes can be made similarly. Clearly show the contents of different descriptors after each conversion of three address instruction to assembly instruction.	6	CO3
Q.4 B.	What does backpatching mean ? Illustrate with a simple example.	8	CO3 CO4
Q.5 A.	Generate three address code and a quadruple, triple of a generated three-address code in static single assignment form for the expression $a[i] = b[i+1] + (k*2)$.	6	CO3 CO4
Q.5 B.	Explain mark and sweep and copy collector garbage collection methods with respect to examples only.	5	CO5