Tutorial

Common Mistakes

- Didn’t used $finish at the end of testbench.
- Using initial block instead of always/forever block for clock.
- Forget to initialize clock in the testbench.
- Using incorrect module names and forgetting semicolon at the end of each line.

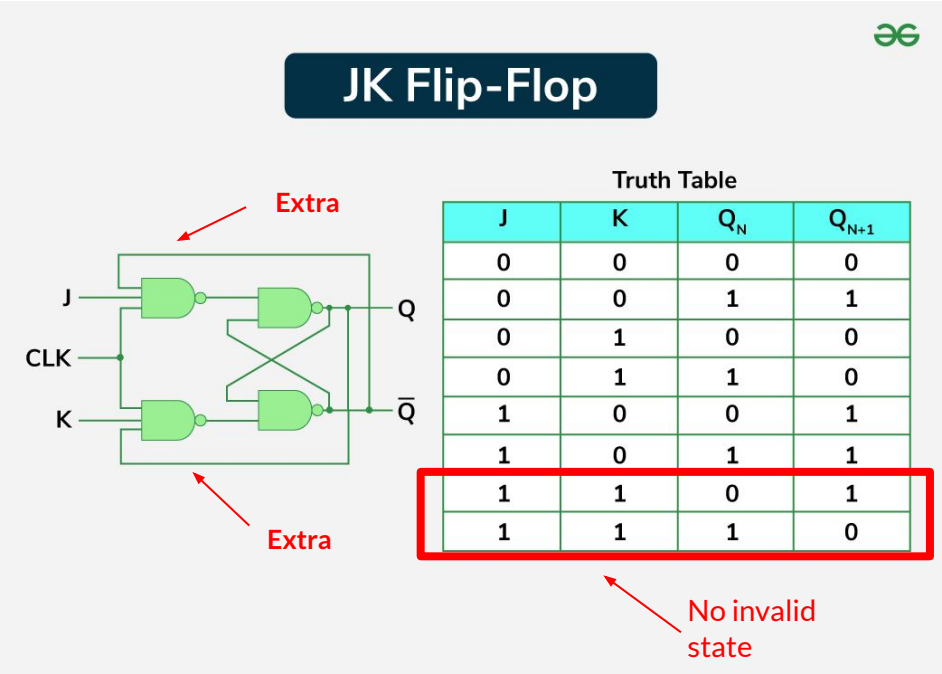
More About Flip Flops

Why do we need one more flip-flop?

- No Invalid States
- Need a device which can toggle its previous state.

JK-Flip Flop

$$Q(t+1) = J\bar{Q}(t) + Q\bar{K}(t)$$



J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

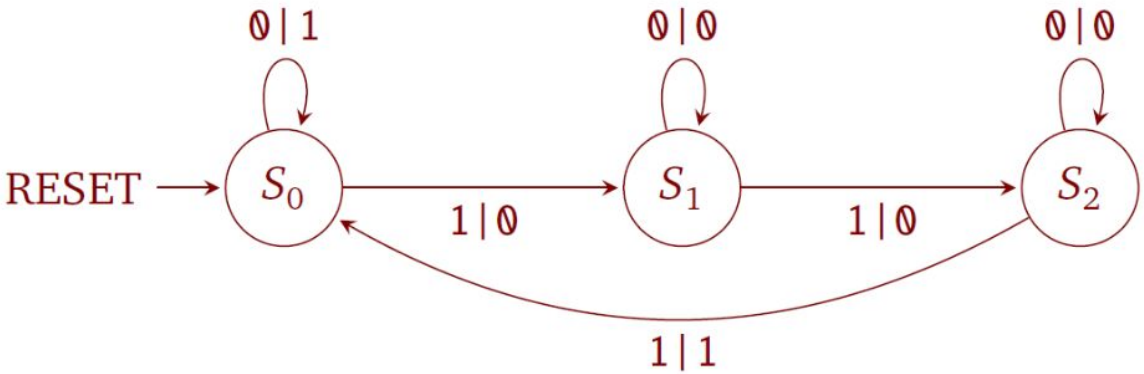
Task-1

JK Flip Flop (Behavioral) Implementation in Verilog

FSM

Task 1

Coding the given FSM in verilog



Task 2

The following is the state transition table for a Moore machine with one input, one output, and four states. Implement this state machine. Include a reset that resets the FSM to state A.

State	Next state		Output
	in=0	in=1	
A	A	B	0
B	C	B	0
C	A	D	0
D	C	B	1