Registers Tutorial

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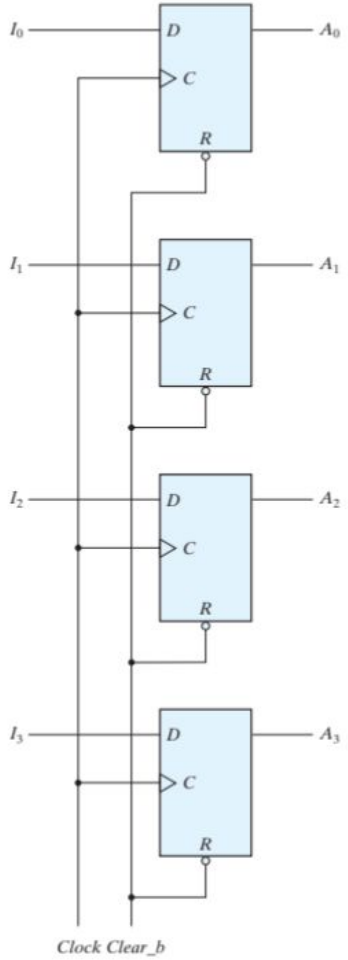
Introduction to Registers

- A register is a group of flip-flops used to store multiple bits of data
- Commonly used in digital systems for temporary data storage
- Essential components in computer memory and processing units
- Temporary data storage in CPUs
- Address storage in memory units
- Implementing counters and timers
- Data conversion between serial and parallel formats

Simple 4-bit Register using D Flip-flops

4-bit register:

1. Data inputs (D0-D3) are connected to flip-flop D inputs
2. Clock signal is applied to all flip-flops simultaneously
3. On the rising edge of the clock:
   - Input data is stored in the flip-flops
   - Outputs (Q0-Q3) reflect the stored data



Parallel Load Register

• Allows simultaneous loading of all data bits

• Useful for quick data transfer between registers or from external sources

1. Data inputs (D0-D3) connected to all flip-flops

2. Load signal enables parallel data input

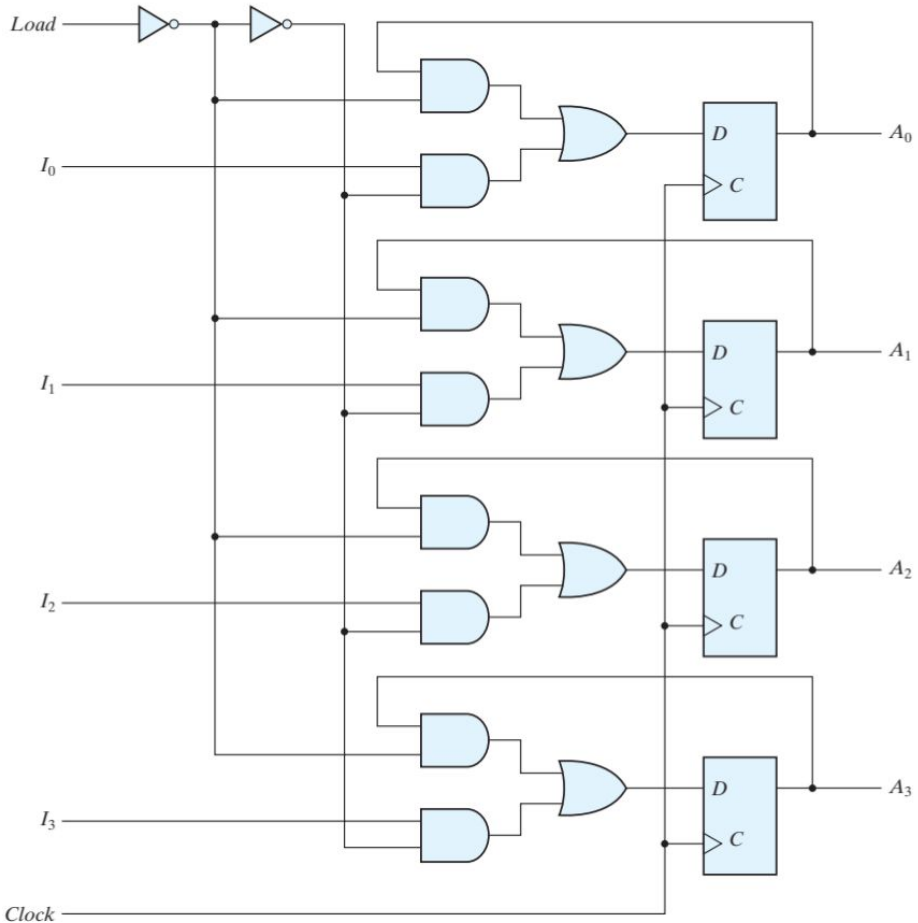
3. When Load is active:

• All flip-flops update simultaneously with new data

• Outputs (Q0-Q3) reflect the loaded data

4.When the Load is inactive the output of flip-flop is loaded into the register.

Parallel load register:



Shift Registers

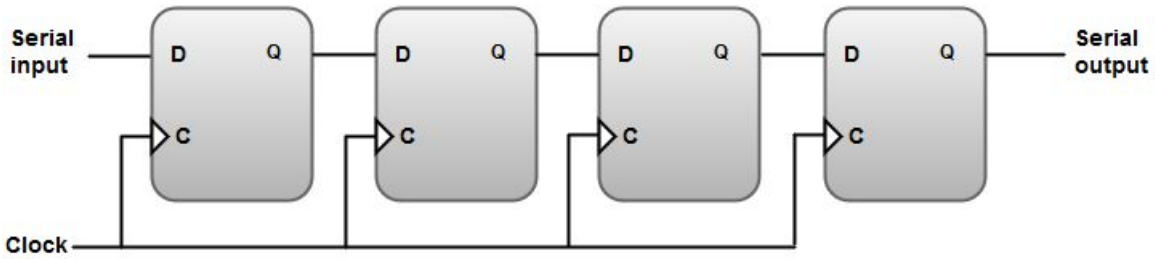
- Special type of register that can shift data left or right
- Used for serial-to-parallel or parallel-to-serial conversion
- Common types:
    - Serial-In Serial-Out (SISO)
    - Serial-In Parallel-Out (SIPO)
    - Parallel-In Serial-Out (PISO)
    - Parallel-In Parallel-Out (PIPO)

- In this course, we will be dealing with Serial-In-Serial-Out (SISO) registers.

Serial-In-Serial-Out Register

- Data enters serially and exits serially
- Each clock pulse shifts data one position to the right
- Commonly used in data transmission over serial lines

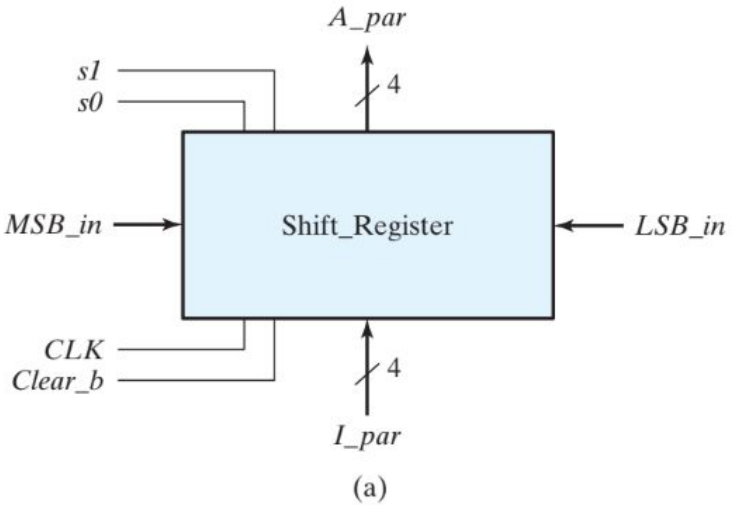
4 - bit Shift-Register:

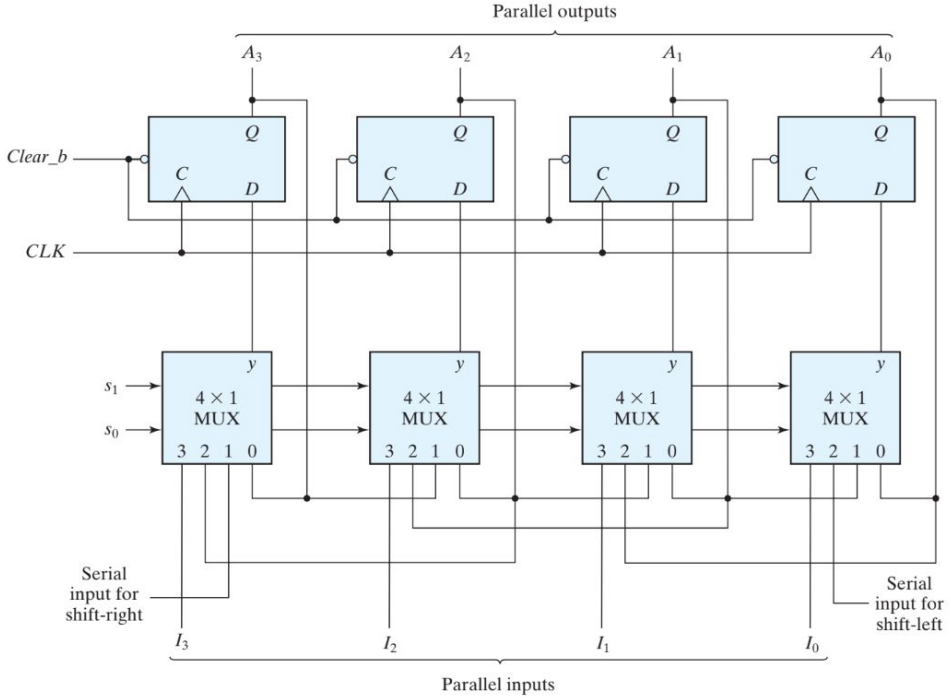


Universal Shift Register

- It has 2-bit control input, that selects one of the below operations:

    1. **Shift Right**: Data moves one position to the right
    2. **Shift Left:** Data moves one position to the left
    3. **Parallel Load:** Load all bits simultaneously
    4. **Hold:** Maintain current data without changes


A_par
s1
s0
4
MSB_in
Shift_Register
LSB_in
CLK
Clear_b
4
I_par
(a)


Parallel outputs
A3
A2
A1
A0
Clear_b
CLK
Q
C
D
s1
s0
4 × 1
MUX
y
3 2 1 0
Serial
input for
shift-right
Serial
input for
shift-left
I3
I2
I1
I0
Parallel inputs
(b)