Dragon 4 | Bus-Control permutations

Ctrl_REG_A

num	hex	binary	description	Control Line
	0x0	0 0 0 0	NONE	NONE
1	0x1	0 0 0 1	Assert | GPR_A | MAIN_BUS	$\overline{CTRL\_GPR\_A\_ASSERT}$
2	0x2	0 0 1 0	Assert | GPR_B | MAIN_BUS	$\overline{CTRL\_GPR\_B\_ASSERT}$
3	0x3	0 0 1 1	Assert | GPR_C | MAIN_BUS	$\overline{CTRL\_GPR\_C\_ASSERT}$
4	0x4	0 1 0 0	Assert | GPR_D | MAIN_BUS	$\overline{CTRL\_GPR\_D\_ASSERT}$
5	0x5	0 1 0 1	Assert | GPR_X | MAIN_BUS	$\overline{CTRL\_GPR\_X\_ASSERT}$
6	0x6	0 1 1 0	Assert | PC | Xfer_BUS	$\overline{CTRL\_PC\_ASSERT\_XFER}$
7	0x7	0 1 1 1	Assert | SP | Xfer_BUS	$\overline{CTRL\_SP\_ASSERT\_XFER}$
8	0x8	1 0 0 0	Assert | CREG | Xfer_BUS	$\overline{CTRL\_CREG\_ASSERT\_XFER}$
9	0x9	1 0 0 1	Assert | ALU | MAIN_BUS	$\overline{CTRL\_ALU\_ASSERT}$
10	0xa	1 0 1 0	Assert | RAM | MAIN_BUS	$\overline{CTRL\_RAM\_ASSERT\_MAIN}$
11	0xb	1 0 1 1	Reserved	Reserved
12	0xc	1 1 0 0	Assert | Xfer | Xfer_BUS	$\overline{CTRL\_XFER\_ASSERT\_XFER}$
13	0xd	1 1 0 1	Assert | Xfer_R | MAIN_BUS	$\overline{CTRL\_XFER\_R\_ASSERT}$
14	0xe	1 1 1 0	Assert | Xfer_L | MAIN_BUS	$\overline{CTRL\_XFER\_L\_ASSERT}$
15	0xf	1 1 1 1	Assert | constant_REG | MAIN_BUS	$\overline{CTRL\_CONST\_ASSERT}$

Ctrl_REG_L

num	hex	binary	description	Control Line
	0x0	0 0 0 0	NONE	NONE
16	0x1	0 0 0 1	Load | GPR_A | MAIN_BUS	$\overline{CTRL\_GPR\_A\_LOAD}$
17	0x2	0 0 1 0	Load | GPR_B | MAIN_BUS	$\overline{CTRL\_GPR\_B\_LOAD}$
18	0x3	0 0 1 1	Load | GPR_C | MAIN_BUS	$\overline{CTRL\_GPR\_C\_LOAD}$
19	0x4	0 1 0 0	Load | GPR_D | MAIN_BUS	$\overline{CTRL\_GPR\_D\_LOAD}$
20	0x5	0 1 0 1	Load | GPR_X | MAIN_BUS	$\overline{CTRL\_GPR\_X\_LOAD}$
21	0x6	0 1 1 0	Load | PC | Xfer_BUS	$\overline{CTRL\_PC\_LOAD\_XFER}$
22	0x7	0 1 1 1	Load | SP | Xfer_BUS	$\overline{CTRL\_SP\_LOAD\_XFER}$
23	0x8	1 0 0 0	Load | CREG | Xfer_BUS	$\overline{CTRL\_CREG\_LOAD\_XFER}$
24	0x9	1 0 0 1	Load | RAM | MAIN_BUS	$\overline{CTRL\_RAM\_LOAD\_MAIN}$
25	0xa	1 0 1 0	Reserved	$\overline{CTRL\_DPLY\_ENABLE}$
26	0xb	1 0 1 1	Load | Instruction_REG | mem_BUS	$\overline{CTRL\_IR\_LOAD}$
27	0xc	1 1 0 0	!C	$\overline{CTRL\_XFER\_LOAD\_XFER}$
28	0xd	1 1 0 1	Load | Xfer_R | MAIN_BUS	$\overline{CTRL\_XFER\_R\_LOAD}$
29	0xe	1 1 1 0	Load | Xfer_L | MAIN_BUS	$\overline{CTRL\_XFER\_L\_LOAD}$
30	0xf	1 1 1 1	Load | constant_REG | mem_BUS	$\overline{CTRL\_CONST\_LOAD}$

Dragon 4 | Bus-Control permutations

Ctrl_CREG_A_addr

num	hex	binary	description	Control Line
	0x0	0 0 0	NONE	NONE
31	0x1	0 0 1	Assert | PC | address_BUS	$\overline{CTRL\_PC\_ASSERT\_ADDR}$
32	0x2	0 1 0	Assert |SP | address_BUS	$\overline{CTRL\_SP\_ASSERT\_ADDR}$
33	0x3	0 1 1	Assert | CREG | address_BUS	$\overline{CTRL\_CREG\_ASSERT\_ADDR}$
34	0x4	1 0 0	Assert | Xfer | address_BUS	$\overline{CTRL\_XFER\_ASSERT\_ADDR}$
35	0x5	1 0 1	Reserved	Reserved
36	0x6	1 1 0	Reserved	Reserved
37	0x7	1 1 1	Reserved	Reserved

Ctrl_GPR_A_ALU_R

num	hex	binary	description	Control Line
	0x0	0 0 0	NONE	NONE
38	0x1	0 0 1	Assert | GPR_A | ALU_R	$\overline{CTRL\_GPR\_A\_ASSERT\_ALU\_R}$
39	0x2	0 1 0	Assert | GPR_B | ALU_R	$\overline{CTRL\_GPR\_B\_ASSERT\_ALU\_R}$
40	0x3	0 1 1	Assert | GPR_C | ALU_R	$\overline{CTRL\_GPR\_C\_ASSERT\_ALU\_R}$
41	0x4	1 0 0	Assert | GPR_D | ALU_R	$\overline{CTRL\_GPR\_D\_ASSERT\_ALU\_R}$
42	0x5	1 0 1	Assert | GPR_X | ALU_R	$\overline{CTRL\_GPR\_X\_ASSERT\_ALU\_R}$
43	0x6	1 1 0	Reserved	Reserved
44	0x7	1 1 1	Reserved	Reserved

Ctrl_GPR_A_ALU_L

num	hex	binary	description	Control Line
	0x0	0 0 0	NONE	NONE
45	0x1	0 0 1	Assert | GPR_A | ALU_L	$\overline{CTRL\_GPR\_A\_ASSERT\_ALU\_L}$
46	0x2	0 1 0	Assert | GPR_B | ALU_L	$\overline{CTRL\_GPR\_B\_ASSERT\_ALU\_L}$
47	0x3	0 1 1	Assert | GPR_C | ALU_L	$\overline{CTRL\_GPR\_C\_ASSERT\_ALU\_L}$
48	0x4	1 0 0	Assert | GPR_D | ALU_L	$\overline{CTRL\_GPR\_D\_ASSERT\_ALU\_L}$
49	0x5	1 0 1	Assert | GPR_X | ALU_L	$\overline{CTRL\_GPR\_X\_ASSERT\_ALU\_L}$
50	0x6	1 1 0	Reserved	Reserved
51	0x7	1 1 1	Reserved	Reserved

Dragon 4 | Bus-Control permutations

Ctrl_CREG_inc					
num	hex	bin		description	Control Line
	0x0	0	0	NONE	NONE
52	0x1	0	1	increase | PC	$\overline{CTRL\_PC\_INC}$
53	0x2	1	0	increase | SP	$\overline{CTRL\_SP\_INC}$
54	0x3	1	1	increase | CREG	$\overline{CTRL\_CREG\_INC}$

Ctrl_CREG_dec					
num	hex	bin		description	Control Line
	0x0	0	0	NONE	NONE
55	0x1	0	1	decrease | PC	$\overline{CTRL\_PC\_DEC}$
56	0x2	1	0	decrease | SP	$\overline{CTRL\_SP\_DEC}$
57	0x3	1	1	decrease | CREG	$\overline{CTRL\_CREG\_DEC}$