Instructionset LED+ architecture

mode	Instruction	OP-Code byte 0	Arg A/immediate byte 1	Arg B/immediate byte 2	destination byte 3
calculate	add	0b00 00 0000	register	register	register
	adc	0b00 00 0001	register	register	register
	sub	0b00 00 0010	register	register	register
	mul	0b00 00 0011	register	register	register
	inc	0b00 00 0100	x	register	register
	dec	0b00 00 0101	x	register	register
	and	0b00 00 0110	register	register	register
	or	0b00 00 0111	register	register	register
	xor	0b00 00 1000	register	register	register
	not	0b00 00 1001	x	register	register
	neg	0b00 00 1010	x	register	register
	shl	0b00 00 1011	x	register	register
	shrl	0b00 00 1100	x	register	register
	shra	0b00 00 1101	x	register	register
	rol	0b00 00 1110	x	register	register
	ror	0b00 00 1111	x	register	register
calculate	iBadd / iadd	0b00 01 0000	register	immediate	register
	iBadc / iadc	0b00 01 0001	register	immediate	register
	iBsub / isub	0b00 01 0010	register	immediate	register
	iBmul / imul	0b00 01 0011	register	immediate	register
	iBinc / iinc	0b00 01 0100	x	immediate	register
	iBdec / idec	0b00 01 0101	x	immediate	register
	iBand / iand	0b00 01 0110	register	immediate	register
	iBor / ior	0b00 01 0111	register	immediate	register
	iBxor / ixor	0b00 01 1000	register	immediate	register
	iBnot / inot	0b00 01 1001	x	immediate	register
	iBneg / ineg	0b00 01 1010	x	immediate	register
	iBshl / ishl	0b00 01 1011	x	immediate	register
	iBshrl / ishrl	0b00 01 1100	x	immediate	register
	iBshra / ishra	0b00 01 1101	x	immediate	register
	iBrol / irol	0b00 01 1110	x	immediate	register
	iBror / iror	0b00 01 1111	x	immediate	register
calculate	iAadd	0b00 10 0000	immediate	register	register
	iAadc	0b00 10 0001	immediate	register	register
	iAsub	0b00 10 0010	immediate	register	register
	iAmul	0b00 10 0011	immediate	register	register
	iAinc (unvalid)	0b00 10 0100	UNVALID	UNVALID	UNVALID
	iAdec (unvalid)	0b00 10 0101	UNVALID	UNVALID	UNVALID
	iAand	0b00 10 0110	immediate	register	register
	iAor	0b00 10 0111	immediate	register	register
	iAxor	0b00 10 1000	immediate	register	register
	iAnot (unvalid)	0b00 10 1001	UNVALID	UNVALID	UNVALID
	iAneg (unvalid)	0b00 10 1010	UNVALID	UNVALID	UNVALID
	iAshl (unvalid)	0b00 10 1011	UNVALID	UNVALID	UNVALID
	iAshrl (unvalid)	0b00 10 1100	UNVALID	UNVALID	UNVALID
	iAshra (unvalid)	0b00 10 1101	UNVALID	UNVALID	UNVALID
	iArol (unvalid)	0b00 10 1110	UNVALID	UNVALID	UNVALID
	iAror (unvalid)	0b00 10 1111	UNVALID	UNVALID	UNVALID
calculate	iABadd	0b00 11 0000	immediate	immediate	register
	iABadc	0b00 11 0001	immediate	immediate	register
	iABsub	0b00 11 0010	immediate	immediate	register
	iABsbb	0b00 11 0011	immediate	immediate	register
	iABinc (unvalid)	0b00 11 0100	UNVALID	UNVALID	UNVALID
	iABdec (unvalid)	0b00 11 0101	UNVALID	UNVALID	UNVALID
	iABand	0b00 11 0110	immediate	immediate	register
	iABor	0b00 11 0111	immediate	immediate	register
	iABxor	0b00 11 1000	immediate	immediate	register
	iABnot (unvalid)	0b00 11 1001	UNVALID	UNVALID	UNVALID
	iABneg (unvalid)	0b00 11 1010	UNVALID	UNVALID	UNVALID
	iABshl (unvalid)	0b00 11 1011	UNVALID	UNVALID	UNVALID
	iABshrl (unvalid)	0b00 11 1100	UNVALID	UNVALID	UNVALID
	iABshra (unvalid)	0b00 11 1101	UNVALID	UNVALID	UNVALID
	iABrol (unvalid)	0b00 11 1110	UNVALID	UNVALID	UNVALID
	iABror (unvalid)	0b00 11 1111	UNVALID	UNVALID	UNVALID

mode	Instruction	OP-Code byte 0	Arg A/immediate byte 1	Arg B/immediate byte 2	destination byte 3
move	mov / move	0b01 00 0000	register	(addr register)	register / RAM / IO
	push	0b01 00 0001	register	x	RAM
	pop	0b01 00 0010	RAM	x	register / IO
	jmp	0b01 00 0011	register	x	register
		0b01 00 0100			
		0b01 00 0101			
		0b01 00 0110			
		0b01 00 0111			
		0b01 00 1000			
		0b01 00 1001			
		0b01 00 1010			
		0b01 00 1011			
		0b01 00 1100			
		0b01 00 1101			
		0b01 00 1110			
		0b01 00 1111			
move	iamov / iamove	0b01 01 0000	register	immediate	RAM
		0b01 01 0001			
		0b01 01 0010			
		0b01 01 0011			
		0b01 01 0100			
		0b01 01 0101			
		0b01 01 0110			
		0b01 01 0111			
		0b01 01 1000			
		0b01 01 1001			
		0b01 01 1010			
		0b01 01 1011			
		0b01 01 1100			
		0b01 01 1101			
		0b01 01 1110			
		0b01 01 1111			
move	ivmov / ivmove	0b01 10 0000	immediate	(addr register)	register / RAM / IO
	ipush	0b01 10 0001	immediate	x	RAM
	ipop	0b01 10 0010	immediate	x	register / IO
	ijmp	0b01 10 0011	immediate	x	register
		0b01 10 0100			
		0b01 10 0101			
		0b01 10 0110			
		0b01 10 0111			
		0b01 10 1000			
		0b01 10 1001			
		0b01 10 1010			
		0b01 10 1011			
		0b01 10 1100			
		0b01 10 1101			
		0b01 10 1110			
		0b01 10 1111			
move		0b01 11 0000			
		0b01 11 0001			
		0b01 11 0010			
		0b01 11 0011			
		0b01 11 0100			
		0b01 11 0101			
		0b01 11 0110			
		0b01 11 0111			
		0b01 11 1000			
		0b01 11 1001			
		0b01 11 1010			
		0b01 11 1011			
		0b01 11 1100			
		0b01 11 1101			
		0b01 11 1110			
		0b01 11 1111			

mode	Instruction	OP-Code byte 0	Arg A/immediate byte 1	Arg B/immediate byte 2	destination byte 3
condition	jz	0b01 00 0000	register	x	PC
	jnz	0b01 00 0001	register	x	PC
	js	0b01 00 0010	register	x	PC
	jns	0b01 00 0011	register	x	PC
	jc	0b01 00 0100	register	x	PC
	jnc	0b01 00 0101	register	x	PC
	je (equal)	0b01 00 0110	register	register	PC
	jne (not equal)	0b01 00 0111	register	register	PC
	ja (above unsigned)	0b01 00 1000	register	register	PC
	jb (below unsigned)	0b01 00 1001	register	register	PC
	jg (greater signed)	0b01 00 1010	register	register	PC
	jl (less signed)	0b01 00 1011	register	register	PC
	jp / jpe (even parity)	0b01 00 1100	register	x	PC
	jnp / jpo (odd parity)	0b01 00 1101	register	x	PC
	jcz (last calc. zero)	0b01 00 1110	register	x	PC
	jcnz (last calc. not zero)	0b01 00 1111	register	x	PC
condition		0b01 01 0000			
		0b01 01 0001			
		0b01 01 0010			
		0b01 01 0011			
		0b01 01 0100			
		0b01 01 0101			
	iBJE (equal)	0b01 01 0110	register	immediate	PC
	iBJNE (not equal)	0b01 01 0111	register	immediate	PC
	iBJA (above unsigned)	0b01 01 1000	register	immediate	PC
	iBJB (below unsigned)	0b01 01 1001	register	immediate	PC
	iBJG (greater signed)	0b01 01 1010	register	immediate	PC
	iBJL (less signed)	0b01 01 1011	register	immediate	PC
		0b01 01 1100			
		0b01 01 1101			
		0b01 01 1110			
		0b01 01 1111			
condition	iAjz	0b01 10 0000	immediate	x	PC
	iAjnz	0b01 10 0001	immediate	x	PC
	iAjs	0b01 10 0010	immediate	x	PC
	iAjns	0b01 10 0011	immediate	x	PC
	iAjc	0b01 10 0100	immediate	x	PC
	iAjnc	0b01 10 0101	immediate	x	PC
	iAje (equal)	0b01 10 0110	immediate	register	PC
	iAjne (not equal)	0b01 10 0111	immediate	register	PC
	iAja (above unsigned)	0b01 10 1000	immediate	register	PC
	iAjb (below unsigned)	0b01 10 1001	immediate	register	PC
	iAjg (greater signed)	0b01 10 1010	immediate	register	PC
	iAjl (less signed)	0b01 10 1011	immediate	register	PC
	iAjp / iAjpe (even parity)	0b01 10 1100	immediate	x	PC
	iAjnp / iAjpo (odd parity)	0b01 10 1101	immediate	x	PC
	iAjcz (last calc. zero)	0b01 10 1110	immediate	x	PC
	iAjcnz (last calc. not zero)	0b01 10 1111	immediate	x	PC
condition		0b01 11 0000			
		0b01 11 0001			
		0b01 11 0010			
		0b01 11 0011			
		0b01 11 0100			
		0b01 11 0101			
	iABJE (equal)	0b01 11 0110	immediate	immediate	PC
	iABJNE (not equal)	0b01 11 0111	immediate	immediate	PC
	iABJA (above unsigned)	0b01 11 1000	immediate	immediate	PC
	iABJB (below unsigned)	0b01 11 1001	immediate	immediate	PC
	iABJG (greater signed)	0b01 11 1010	immediate	immediate	PC
	iABJL (less signed)	0b01 11 1011	immediate	immediate	PC
		0b01 11 1100			
		0b01 11 1101			
		0b01 11 1110			
		0b01 11 1111			