Dragon_4_Bus-Control_permutations

Ctrl_REG_A

num	hex	binary	description	Control Line
0	0x0	0 0 0 0	NONE	NONE
1	0x1	0 0 0 1	Assert | GPR_A | MAIN_BUS	
2	0x2	0 0 1 0	Assert | GPR_B | MAIN_BUS	
3	0x3	0 0 1 1	Assert | GPR_C | MAIN_BUS	
4	0x4	0 1 0 0	Assert | GPR_D | MAIN_BUS	
5	0x5	0 1 0 1	Assert | GPR_X | MAIN_BUS	
6	0x6	0 1 1 0	Assert | PC | Xfer_BUS	
7	0x7	0 1 1 1	Assert | SP | Xfer_BUS	
8	0x8	1 0 0 0	Assert | CREG | Xfer_BUS	
9	0x9	1 0 0 1	Assert | ALU | MAIN_BUS	
10	0xa	1 0 1 0	Assert | RAM | MAIN_BUS	
11	0xb	1 0 1 1	Reserved	Reserved
12	0xc	1 1 0 0	Assert | Xfer | Xfer_BUS	
13	0xd	1 1 0 1	Assert | Xfer_R | MAIN_BUS	
14	0xe	1 1 1 0	Assert | Xfer_L | MAIN_BUS	
15	0xf	1 1 1 1	Assert | constant_REG | MAIN_BUS	

Ctrl_REG_L

num	hex	binary	description	Control Line
16	0x0	0 0 0 0	NONE	NONE
17	0x1	0 0 0 1	Load | GPR_A | MAIN_BUS	
18	0x2	0 0 1 0	Load | GPR_B | MAIN_BUS	
19	0x3	0 0 1 1	Load | GPR_C | MAIN_BUS	
20	0x4	0 1 0 0	Load | GPR_D | MAIN_BUS	
21	0x5	0 1 0 1	Load | GPR_X | MAIN_BUS	
22	0x6	0 1 1 0	Load | PC | Xfer_BUS	
23	0x7	0 1 1 1	Load | SP | Xfer_BUS	
24	0x8	1 0 0 0	Load | CREG | Xfer_BUS	
25	0x9	1 0 0 1	Load | RAM | MAIN_BUS	
26	0xa	1 0 1 0	Reserved	Reserved
27	0xb	1 0 1 1	Load | Instruction_REG | mem_BUS	
28	0xc	1 1 0 0	Load | Xfer | Xfer_BUS	
29	0xd	1 1 0 1	Load | Xfer_R | MAIN_BUS	
30	0xe	1 1 1 0	Load | Xfer_L | MAIN_BUS	
31	0xf	1 1 1 1	Load | constant_REG | mem_BUS	

Dragon_4_Bus-Control_permutations

Ctrl_CREG_A_addr

num	hex	binary	description	Control Line
32	0x0	0 0 0	NONE	NONE
33	0x1	0 0 1	Assert | PC | address_BUS	
34	0x2	0 1 0	Assert |SP | address_BUS	
35	0x3	0 1 1	Assert | CREG | address_BUS	
36	0x4	1 0 0	Assert | Xfer | address_BUS	
37	0x5	1 0 1	Reserved	Reserved
38	0x6	1 1 0	Reserved	Reserved
39	0x7	1 1 1	Reserved	Reserved

Ctrl_GPR_A_ALU_R

num	hex	binary	description	Control Line
40	0x0	0 0 0	NONE	NONE
41	0x1	0 0 1	Assert | GPR_A | ALU_R	
42	0x2	0 1 0	Assert | GPR_B | ALU_R	
43	0x3	0 1 1	Assert | GPR_C | ALU_R	
44	0x4	1 0 0	Assert | GPR_D | ALU_R	
45	0x5	1 0 1	Assert | GPR_X | ALU_R	Reserved
46	0x6	1 1 0	Reserved	Reserved
47	0x7	1 1 1	Reserved	Reserved

Ctrl_GPR_A_ALU_L

num	hex	binary	description	Control Line
48	0x0	0 0 0	NONE	NONE
49	0x1	0 0 1	Assert | GPR_A | ALU_L	
50	0x2	0 1 0	Assert | GPR_B | ALU_L	
51	0x3	0 1 1	Assert | GPR_C | ALU_L	
52	0x4	1 0 0	Assert | GPR_D | ALU_L	
53	0x5	1 0 1	Assert | GPR_X | ALU_L	Reserved
54	0x6	1 1 0	Reserved	Reserved
55	0x7	1 1 1	Reserved	Reserved

Dragon_4_Bus-Control_permutations

Ctrl_CREG_inc					
num	hex	bin		description	Control Line
56	0x0	0	0	NONE	NONE
57	0x1	0	1	increase | PC	
58	0x2	1	0	increase | SP	
59	0x3	1	1	increase | CREG	

Ctrl_CREG_dec					
num	hex	bin		description	Control Line
60	0x0	0	0	NONE	NONE
61	0x1	0	1	decrease | PC	
62	0x2	1	0	decrease | SP	
63	0x3	1	1	decrease | CREG	