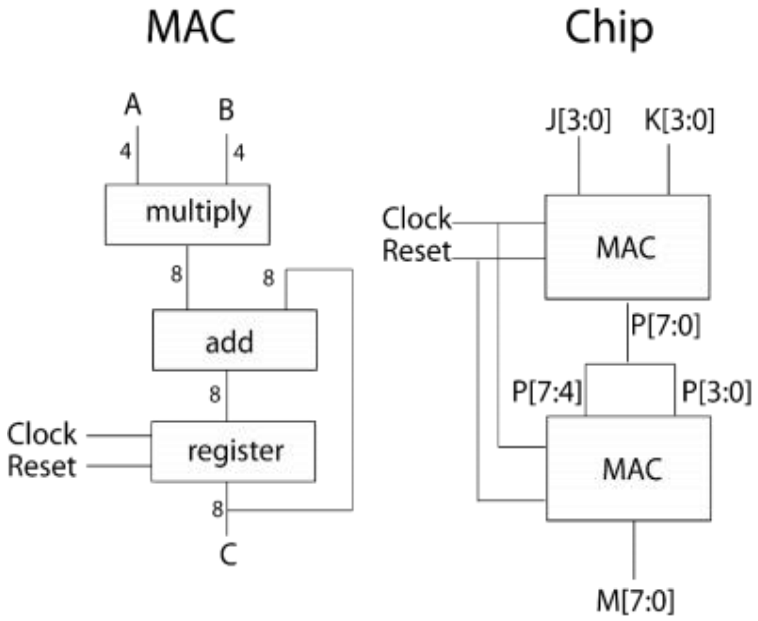
Final Projects of Digital IC Design Practice

Fall Semester 2023

Due Monday, November 27, by 4:00 p.m.

Project 1

You are to design a "Chip" that contains two registered multiply-accumulate (MAC) blocks, as pictured below, that might be used in digital signal processing applications. The MAC is to perform the operation C = C + (A × B), where A and B are unsigned 4-bit numbers and C is the 8-bit number in the register. The active-high Reset signal should clear the register to all 0s, and the register should capture the adder output at the rising edge of each Clock pulse. The "Chip" is to have two 4-bit inputs, J and K, which are the inputs to the first MAC, one 8-bit output M, which is the output of the second MAC, and the Clock and Reset signals, which go to both MACs. The upper and lower 4-bit nibbles of the first MAC output are to be the A and B inputs, respectively, of the second MAC.

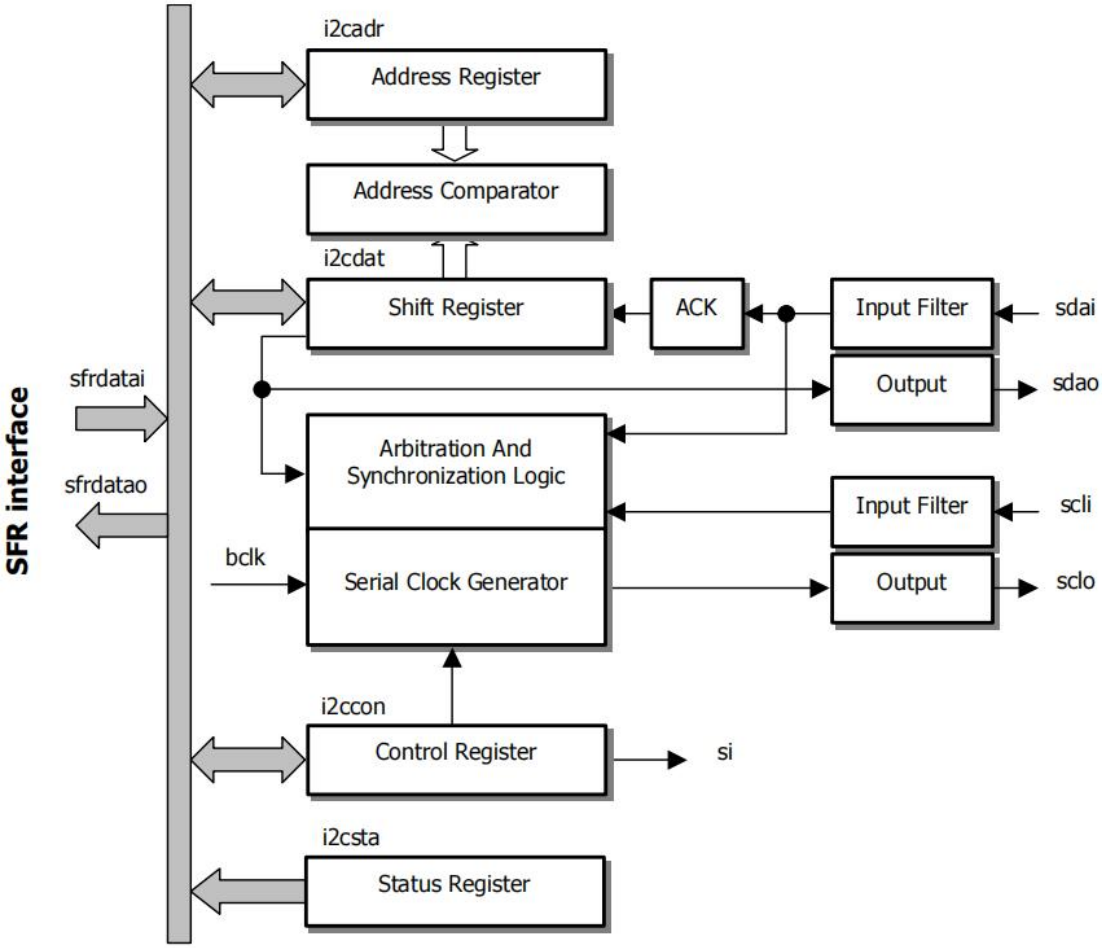


Using the **Dongbu 180nm Process**, the MAC is to be modeled in Verilog, but schematic drawned in Virtuoso, and a physical layout created in Innovus.

For extra credit, you may also finish the typical standard cell design flow paralleled with the semi-custom design flow. The report is to be submitted electronically, addressing the following items.

Project2

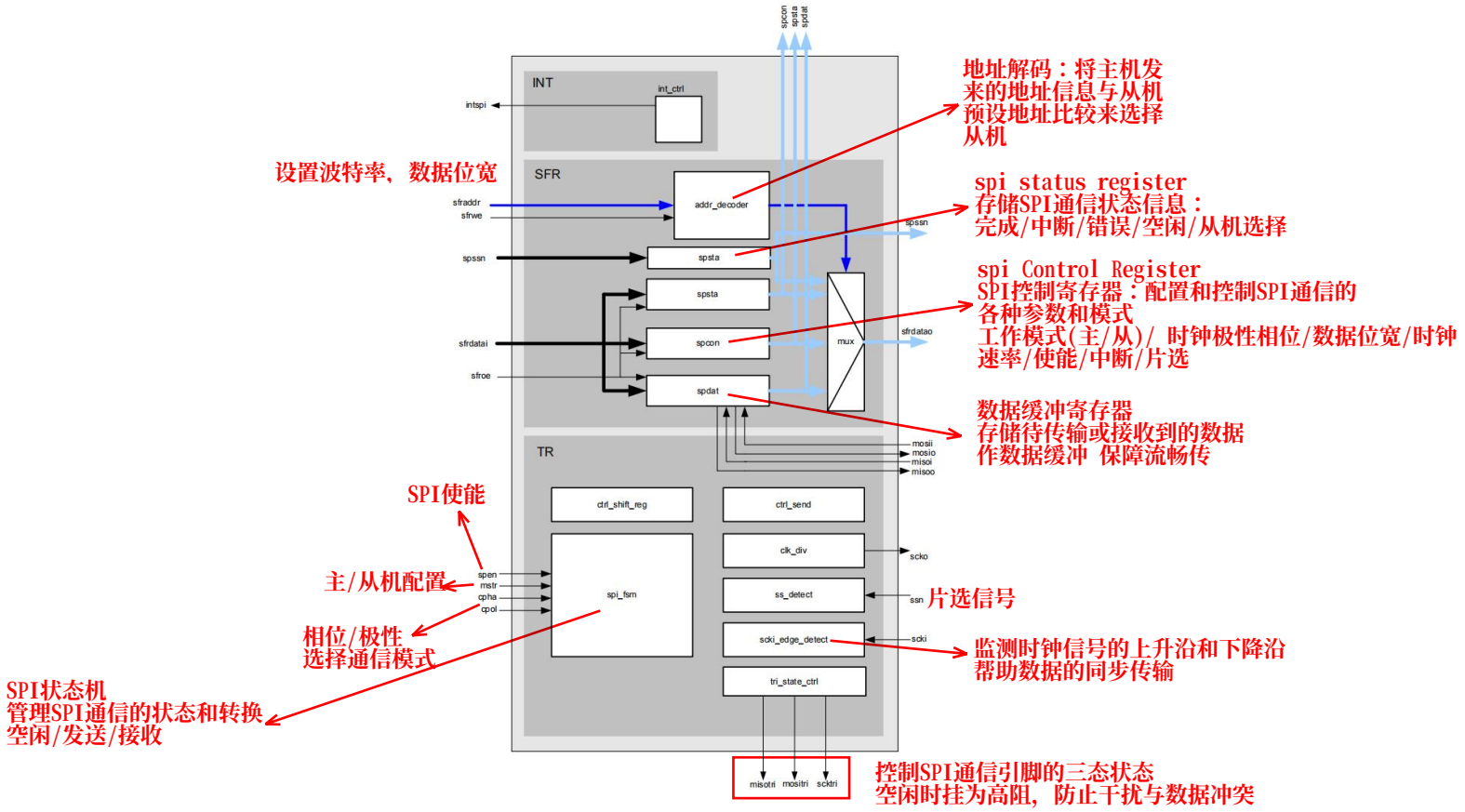
You are to design a "I2C Bus Controller Chip" that provides an interface that meets the Philips I2C bus specification and supports all transfer modes from and to the I2C bus. The I2C bus uses two wires to transfer information between devices connected to the bus: "scl" (serial clock line) and "sda" (serial data line). The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register ("i2csta") reflects the status of the I2C Bus Controller and the I2C bus.



Other requirements are the same as project 1.

Project3

You are to design a "SPI_MS Chip" that allows full-duplex, synchronous, serial communication between the Chip and peripherals.



The SPI_MS provides the following features:

- Full duplex mode
- Master or Slave mode
- Multi SPI Master baud rates
- Slave Clock rate up to Fclk/4 Fclk-CPU时钟
- Serial clock with programmable polarity and phase
- 8-bit data transmitted Most Significant Bit (MSB) first, Least Significant Bit (LSB) last
- ~~8-bit Slave Select Output port to control external slave devices~~ 8bit的片选信号
- No bi-directional ports; standard SPI pins to be externally connected to 3-state buffers

没有双向端口，标准SPI引脚在外部连接到三态缓冲器

Other requirements are the same as project 2&3.