

# Logică digitală



-Curs 1-  
INTRODUCERE  
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# De ce sunteți aici?

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- Motive evidente
    - Curs obligatoriu
    - Necesar pentru toata ramura de HW/embedded
    - Notiuni care vizeaza toate dispozitivele moderne
      - Constructia componentelor complexe din componente mai simple
      - O alta perspectiva a ceea ce este un calculator
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# De ce sunteți aici?

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- Motivele cele mai importante:
    - Conceptul de paralelism inherent pe care îl prezintă HW-ul;  
prima expunere la ceea ce înseamnă calcul paralel
    - Oferă o paradigma complementară design-ului și proiectării software;  
folositor pentru a înțelege ce conceptul de computație
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# Ce veti invata la acest curs?

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- Limbaje si concepte pentru proiectarea HW
    - Algebra booleana, minimizari logice, stare, timp, tool-uri CAD
    - Conceptul de stare in sistemele digitale
    - Analogie cu variabile si programe din SW
  - Specificarea/compilarea/simularea design-urilor
  - Analogie cu design-ul SW
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# Ce veti invata la acest curs?

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- Limbaje si concepte pentru proiectarea HW
  - Specificarea/compilarea/simularea design-urilor
    - Limbaje de descriere HW
    - Tool-uri de simulare pentru verificare
    - Copilatoare logice pentru sinteza blocurilor HW din design-ul nostru
    - Mapare
  - Analogie cu design-ul SW
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# Ce veti invata la acest curs?

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- Limbaje si concepte pentru proiectarea HW
- Specificarea/compilarea/simularea design-urilor
- Analogie cu design-ul SW
  - Amandoua mapeaza probleme bine intelese/specificate pe dispozitive
  - Amandoua trebuie sa functioneze corect...pretul platit pentru matematici discrete

# Prezentare curs

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## **Curs 1. Introducere în Design-ul Digital**

Reprezentarea unui design; Niveluri de abstractizare; Procesul aferent unui design; Programe CAD

## **Curs 2-3. Tipuri de date și reprezentarea lor în sistemele de calcul**

Sisteme de numerație pozitionale; Sisteme de numerație: binar, octal, hexazecimal; Reprezentarea numerelor binare în sistemele de calcul; Reprezentarea numerelor de virgulă flotantă; Coduri binare pentru numere zecimale

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# Prezentare curs

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## **Curs 4-5. Algebra Booleană și logica digitală**

Axiomele și teoremele algebrei booleene; Funcții booleene; Forma canonică; Forma standard; Porti logice; Aspecte legate de implementarea portilor logice;

## **Curs 6-7. Simplificarea funcțiilor booleene**

Metoda hărților Karnaugh; Metoda tabulară Quine McCluskey; Sinteză funcțiilor folosind biblioteci standard de porti; Hazardul în design-ul digital;

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# Prezentare curs

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## **Curs 8-9. Circuite combinaționale**

Sumatoare; Multiplexoare; Demultiplexoare;  
Magistrale; Unități logice: Unitate Aritmetică-logică;  
Circuite combinaționale mai complexe;

## **Curs 10-12. Circuite secvențiale**

Clasificarea circuitelor secvențiale; Elemente de memorare asincrone: tabelul caracteristic, tabelul excitațiilor, și ecuația de stare; Elemente de memorare sincrone: tabelul caracteristic, tabelul excitațiilor, și ecuația de stare; Analiza circuitelor secvențiale; Sinteza circuitelor secvențiale;

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# Prezentare curs

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## **Curs 13. Componente pentru memorare**

Registre; Numărătoare; Pila de registre; Stiva

## **Curs 14. Circuite secvențiale: sinteza**

Diagrame ASM; Sinteza circuitelor secvențiale folosind diagrame ASM;

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# Textbooks & resources

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- <https://sites.google.com/site/logicadigitala/home/couse>
  - John F. Wakerly „Digital Design: Principles and Practices”, 3rd Edition, Prentice Hall, 2000
  - Daniel D. Gajski „Principles of Digital Design”, Prentice Hall, 1997
  - <http://store.digilentinc.com/>
  - <http://www.testbench.in/>
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# Lucrări laborator

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**Lucrarea 1. FOLOSIREA CAD-URILOR – SCRIPT TCL - ALTERA**

**Lucrarea 2. IMPLEMENTAREA UNUI CIRCUIT ÎN DISPOZITIVE FPGA**

**Lucrarea 3. IMPLEMENTAREA CIRCUITELOR COMBINACIONALE ÎN LIMBAJUL VERILOG HDL**

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# Lucrări laborator

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- Lucrarea 4. MINIMIZAREA FUNCȚIILOR LOGICE.**
  
  - Lucrarea 5-6. IMPLEMENTAREA DECODIFICATORULUI PENTRU AFIȘAJUL CU 7 SEGMENTE .**
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# Lucrări laborator

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- Lucrarea 7. IMPLEMENTAREA CIRCUITELOR DE DEPLASARE BARREL SHIFTER .**
  - Lucrarea 8-9. CIRCUITE SECVENTIALE .**
  - Lucrarea 10-11. AUTOMATE CU STARI FINITE.**
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# Notare

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60 % Examen:

- Întrebări de 0.5-1p notiuni aplicate!
- Aplicații – rezolvarea 1-2 probleme (open book)

40 % Activitate pe parcurs:

- 2 Lucrari anuntate
  - realizarea sarcinilor de laborator – 2,3,...  
lucrari neanuntate + Grad realizare  
sarcini laborator + Implicare + ...
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# Administrativ

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- Prezență laborator obligatorie!**
  - Vă rog să respectați slot-ul din orar!**
  - Dacă doriti alt slot:**
    - Schimb – deziderat: sg. echilibrate
    - Acordul responsabilului la laboratorul respectiv
    - Nu mai târziu de S2
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# **Introducere În Design-ul Digital**

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- Reprezentarea unui design;
  - Niveluri de abstractizare;
  - Programe CAD;
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# Reprezentarea unui design

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- **Reprezentare comportamentală sau funcțională**
  - Specifică comportamentul sau funcția unui design fără a oferi informații legate de implementare;
- **Reprezentare structurală**
  - Specifică implementarea unui design în termeni de componente de bază și maniera în care sunt interconectate
- **Reprezentarea fizică**
  - Specifică caracteristicile fizice ale design-ului
- ***Blueprint pt. producție***

# Niveluri de abstractizare

Niveluri	Descriere	Componente structurale	Obiecte fizice
Tranzistor	Ec.diferențiale, diagrame U/I	Tranzistori, rezistori, cap.	Celule analogice și digitale
Logic	Ec.booleene, FSM	Porti, elem. De mem.	Module sau unități
Procesor	Algoritmi, set de instrucțiuni	Sumatoare, comp., registre	Microcipuri
Sistem	Programe, Specificări de executabile	Procesoare, controlere, memorii, IP	Printed-circuit boards, System-on-chip

# Etapele de design (1)

Design and implement a simple unit permitting to speed up encryption with RC5-similar cipher with fixed key set on 8031 microcontroller. Unlike in the experiment 5, this time your unit has to be able to perform an encryption algorithm by itself, executing 32 rounds.....

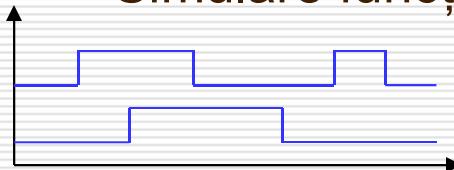
## Specificații funcționare sistem

```
Library IEEE;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

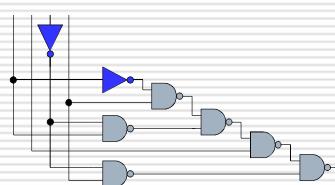
entity RC5_core is
  port(
    clock, reset, encr_decr: in std_logic;
    data_input: in std_logic_vector(31 downto 0);
    data_output: out std_logic_vector(31 downto 0);
    out_full: in std_logic;
    key_input: in std_logic_vector(31 downto 0);
    key_read: out std_logic;
  );
end AES_core;
```

## Descrierea folosind un limbaj de descriere hardware

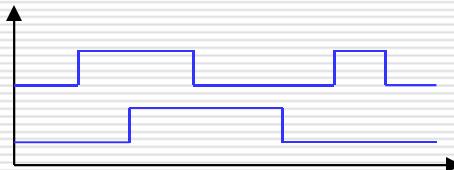
## Simulare funcțională



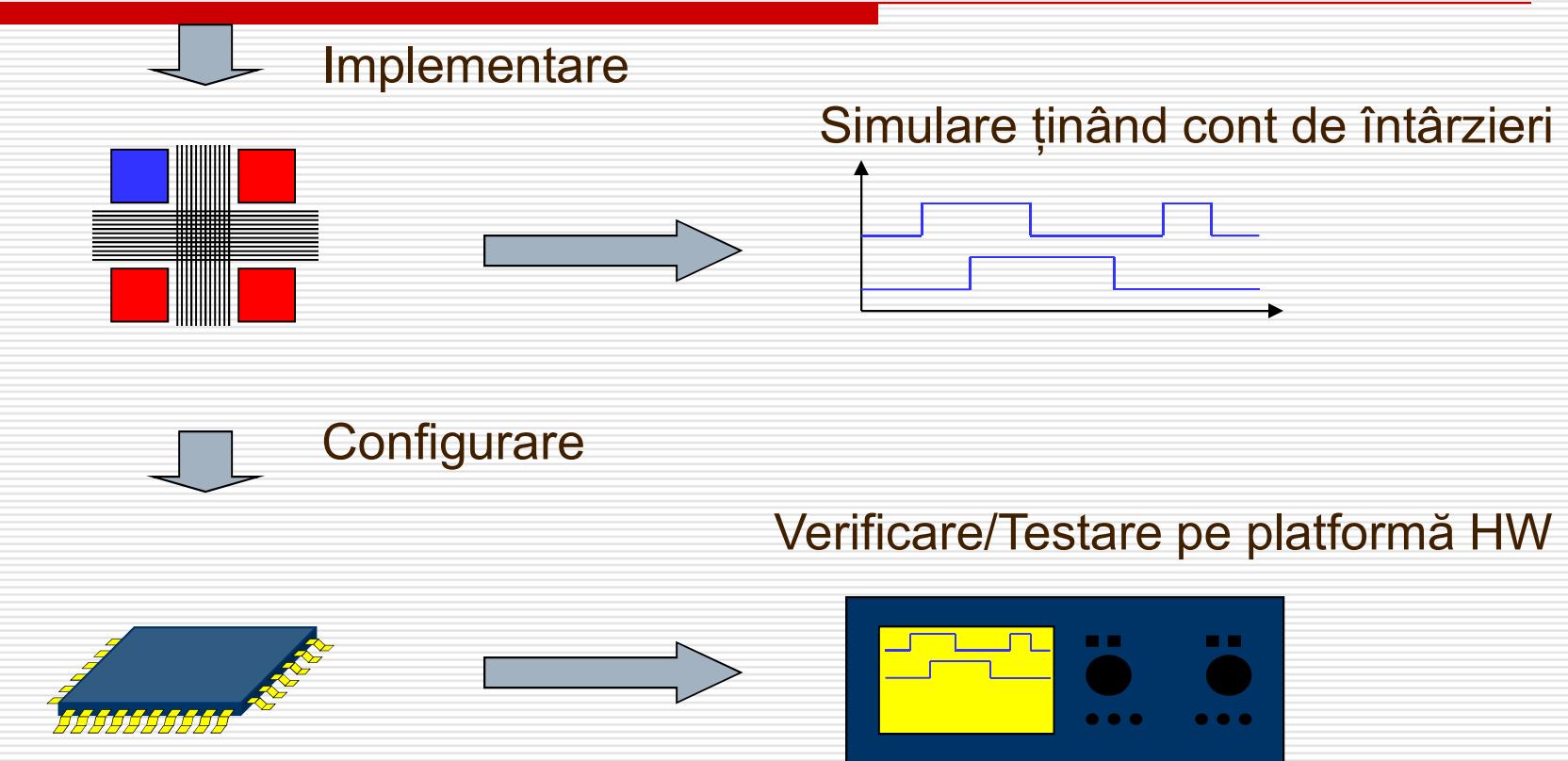
## Sinteză



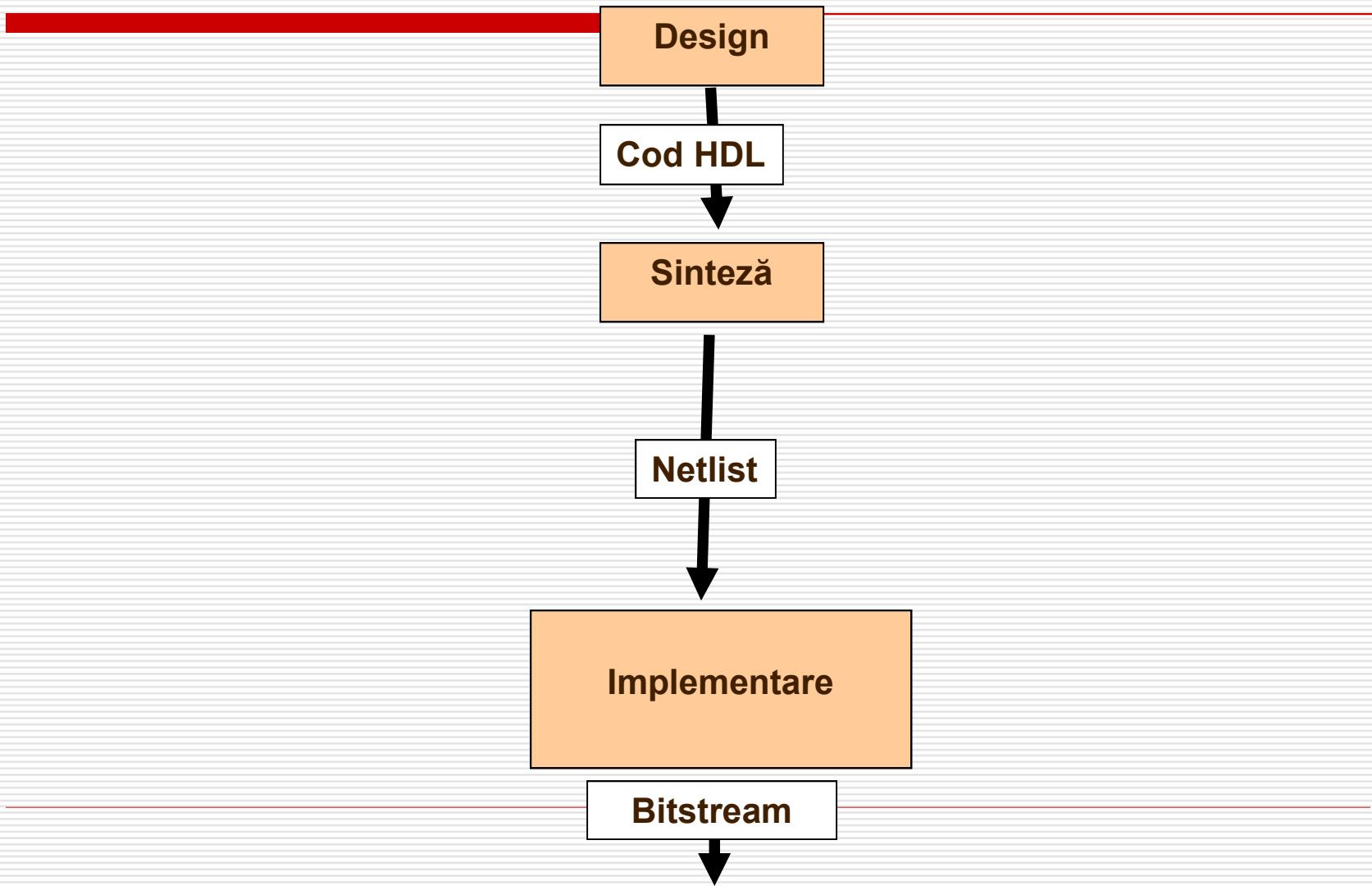
## Simulare post-sinteză



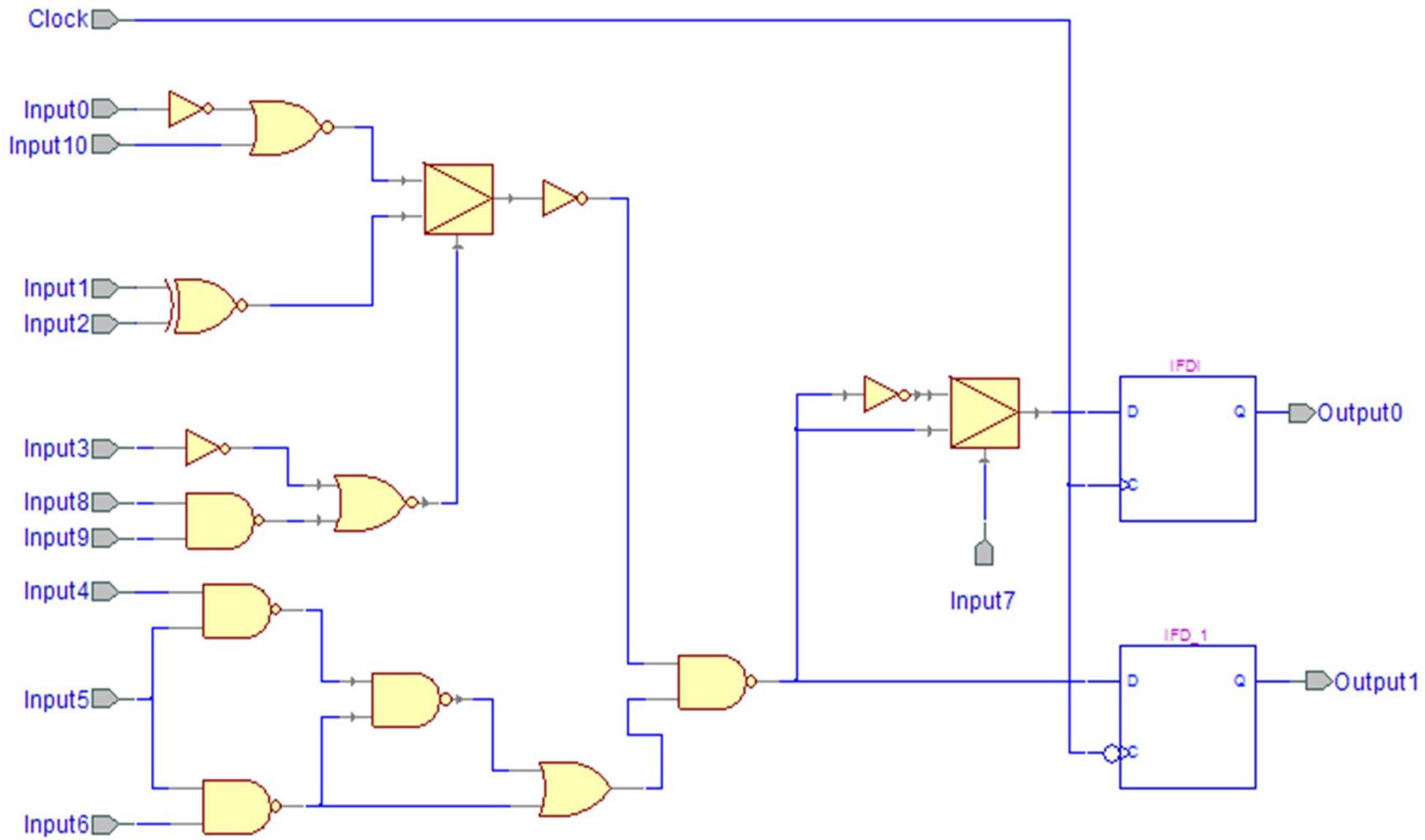
# Etape de design (2)



# Tool-uri folosite în etapele de Design pe FPGA



# Exemplu netlist (post-sinteză)

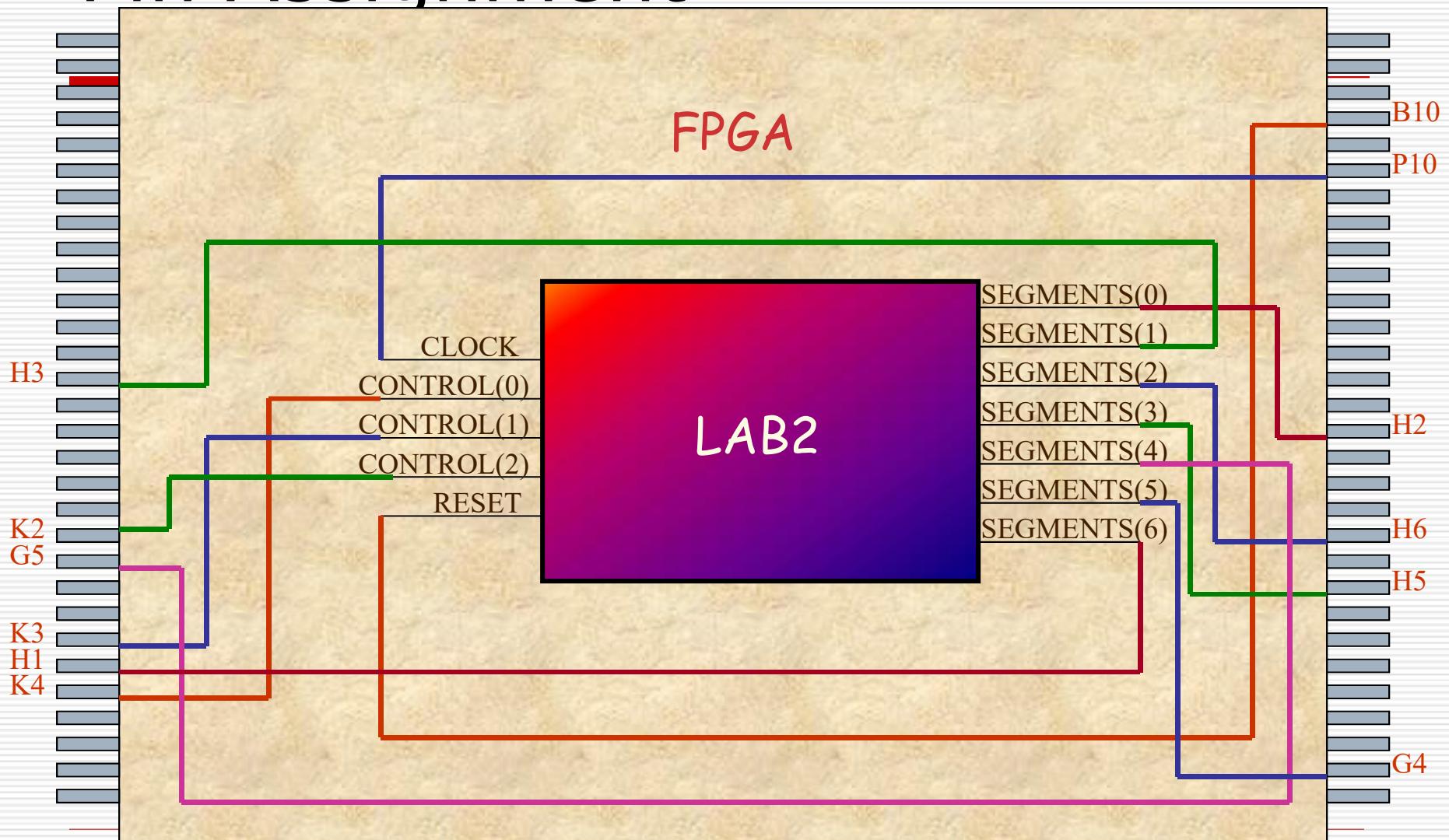


# Implementare

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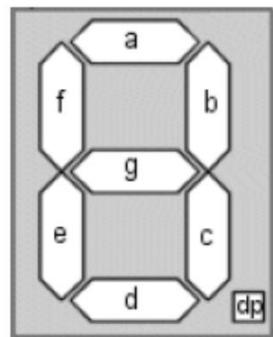
- După sinteză întregul proces legat de implementare este rezultatul tool-urilor puse la dispozitie de vendorii de FPGA
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# Pin Assignment

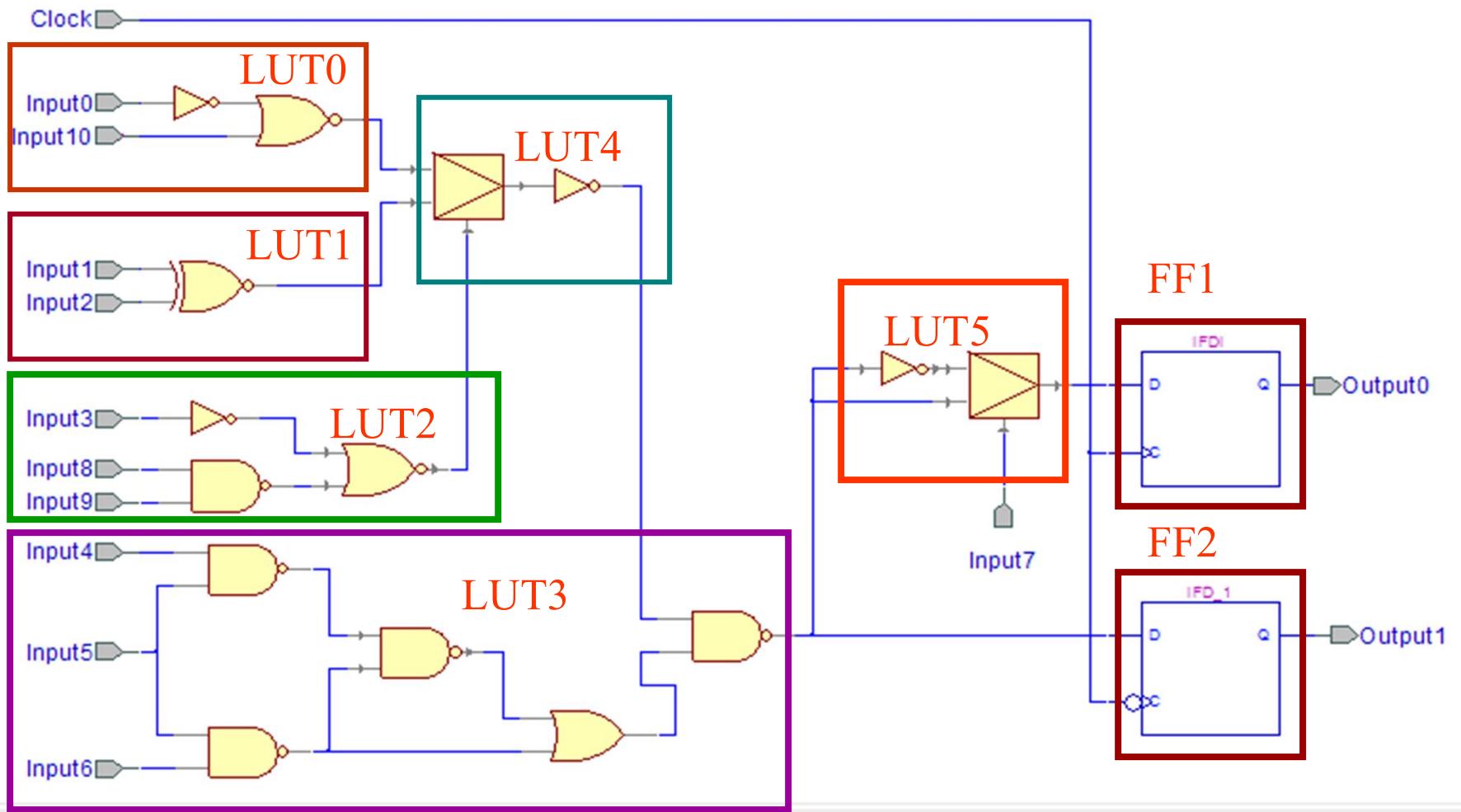


<b>Description</b>	<b>FPGA Pins</b>
Seven Segment 0 'a'	H2
Seven Segment 0 'b'	H3
Seven Segment 0 'c'	H6
Seven Segment 0 'd'	H5
Seven Segment 0 'e'	G5
Seven Segment 0 'f'	G4
Seven Segment 0 'g'	H1
Seven Segment 0 'dp'	C2
Seven Segment 1 'a'	J1
Seven Segment 1 'b'	J2
Seven Segment 1 'c'	K2
Seven Segment 1 'd'	C3
Seven Segment 1 'e'	C1
Seven Segment 1 'f'	H4
Seven Segment 1 'g'	B1
Seven Segment 1 'dp'	J4

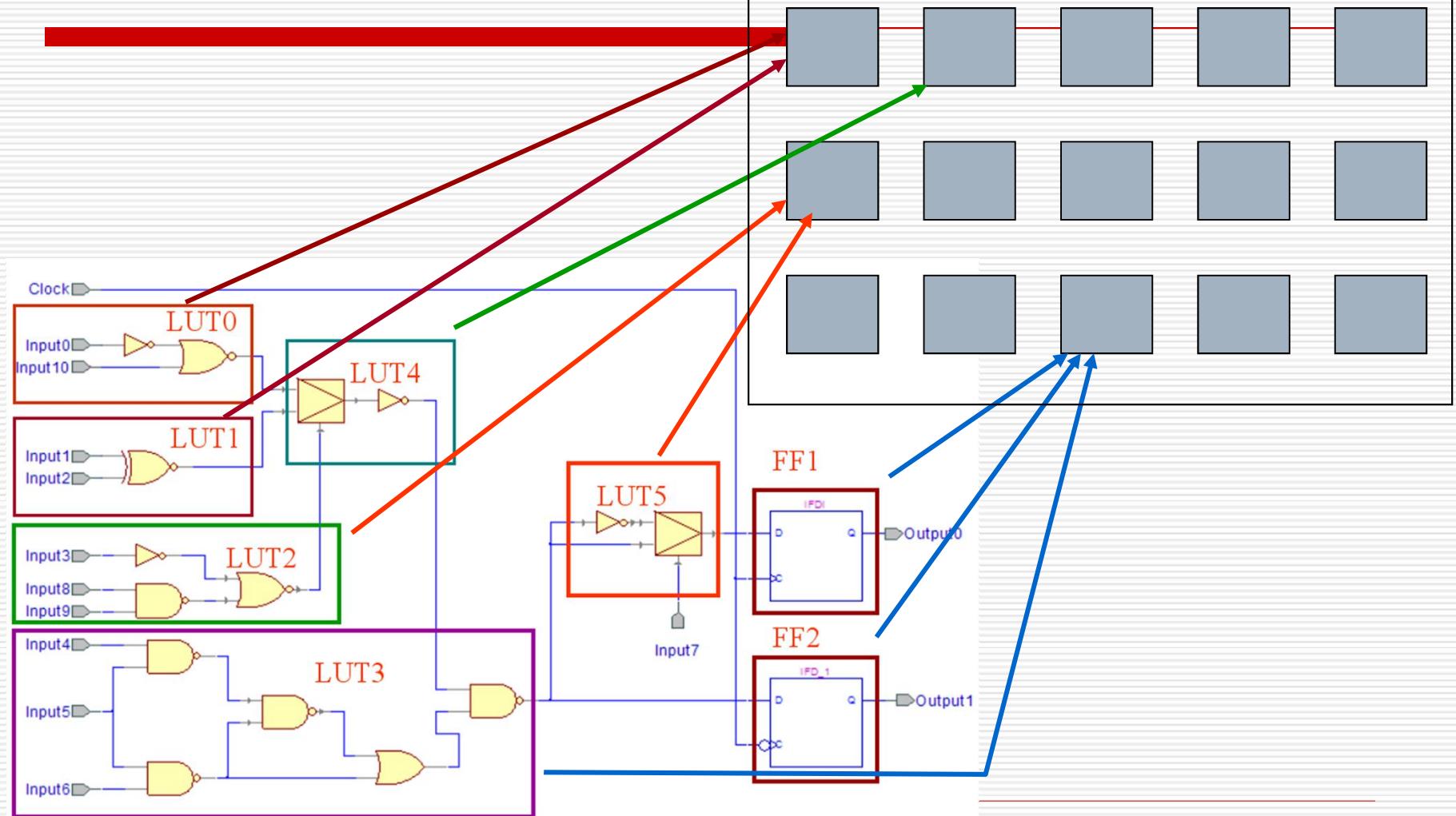
The segments of the display are labelled "a-g" and "dp" in the table above and the figure below.



# Mapping

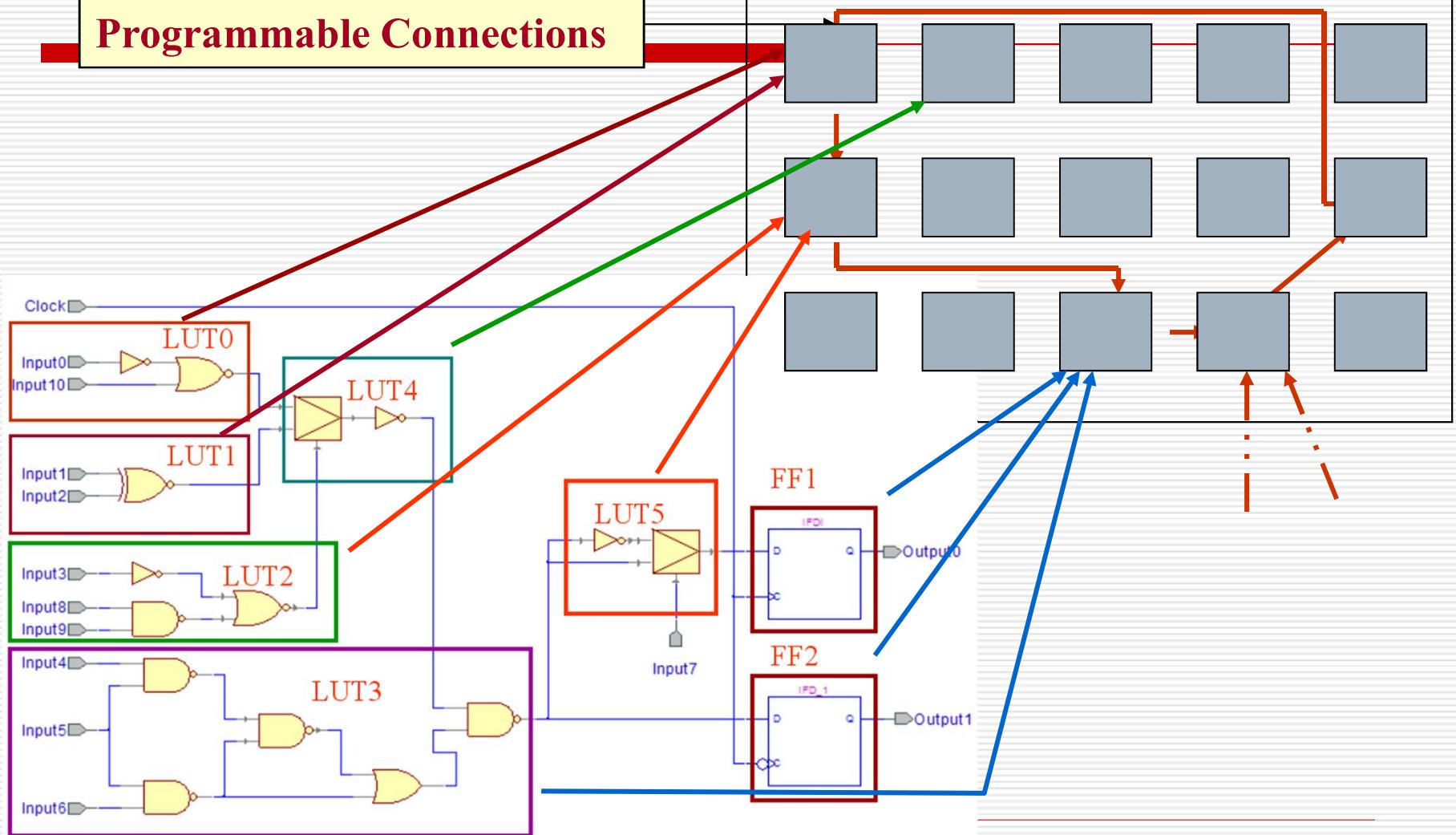


# Placing



# Routing

## Programmable Connections



# Configuration

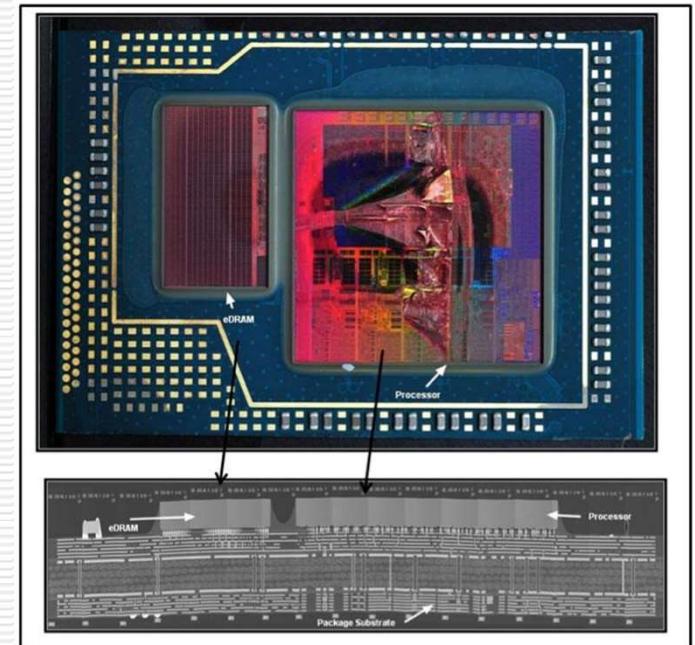
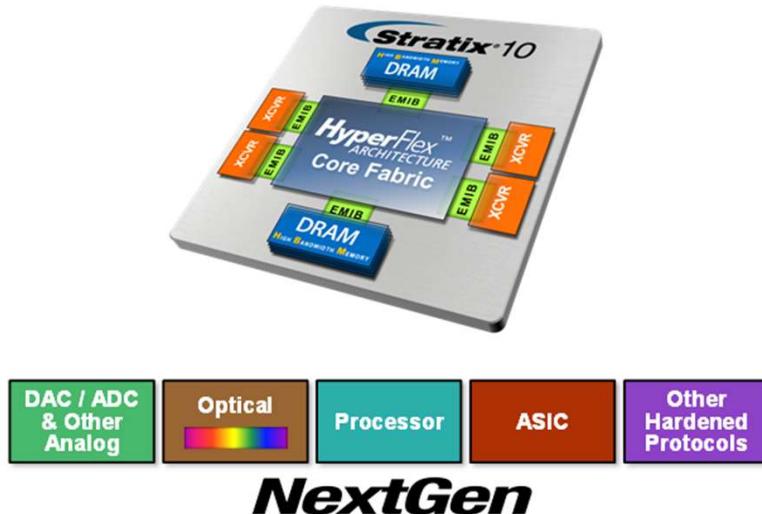
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- După ce întregul design este realizat el trebuie să fie scris într-un format recunoscut de FPGA
  - Acest fișier se numește bit stream: BIT file (.bit)
- Acest fisier BIT poate fi descarcat pe FPGA sau poate fi convertit într-un fișier PROM care să conțină info. de configurare



# FPGA/System-in-Package

Intel consolidates on the FPGA market by acquiring Altera  
FPGAs are integrated into processors, mostly for data center and telecom applications  
Intel promotes tight integration of the ASIC and FPGA



# AMD & Xilinx

## AMD Completes Acquisition of Xilinx

- Transaction creates high-performance and adaptive computing leader
- AMD to offer industry's strongest portfolio of leadership CPUs, GPUs, FPGAs and Adaptive SoCs to address approximately \$135 billion market opportunity

SANTA CLARA, Calif. 02/14/2022

AMD (NASDAQ: AMD) today announced the completion of its acquisition of Xilinx in an all-stock transaction. The acquisition, originally announced on October 27, 2020, creates the industry's high-performance and adaptive computing leader with significantly expanded scale and the strongest portfolio of leadership computing, graphics and adaptive SoC products. AMD expects the acquisition to be accretive to non-GAAP margins, non-GAAP EPS and free cash flow generation in the first year.

"The acquisition of Xilinx brings together a highly complementary set of products, customers and markets combined with differentiated IP and world-class talent to create the industry's high-performance and adaptive computing leader," said AMD President and CEO Dr. Lisa Su. "Xilinx offers industry-leading FPGAs, adaptive SoCs, AI engines and software expertise that enable AMD to offer the strongest portfolio of high-performance and adaptive computing solutions in the industry and capture a larger share of the approximately \$135 billion market opportunity we see across cloud, edge and intelligent devices."

Former Xilinx CEO Victor Peng will join AMD as president of the newly formed Adaptive and Embedded Computing Group (AECG). AECG remains focused on driving leadership FPGA, Adaptive SoC and software roadmaps, now with the additional scale of the combined company and the ability to offer an expanded set of solutions including AMD CPUs and GPUs.

"The rapid expansion of connected devices and data-intensive applications with embedded AI are driving the growing demand for highly efficient and adaptive high-performance computing solutions," said Victor Peng. "Bringing AMD and Xilinx together will accelerate our ability to define this new era of computing by providing the most comprehensive portfolio of adaptive computing platforms capable of powering a wide range of intelligent applications."

# Intel FPGAs – target Applications



Artificial Intelligence



Data Analytics



Network Functions Virtualization



Financial

# ASIC/SoC – FPGA's in the Cloud

- Today, nearly every new server in Microsoft datacenters integrates an FPGA into a unique distributed architecture, which creates an interconnected and configurable

Project Catapult is transforming cloud computing

We are living in an era where information grows exponentially and creates the need for massive computing power to process that information. At the same time, advances in silicon fabrication technology are approaching theoretical limits, and [Moore's Law](#) has run its course. Chip performance improvements no longer keep pace with the needs of cutting-edge, computationally expensive workloads like software-defined networking (SDN) and artificial intelligence (AI). To create a faster, more intelligent cloud that keeps up with growing appetites for computing power, datacenters need to add other processors distinctly suited for critical workloads.



[first hardware accelerated model released May 7, 2018!](#)

# Amazon EC2 F1 Instances

Enable faster FPGA accelerator development and deployment in the cloud

[Get Started with F1 Instances](#)

Amazon EC2 F1 instances use FPGAs to enable delivery of custom hardware accelerations. F1 instances are easy to program and come with everything you need to develop, simulate, debug, and compile your hardware acceleration code, including an FPGA Developer AMI and supporting hardware level development on the cloud. Using F1 instances to deploy hardware accelerations can be useful in many applications to solve complex science, engineering, and business problems that require high bandwidth, enhanced networking, and very high compute capabilities. Examples of target applications that can benefit from F1 instance acceleration are genomics, search/analytics, image and video processing, network security, electronic design automation (EDA), image and file compression and big data analytics.

## Unleash Your Data Center

For Intel® Xeon® CPU with FPGAs



- Intel FPGAs burst open these bottlenecks with a combination of microarchitectural flexibility, massive parallelism, huge data bandwidth, and rapid reconfigurability. As workloads and traffic pattern shift, Intel FPGAs can anticipate needs and bring optimized hardware acceleration to bear on the critical points. Read on to see how Intel FPGAs can burst the bottlenecks in the applications most vital to you.

# Copiat/Plagiat/Cheating policy

- Daca predai munca sau parti din munca altcuiva esti vinovat de frauda. Acest lucru se aplica la orice material de laborator, examen, cerinta predata, etc.
- Esti vinovat daca ajuti pe cineva sa triseze!
- E OK sa colaborezi si sa schimbi idei!
- Nu postati materiale predate/solutii public!
- La laborator problemele de copiat si colaborare prost inteleasa pot primi puncte NEGATIVE!
- La examen – picat cu referat in vederea exmatricularii!
- Toate cazurile sa aleg cu referat la decanat!

# Întrebări?

# Hands-on Session

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**Enough Talking Let's Get To It  
!!Brace Yourselves!!**

