

The image features a title card for 'EDA Playground Tutorial'. The background is composed of three main color sections: a light blue area on the left, a light pink area on the right, and a large white central area. A dark blue, curved shape at the bottom frames the white area. The title text is centered in the white area in a bold, dark blue font.

# **EDA PLAYGROUND TUTORIAL**

# CONȚINUT

**1. CREEAREA UNUI  
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**2. PERSONALIZARE**

**3. ÎNTELEGerea  
LAYOUT-ULUI**

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**5. SALVAREA  
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**9. EPWAVE**

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**CAPITOLE  
AVANSATE**

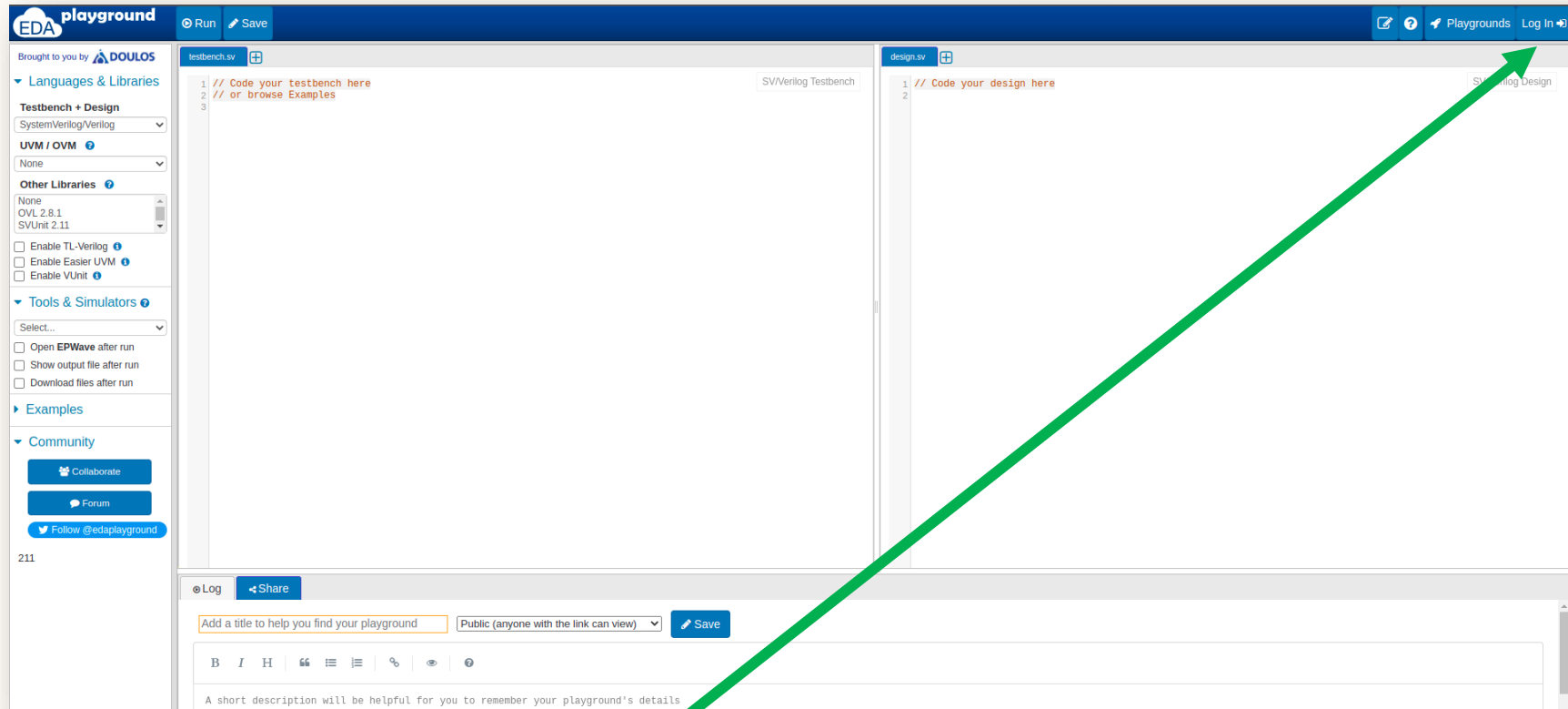
**11. OPTIUNI DE  
COMPILARE & RUN**

**12. COVERAGE  
RAPORT**

## 1.Crearea unui cont

3

1.Dacă folosești acest [link](#) vei ajunge aici:



2.Un prim pas ar fi înregistrarea unui cont.

## 1.Crearea unui cont

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Ideal, vei folosi email-ul de student pentru a avea acces la toate resursele EDA disponibile.

Email (Company or Institution):

To prevent your validation from being disabled, please supply your company or institution email address. Access will not be granted to freely available email addresses (eg gmail).

Password:  At least one upper and lowercase character, at least one number, at least one special character and at least 8 characters in length

Company or Institution name:

First name:

Last name:

Job Title:

City:

Country:

Products.

I have read and accept responsibility for compliance with the LIMITED USE terms above for usage associated with my VALIDATED USER ID.

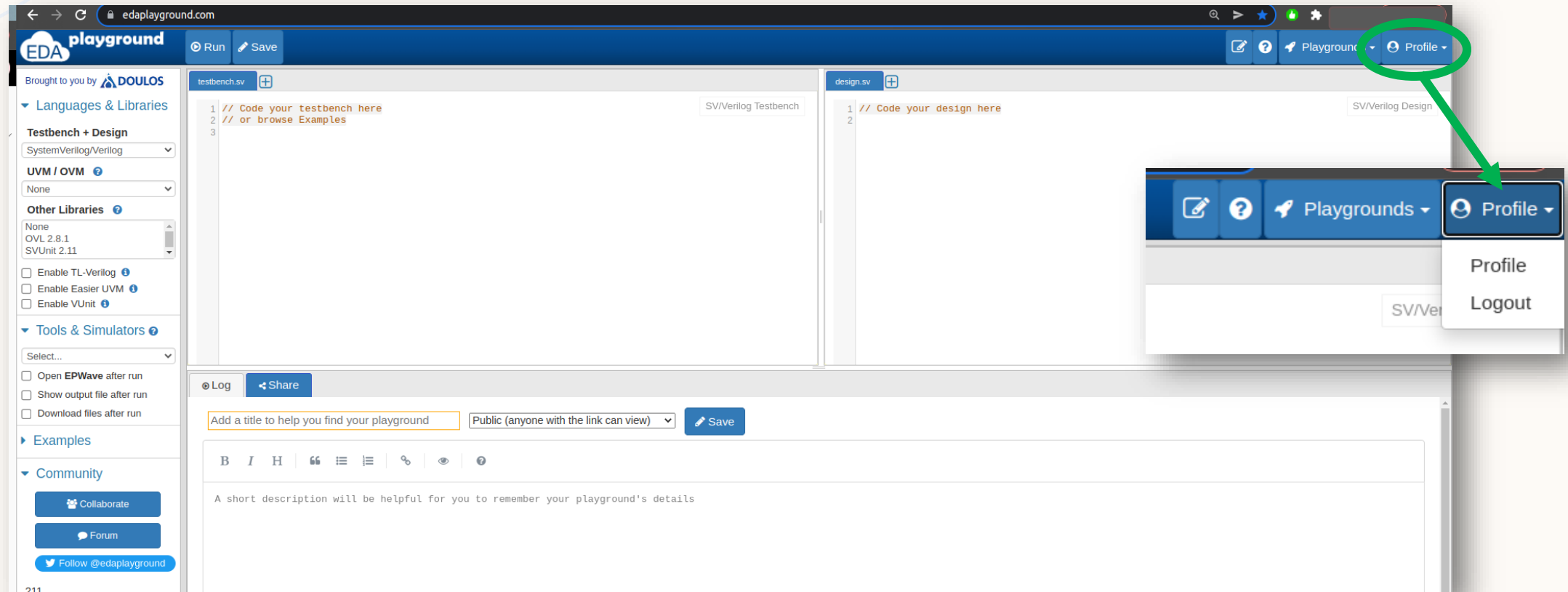
Problems registering your account?

Please contact Matthew Taylor ([getedaplayground@gmail.com](mailto:getedaplayground@gmail.com)) and/or check out the [forum](#)

## 1.Crearea unui cont - final

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După confirmarea email-ului și logare, am ajuns aici:



## 2. Personalizare

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1. Din pagina inițială, de la *Profile*, *Profile* se ajunge în pagina de personalizare a playgraund-urilor.

2. Poți să deschizi wave-ul în altă filă, dar pentru început recomand să nu se bifeze opțiunea.

3. De aici se poate trece în modul dark (tema întunecată).  
\*eu nu-l folosesc pentru că e urât\*

The screenshot shows the EDA Playground website. The header is blue with the EDA Playground logo and buttons for 'Run' and 'Save'. The main content area is white and contains sections for 'Your Details' and 'Playground Options'. The 'Your Details' section has fields for 'Company or Institution name', 'First name', 'Last name', 'Job Title', 'City', and 'Country'. The 'Playground Options' section has checkboxes for 'Alert before leaving EDA Playground when code has been modified' and 'Open EPWave waveforms on a separate page after run', and dropdown menus for 'Editor Mode' and 'Screen (beta)'. There are 'Save Details' and 'Logout' buttons at the bottom.

3.Întelegerea layout-ului.

1.Butonul de editor duce la un link cu diverse keyboard shortcuts.

2. Butonul cu semnul întrebării duce la o pagină de help.

EDA Playground Keyboard Shortcuts

GUI

Option	Description
CTRL-Enter	Run
CTRL-S	Save playground

Editor

Basic

Option	Description
CTRL-Z	Undo
CTRL-Y	Redo
CTRL-A	Select all
CTRL-C	Copy
CTRL-X	Cut
CTRL-V	Paste
CTRL-D	Delete line

Find/Replace

Option	Description
CTRL-F	Find
CTRL-G	Find next
CTRL-SHIFT-G	Find previous
CTRL-SHIFT-R	Replace

Selecting/Navigation

Option	Description
SHIFT-click	select region
CTRL-click	Edit multiple lines
ALT-click-drag	column editing
CTRL-left	jump left one word
CTRL-right	jump right one word
CTRL-SHIFT-up	Select to start of the file
CTRL-SHIFT-down	Select to end of the file

Formatting

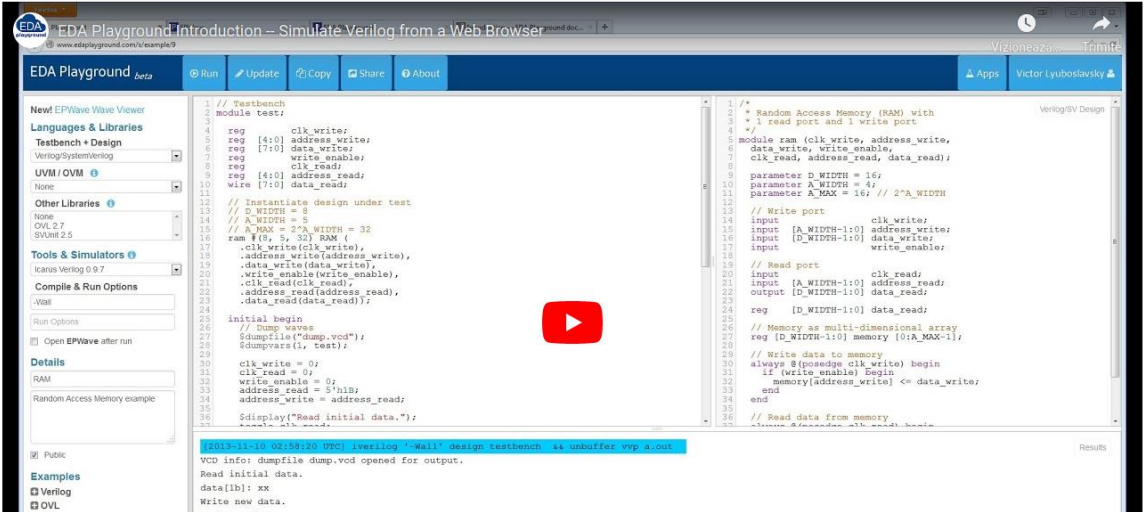
Option	Description
CTRL-/	comment/uncomment selection
CTRL-]	indent selection
CTRL-[	outdent selection

EDA Playground Documentation

Table of Contents:

- [FAQ](#)
- [EDA Playground Help](#)
- [Logging in](#)
- [Tutorial](#)
- [Settings & Buttons](#)
- [Yosys Circuit Diagrams](#)
- [Tutorials and Code Examples](#)
- [Privacy Policy](#)

EDA Playground on YouTube - Tutorials for Verilog, SystemVerilog, UVM, and VHDL, interview questions, news and features, etc.



### 3.Întelegerea layout-ului.

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The screenshot shows the EDA Playground web interface. It is divided into several sections:

- Left Sidebar:** Contains settings for 'Languages & Libraries' (Testbench + Design, UVM / OVM, Other Libraries) and 'Tools & Simulators' (Select..., Open EPWave after run, Show output file after run, Download files after run). There are also links for 'Examples' and 'Community'.
- Top Bar:** Includes 'Run' and 'Save' buttons, and links for 'Playgrounds' and 'Log In'.
- Main Editor:** Split into two panes. The left pane is labeled 'testbench.sv' and contains a placeholder for testbench code. The right pane is labeled 'design.sv' and contains a placeholder for design code.
- Bottom Bar:** Includes a 'Log' button (circled in green) and a 'Share' button. Below these is a text input field for a title, a dropdown for visibility (set to 'Public'), and a 'Save' button.
- Log Panel (Bottom Right):** Displays the execution log, showing a timestamp, a command executed, and a warning message about an unsupported Linux kernel.

Annotations in blue boxes explain the sections:

- 2. Partea de testbench.**  
\*unde se scrie codul pentru testarea DUT\*
- 1. Partea de design.**  
\*unde se scrie codul sursă\*
- 3. Partea de compilare si simulare.**  
\*unde selectezi/deselectezi opțiuni\*
- 4. Partea de vei vedea mesajele simulării**

The log panel shows the following output:

```
[2023-10-23 09:07:56 UTC] chmod +x run.bash; sed -i -e 's/\r//g' run.bash; ./run.bash
Ce mancam azi bun?

Warning-[LINUX_KRNL] Unsupported Linux kernel
Linux kernel '5.4.0-153-generic' is not supported.
Supported versions are 2.4* or 2.6*.

Chronologic VCS (TM)
Version S-2021.09 -- Mon Oct 23 05:07:57 2023

Copyright (c) 1991 - 2021 Synopsys, Inc.
```



## 4. Adăugarea de fișiere - design

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The screenshot displays the EDA Playground web interface. On the left, there is a sidebar with sections for 'Languages & Libraries', 'Tools & Simulators', 'Examples', and 'Community'. The main workspace is divided into two panels: 'testbench.v' and 'design.v'. The 'design.v' panel is active, showing a code editor with the following content:

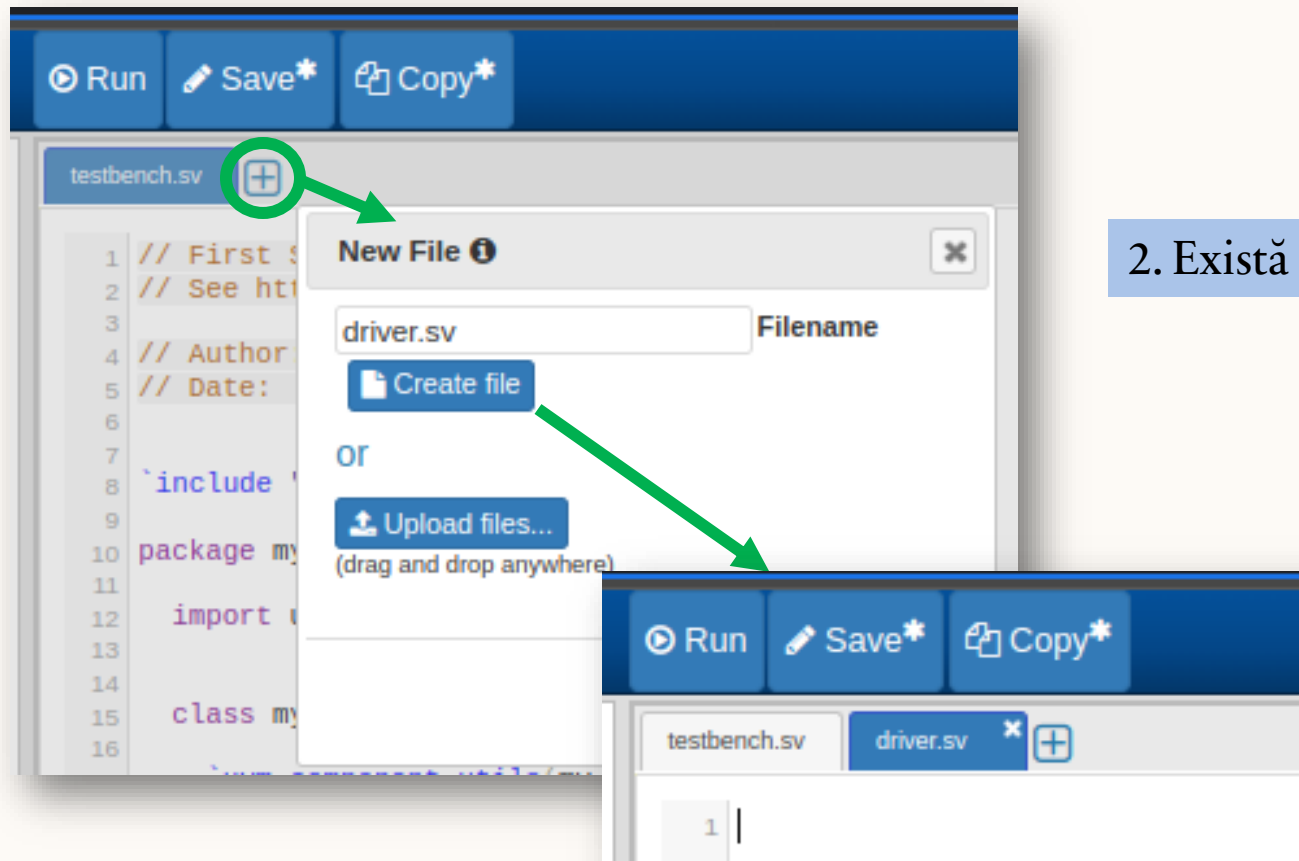
```
1 // Code your design here
2
3
```

A 'New File' dialog box is open over the 'design.v' panel. The dialog has a 'Filename' input field containing 'fifo.v' and a 'Create file' button, which is circled in green. Below the input field, there is an 'or' label and an 'Upload files...' button with the instruction '(drag and drop anywhere)'. A green arrow points from the 'Create file' button to the 'design.v' tab in the file manager at the bottom. The file manager shows three tabs: 'design.v', 'fifo.v', and 'port\_fsm.v'. The 'fifo.v' tab is selected, showing the following code:

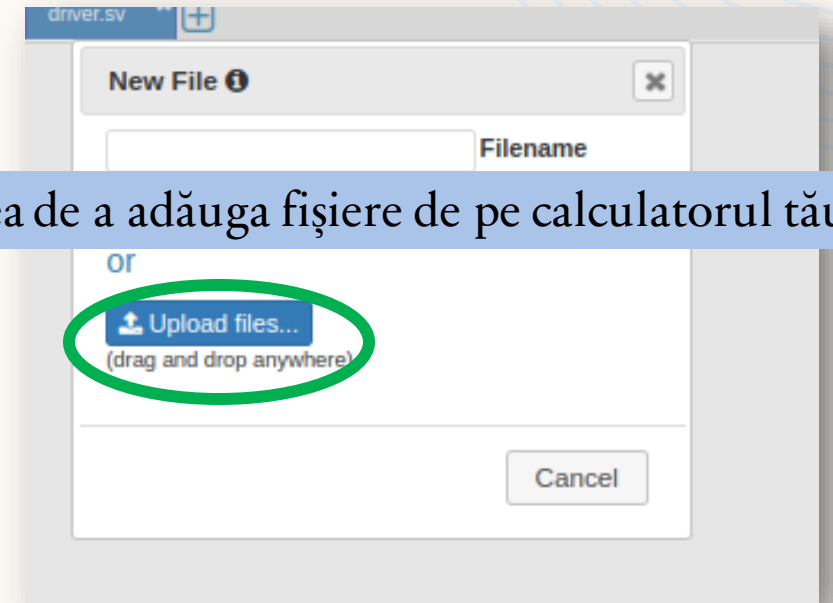
```
1 `include "fifo.v"
2 `include "port_fsm.v"
3
4 module switch (
5     clk,
6     reset,
```

#### 4. Adăugarea de fișiere - testbench

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2. Există și opțiunea de a adăuga fișiere de pe calculatorul tău.

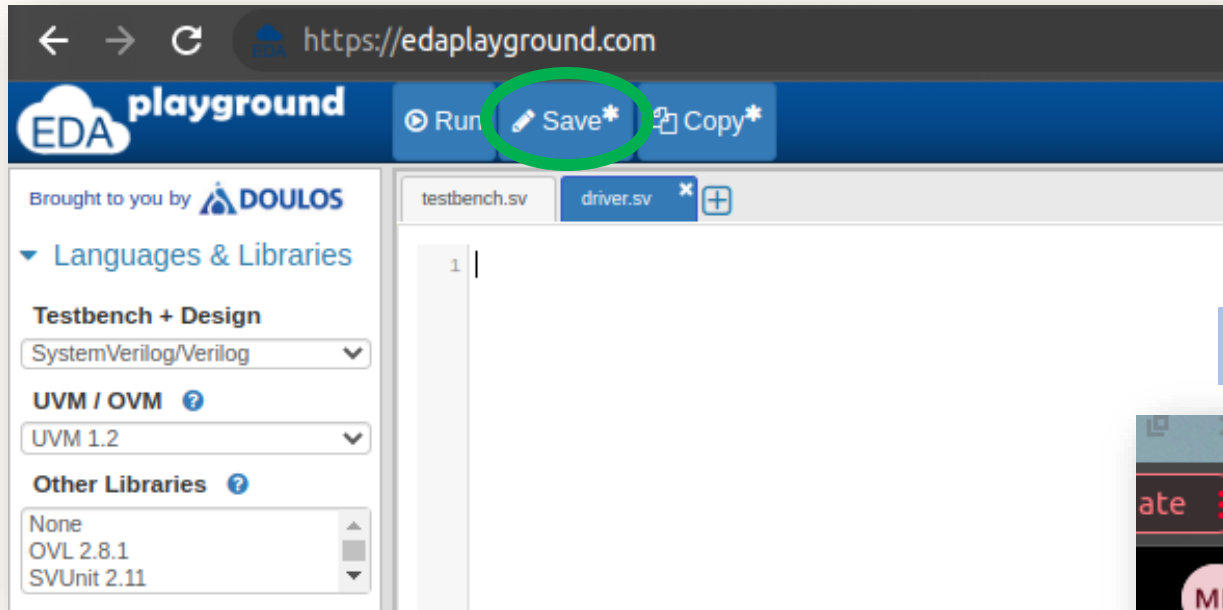


1. Adăugarea se face la fel ca și în partea de design.

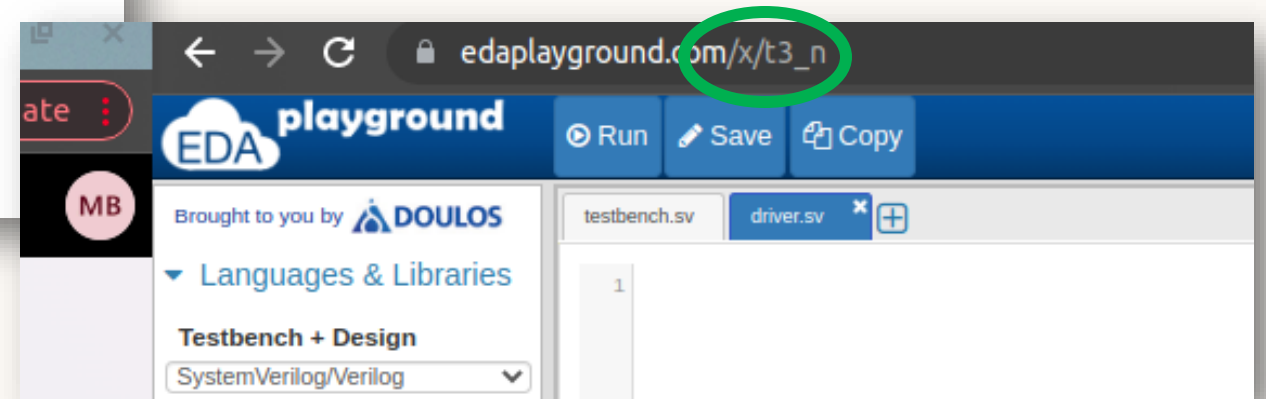
## 5. Salvarea playground-ului

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1. Salvarea se face apăsând butonul *Save* sau din tastatură : *CTR+s*.



2. După prima salvare playground-ul tău va primi un link.



## 6. Vizibilitatea playground-ului

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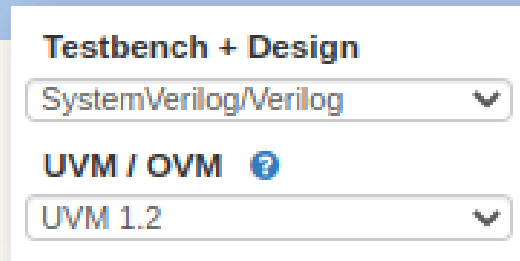
1. Cât timp ai linkul unui playground și acesta nu este privat, poți accesa acel playground.

The screenshot displays the EDA Playground web interface. On the left, there's a sidebar with 'Languages & Libraries' and 'Tools & Simulators' sections. The main area shows a code editor with 'testbench.sv' and 'driver.sv' files. A sharing overlay is visible, showing '0 views and 0 likes' and a dropdown menu for visibility settings. The dropdown menu is open, showing options: 'Private (only you can view)', 'Public (anyone with the link can view)', 'Published (will appear in search results)', and 'Private (only you can view)'. A green arrow points from a text box to the 'Public' option. Below the sharing overlay, there's a 'Share' button and a 'demo' link. A green circle highlights the 'Private (only you can view)' option in the dropdown menu.

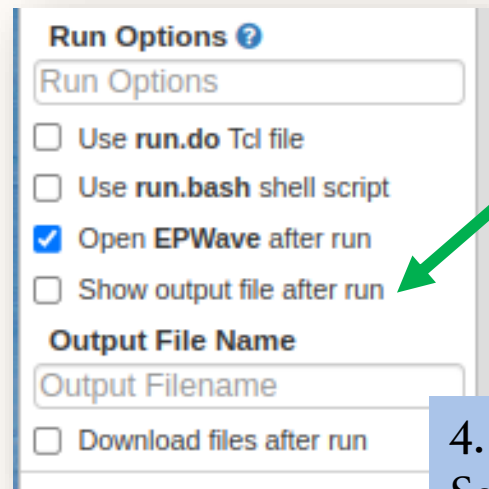
2. Poți selecta cine poate să îți vadă munca.

## 7. Configurarea simulării

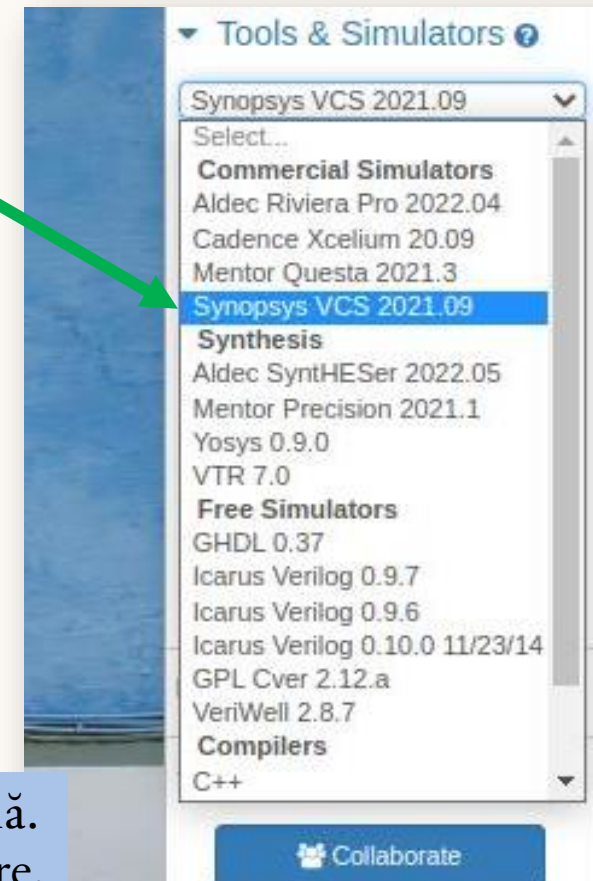
1. Înainte de a simula, asigură-te că ai selectat limbajul de programare SystemVerilog/Verilog (și biblioteca UVM 1.2, dacă e cazul).



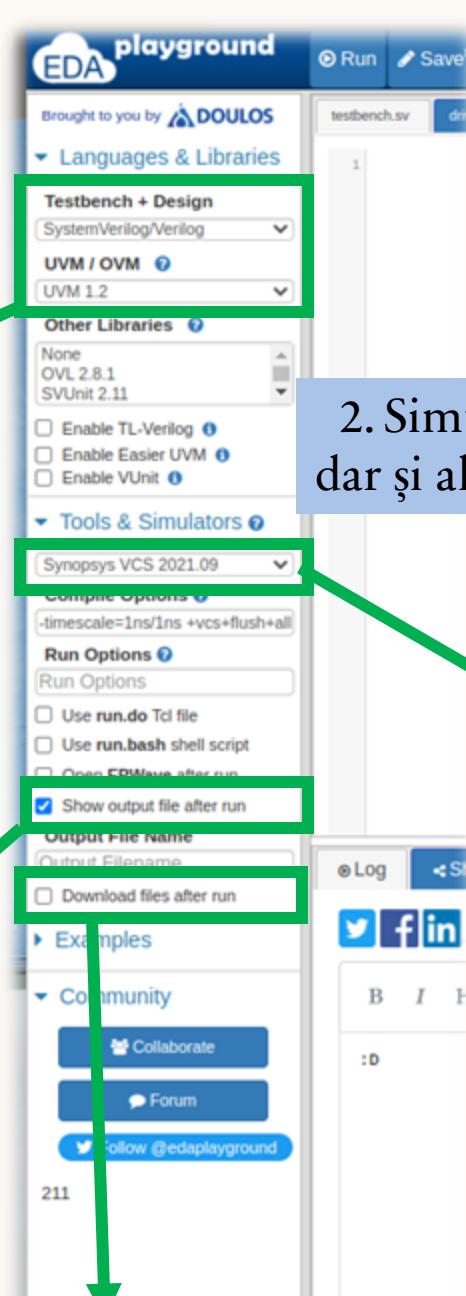
3. Opțiunea *Show output file after run* se bifează singură și cauzează o eroare, debifează-o. Cam așa :



2. Simulatorul Synopsys VCS este cel prezent, dar și alte simulatoare sunt bune.



4. Opțiunea de *Download files after run* este utilă. Se descarcă un .zip cu toate fișierele după rulare.



0.Înainte de a rula, simt nevoia sa amintesc că pentru a vedea un EPWave după simulare e nevoie de trei condiții:

```
initial begin
    $dumpfile("dump.vcd"); $dumpvars;
end
```

1. Există această bucată de cod în testbench.

**Run Options ?**

Run Options

- ☐ Use **run.do** Tcl file
- ☐ Use **run.bash** shell script
- ☒ Open **EPWave** after run
- ☐ Show output file after run
- ☐ Download files after run

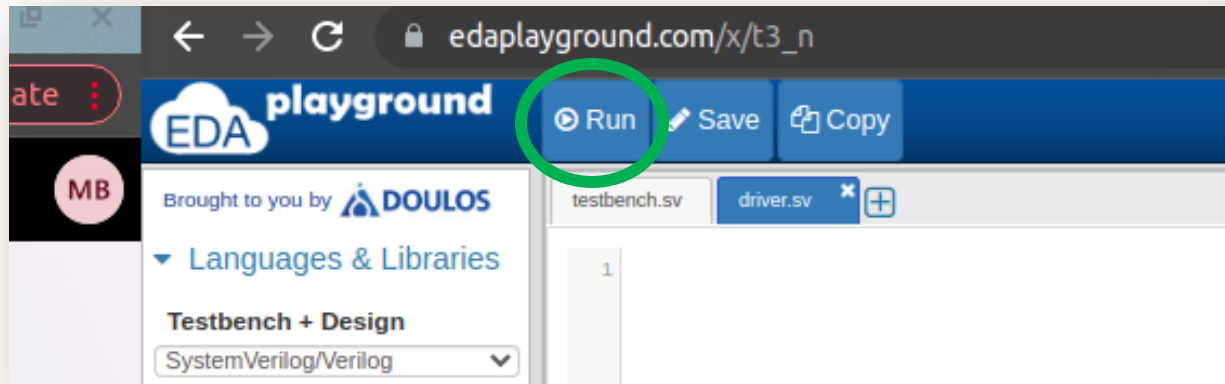
2. S-a bifat *EPWave* în Run Options.

```
$finish at simulation time          65
          V C S   S i m u l a t i o n   R e p o r t
Time: 65 ps
CPU Time:      0.740 seconds;      Data structure size:  0.0Mb
Mon Oct 23 07:06:04 2023
Finding VCD file...
./dump.vcd
[2023-10-23 11:06:04 UTC] Opening EPWave...
Done
```

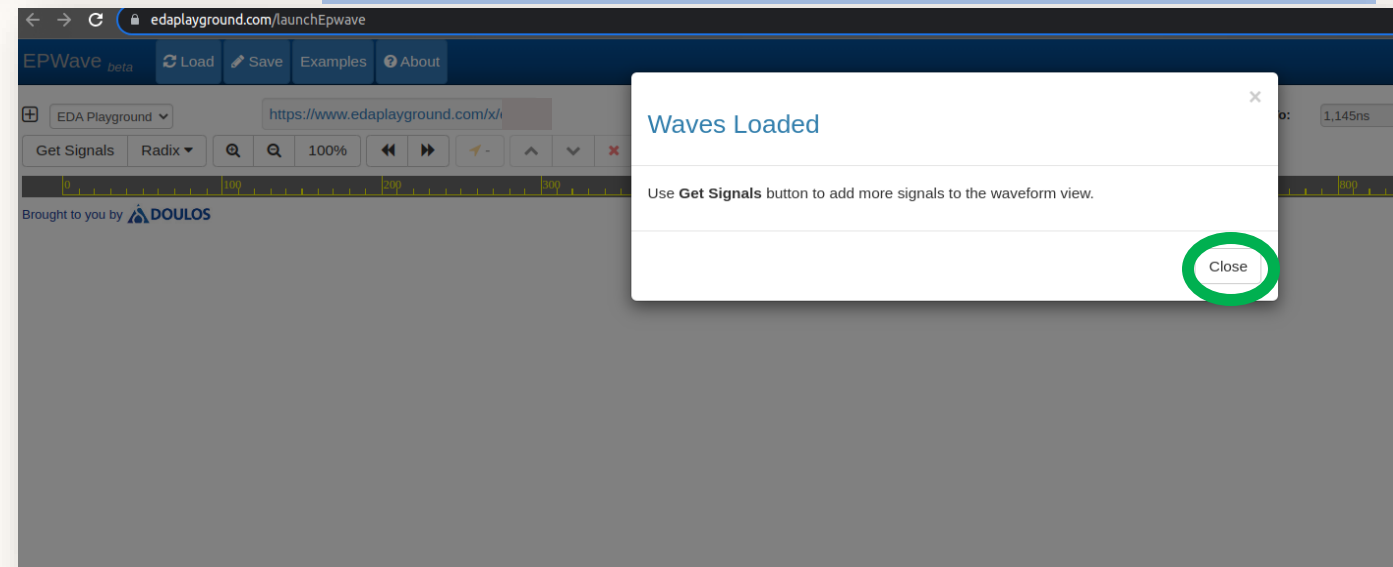
3. Nu există erori în cod.

## 8. Run

1. După scrierea codului (tutorialul nu acoperă partea asta) se ajunge la simulare. Rularea codului se face apăsând butonul *Run* sau din tastatură : *CTR+enter*.



2. Ideal, s-a deschis un EPWave la finalul simulării. E posibil să apară semnalele direct.



2.Radix e folosit pentru a alege în ce format se afișează datele.

1.Adăugarea semnalelor se face din *Get Signals*.

The screenshot displays the EPWave interface with the 'Get Signals to Display' dialog box open. The dialog box has two columns: 'Scope' and 'Signal Name'. The 'Scope' column contains the text 'test'. The 'Signal Name' column contains a list of signals: 'clk', 'd', 'q', 'qb', and 'reset'. At the bottom of the dialog box, there are three buttons: 'Append Selected' (circled in green), 'Append All', and 'Close'. A green arrow points from the 'Get Signals' button in the top toolbar to the dialog box. Another green arrow points from the 'Radix' dropdown in the top toolbar to an inset showing the radix options: 'Hex' (selected) and 'Binary'.

EPWave beta Load Save Examples About

EDA Playground https://www.edaplayground.com/x

From: 0ns To: 1,145ns

Get Signals Radix 100%

Brought to you by DOULOS

Get Signals to Display

Scope

test

Signal Name

clk  
d  
q  
qb  
reset

Append Selected Append All Close

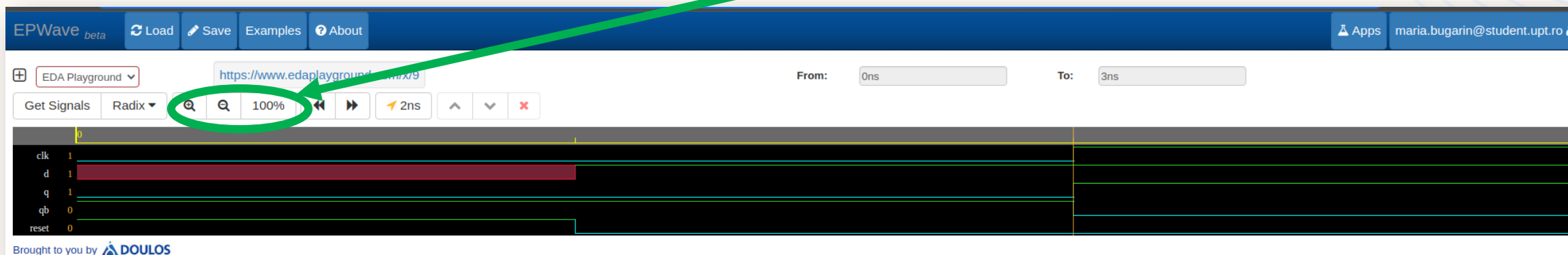
Get Signals Radix

Hex  
Binary

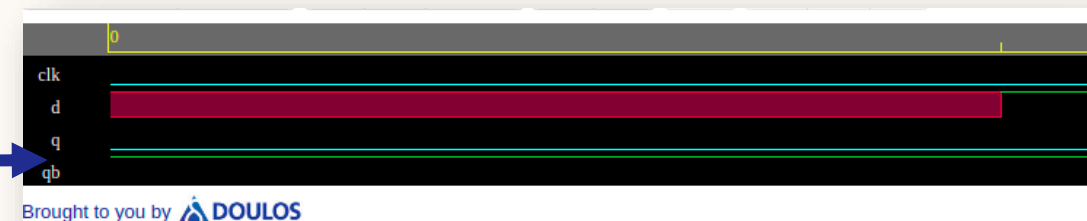
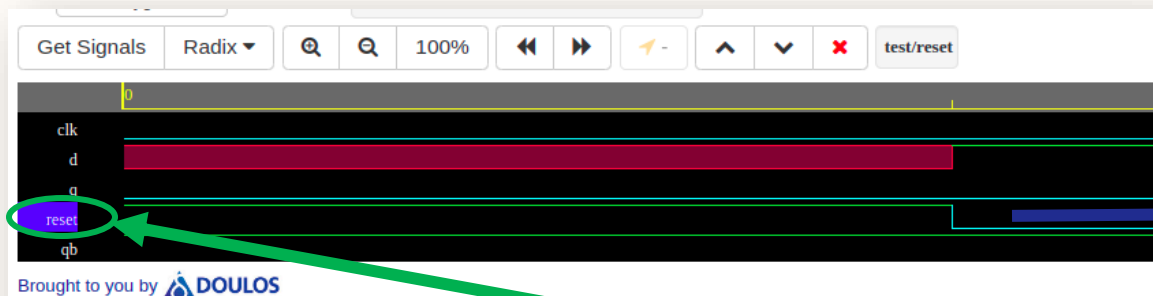


1. În final, apar semnale pe waveform.

2. Opțiuni de zoom.



3. Wave-ul este generat dintr-un exemplu clasic de D flip-flop disponibil [aici](#).



4. Un semnal poate fi șters selectându-l cu click-ul și apăsând *delete* de pe tastatură.

## 10. Playgrounds

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Eda Playground dispune de o varietate de exemple.

The screenshot shows the EDA Playground interface. At the top, there's a blue header with the EDA Playground logo, a 'Run' button, a 'Copy\*' button, and a 'Playgrounds' dropdown menu. Below the header, there's a sidebar on the left with 'Languages & Libraries' and 'Testbench + Design' sections. The main area is divided into two code editors: 'testbench.sv' and 'design.sv'. The 'testbench.sv' editor contains a testbench for a D flip-flop, and the 'design.sv' editor contains the D flip-flop design. Below the code editors, there's a search bar with the text 'Ceva frumos' and a 'Search all playgrounds' button. Below the search bar, there are filters for 'SystemVerilog/Verilog', 'Synopsys VCS 2021.09', and 'UVM'. There are also checkboxes for 'OVL', 'Easier UVM', 'Examples only', 'OSVVM', and 'UVVM'. Below the filters, there are 'Prev' and 'Next' buttons. The main content is a table of search results.

Name	Description	User	Modified	Likes	Views
D flip-flop	D flip-flop example	Victor Lyuboslavsky	2019/10/28 11:05am	96	214101
VHDL - Basic OR Gate	Simple VHDL example of an OR gate design and testbench.	Victor Lyuboslavsky	2019/10/28 11:05am	154	186767
Simple UVM Testbench	Example of a simple UVM testbench consisting of a single uvm_env class.	Victor Lyuboslavsky	2019/10/28 11:05am	35	88081
UVM Hello World	The Fastest Way to Get Started with UVM	Victor Lyuboslavsky	2019/10/28 11:06am	52	60595
RAM	Random Access Memory example	Victor Lyuboslavsky	2019/10/28 11:05am	30	46113
FSM	Finite State Machine example	Victor Lyuboslavsky	2019/10/28 11:06am	11	34824
SVUnit APB Slave example	Example of unit testing apb_slave RTL module with SVUnit.	Victor Lyuboslavsky	2019/10/28 11:05am	9	26777
SystemC Counter	A 4-bit up-counter design and testbench.	Victor Lyuboslavsky	2017/07/11 7:41am	9	24497
UVM Sequence-Driver	This example illustrates how to implement a unidirectional sequence-driver	Victor Lyuboslavsky	2019/10/28 11:06am	8	21595

## 11. Opțiuni compilare

În mod normal opțiunile se pun aici.

EDA playground

Brought to you by DOULOS

▼ Languages & Libraries

Testbench + Design

None

Other Libraries ?

None  
OVL 2.8.7  
SVUnit 1.11

☐ Enable TL-Verilog ?  
☐ Enable Easier UVM ?  
☐ Enable VUnit ?

▼ Tools & Simulators ?

Synopsys VCS 2021.09

**Compile Options ?**

**-timescale=1ns/1ns +vcs+flush+all**

**Run Options ?**

Run Options

☐ Use **run.do** Tcl file  
☒ Use **run.bash** shell script  
☐ Open **EPWave** after run  
☐ Show output file after run  
☐ Download files after run

EDA playground documentation

EDA Playground -> FAQ Site Contents Page

-onfinish stop Stops simulation and leaves the simulation kernel running.

-sv\_seed <integer> | random Seeds the root random number generator for SystemVerilog threads with either a user-specified integer, or a random number generated by Questa SIM.

### Synopsys VCS

#### Compile Options

##### VHDL

Option	Description
-h or -help	Lists descriptions of the most commonly used compile-time and runtime options.
-vhdl87	Enable backward compatibility for VHDL-87 syntax rules. (VHDL-93 syntax rules are the default.)
-xlm	Enable vhdl features beyond those described in lrm.
-f[file] optionsfile	Expand command line options from file optionsfile.
-psl	Enable psl assertions
-pslfile pslfile	specify psl assertion file pslfile
-vhdl08	Enable support for VHDL 2008 constructs.

##### SystemVerilog

Option	Description
-debug_access+all	enable all debug capability.
-f <filename>	Specifies a file that contains a list of pathnames to source files and compile-time options.
-h or -help	Lists descriptions of the most commonly used compile-time and runtime options.
-timescale=<time_unit>/<time_precision>	If only some source files contain the `timescale compiler directive and the ones that don't appear first on the vcs command line, use this option to specify the time scale for these source files.

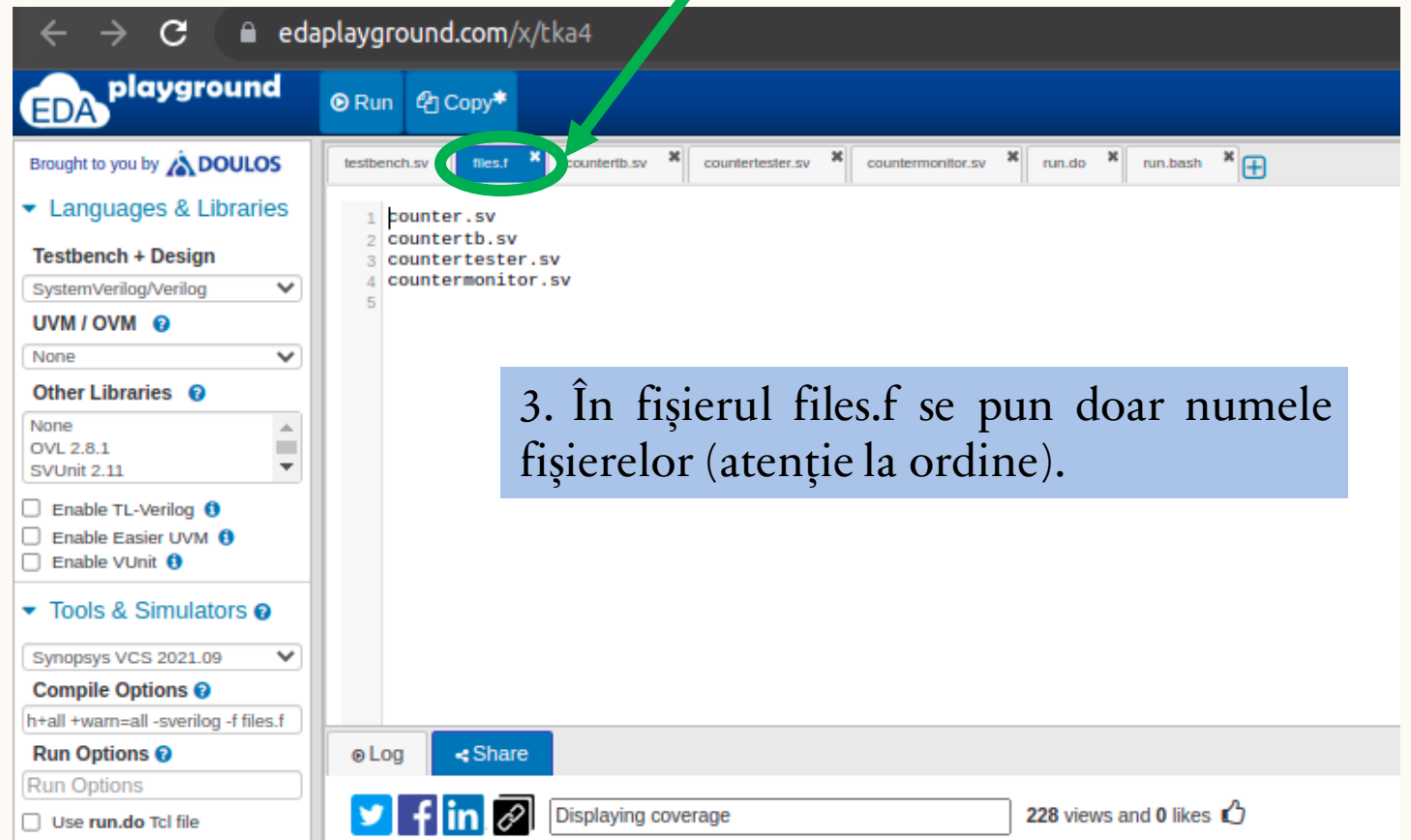
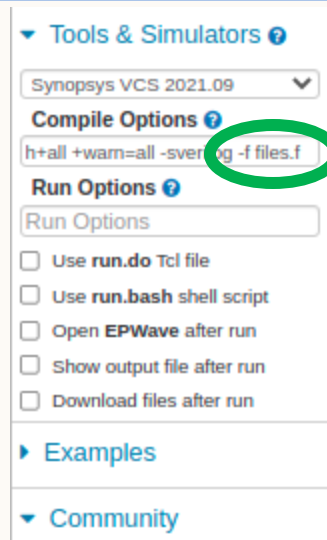
[Link](#) spre pagină cu opțiunile de compilare pentru fiecare simulator.

## 11. Opțiuni compilare – files.f

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1. Exisă posibilitatea de a alege **ordinea de compilare** a fișierelor dintr-un fișier *files.f*.

2. Opțiunea de compilare este "-f files.f"



3. În fișierul *files.f* se pun doar numele fișierelor (atenție la ordine).

## 11. Opțiuni run

În mod normal opțiunile se pun aici.

EDA playground

Brought to you by DOULOS

▼ Languages & Libraries

Testbench + Design

None

Other Libraries ?

None  
OVL 2.8.1  
SVUnit 2.11

☐ Enable TL-Verilog ?  
☐ Enable Easier UVM ?  
☐ Enable VUnit ?

▼ Tools & Simulators ?

Synopsys VCS 2021.09

Compile Options ?

-timescale=1ns/1ns +vcs -push+all

**Run Options ?**

Run Options

☐ Use run.do Tcl file  
☒ Use run.bash shell script  
☐ Open EPWave after run  
☐ Show output file after run  
☐ Download files after run

### Synopsys VCS

#### Compile Options

##### VHDL

Option	Description
-h or -help	Lists descriptions of the most commonly used compile-time and runtime options.
-vhdl87	Enable backward compatibility for VHDL-87 syntax rules. (VHDL-93 syntax rules are the default.)
-xirm	Enable vhdl features beyond those described in lrm.
-f[file] optionsfile	Expand command line options from file optionsfile.
-psl	Enable psl assertions
-pslfile psfile	specify psl assertion file psfile
-vhdl08	Enable support for VHDL 2008 constructs.

##### SystemVerilog

Option	Description
-debug_access+all	enable all debug capability.
-f <filename>	Specifies a file that contains a list of pathnames to source files and compile-time options.
-h or -help	Lists descriptions of the most commonly used compile-time and runtime options.
-timescale=<time_unit>/<time_precision>	If only some source files contain the `timescale compiler directive and the ones that don't appear first on the vcs command line, use this option to specify the time scale for these source files.

#### Run Options

##### Language-independent

Option	Description
-h or -help	Lists descriptions of the most commonly used compile-time and runtime options.

##### SystemVerilog

Option	Description
+ntb_random_seed=<value>	Sets the seed value used by the top level random number generator at the start of simulation. The random(seed) system function call overrides this setting. The value can be any integer number.

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Created using Sphinx 1.8.6.

Link spre pagină cu opțiunile de compilare și rulare menționată anterior.

## 11. Opțiuni compilare și run

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1. Exisă opțiunea de a folosi fișiere proprii pentru configurarea compilării și simulării.

2. În mod normal opțiunile se pun aici.

3. Opțiunile scrise aici sunt ignorate la bifarea acestor opțiuni.

EDA playground

Brought to you by DOULOS

▼ Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM ?

None

Other Libraries ?

None

OVL 2.8.1

SVUnit 2.11

☐ Enable TL-Verilog ?

☐ Enable Easier UVM ?

☐ Enable VUnit ?

▼ Tools & Simulators ?

Synopsys VCS 2021.09

Compile Options ?

-timescale=1ns/1ns +vcs+flush+all

Run Options ?

Run Options

☐ Use run.do Tcl file

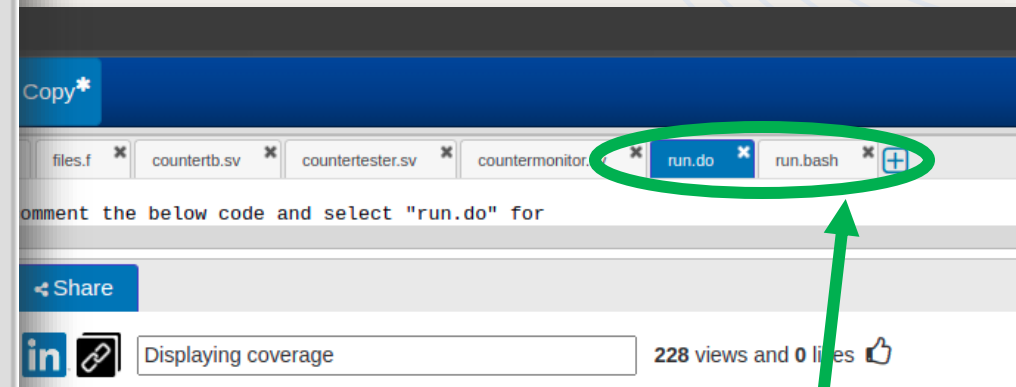
☒ Use run.bash shell script

☐ Open EPWave after run

☐ Show output file after run

☐ Download files after run

5. Synopsys este singurul care folosește run.bash.



4. Opțiunile de compilare și simulare pot fi puse în fișiere separate create de noi.

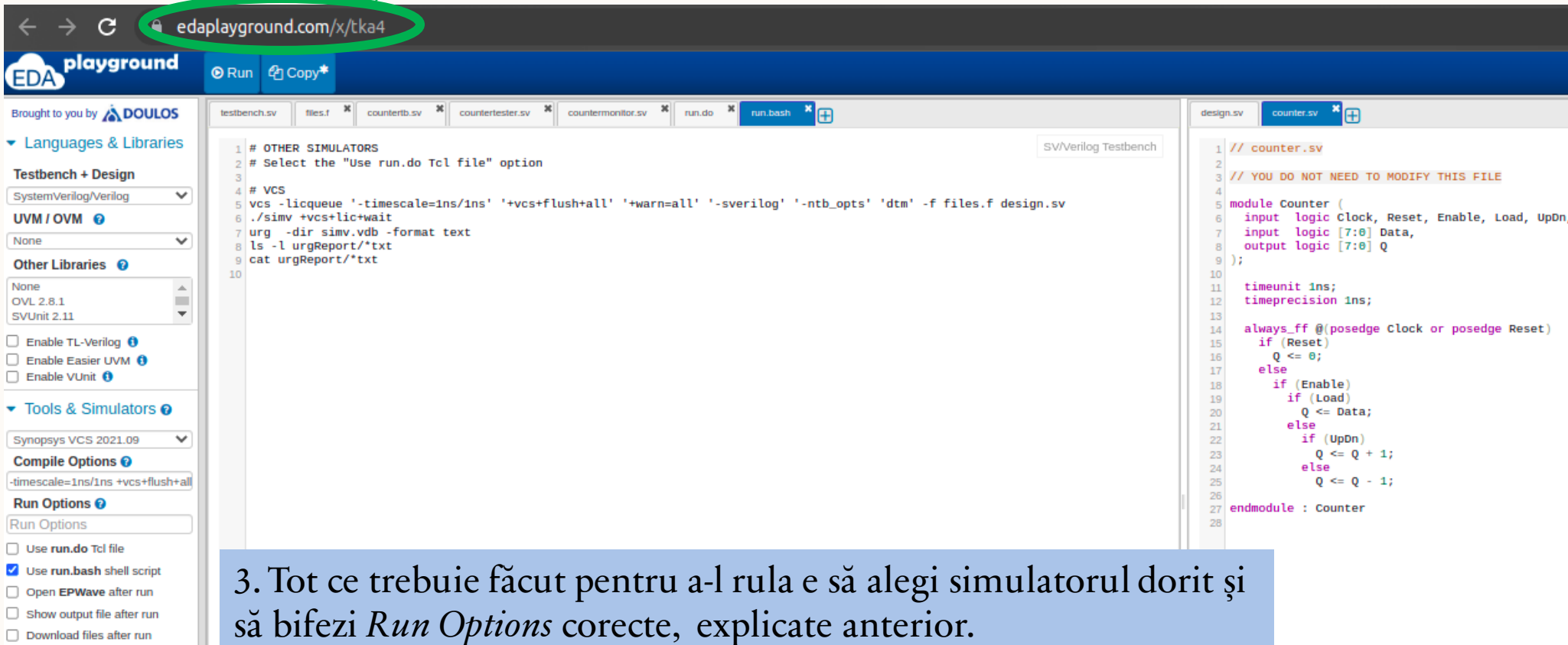
5. Asigură-te că ai bifat formatul de fișier folosit dacă ai ales să folosești run.do/run.bash.

## 12. Coverage raport

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1. Eda Playground dispune posibilitatea de a genera coverage report pe baza simulatorului ales.

2. Exemplul de la acest [link](https://edaplayground.com/x/tka4) arată opțiunile de compilare necesare pentru fiecare simulator.



3. Tot ce trebuie făcut pentru a-l rula e să alegi simulatorul dorit și să bifezi *Run Options* corecte, explicate anterior.

## 12. Coverage raport - UVM

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1. Comanda pentru a genera raport coverage cu UVM și Synopsys VCS.  
Diferența dintr-un raport coverage generat în SV și UVM este includerea fișierelor de UVM, adică "+incdir+\$UVM\_HOME/src \$UVM\_HOME/src/uvm sv \$UVM\_HOME/src/dpi/uvm\_dpi.cc -CFLAGS -DVCS".

The screenshot shows the EDA Playground web interface. The browser address bar displays `edaplayground.com/x/tka4`. The interface includes a top navigation bar with "Run" and "Copy" buttons. On the left, there is a sidebar with "Languages & Libraries" and "Tools & Simulators" sections. The "Languages & Libraries" section shows "Testbench + Design" with "SystemVerilog/Verilog" selected, and "UVM / OVM" with "None" selected. The "Tools & Simulators" section shows "Synopsys VCS 2021.09" selected. The "Compile Options" section shows `-timescale=1ns/1ns +vcs+flush+all`. The "Run Options" section shows `Run Options` and a checkbox for "Use run.bash shell script" which is checked. The main editor area displays a Verilog testbench in `testbench.v` and a counter module in `counter.v`. The testbench code is highlighted in a pink box and contains the following commands:

```
1 vcs -licqueue '-timescale=1ns/1ns' '+vcs+flush+all' '+warn=all' '-sverilog'
2 +incdir+$UVM_HOME/src $UVM_HOME/src/uvm sv
3 $UVM_HOME/src/dpi/uvm_dpi.cc -CFLAGS -DVCS -f files.f
4
5 ./simv +vcs+lic+wait
6 urg -dir simv.vdb -format text
7 ls -l urgReport/*txt
8 cat urgReport/*txt
```

The counter module code in `counter.v` is as follows:

```
1 // counter.v
2 // YOU DO NOT NEED TO MODIFY THIS FILE
3
4 module Counter (
5     input logic Clock, Reset, Enable, Load, UpDn,
6     input logic [7:0] Data,
7     output logic [7:0] Q
8 );
9
10 timeunit 1ns;
11 timeprecision 1ns;
12
13 always_ff @(posedge Clock or posedge Reset)
14     if (Reset)
15         Q <= 0;
16     else
17         if (Enable)
18             if (Load)
19                 Q <= Data;
20             else
21                 if (UpDn)
22                     Q <= Q + 1;
23             else
24                 Q <= Q;
```

2. Comanda este text, se poate copia pentru run.bash-ul tău.





**MULTUMESC!**