	Cache		Clock frequency	I MR	D MR	Miss Penalty
Computer A	WT	DM	2 GHz	10%	12%	80 ns
Computer B	WB	4-way SA	10% degradation	7%	10%	104 ns

Allocate in case of a miss

Load/store machines → 20% L/S instr.

CPI ideal = 2.3 c.c.

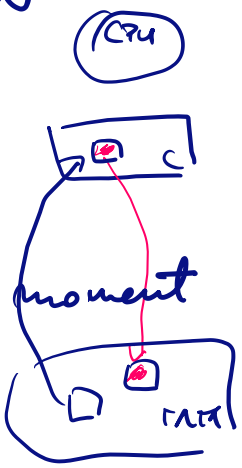
1 block = 16 words

BUS width = 2 words

MM access time = 10 ns

$\frac{16 \text{ words}}{2 \text{ words}}$ = 8 BUS acc.

80 ns to bring the block



Computer B → 30% of all blocks are dirty at any moment

$$\underbrace{\frac{16 \text{ words}}{2 \text{ words}}}_{\text{Allocation}} + 0.3 \underbrace{\frac{16 \text{ words}}{2 \text{ words}}}_{\text{8 BUS writes}} = 1.3 \times 8 = 10.4 \text{ bus acc.}$$

8 BUS reads

$$\text{Miss Penalty}_B = 10.4 \text{ bus acc.} \times 10 \text{ ns} = 104 \text{ ns}$$

$$\text{Clock cycle time}_A = \frac{1}{2 \cdot 10^9} \text{ s} = 0.5 \text{ ns}$$

$$\text{Clock cycle time}_B = 1.1 \times 0.5 = 0.55 \text{ ns}$$

$$\text{Miss Penalty}_A = \left\lceil \frac{80 \text{ ns}}{0.5 \text{ ns}} \right\rceil = 160 \text{ c.c.}$$

$$\text{Miss Penalty}_B = \left\lceil \frac{104\,ns}{0.5\,ns} \right\rceil = 208\ c.c.$$

$$\text{Misses per instruction}_A = IMR_A + 0.2 \times DMR_A =$$

$$= 0.1 + 0.2 \times 0.12 = 0.124$$

$$\text{Misses per instruction}_B = 0.07 + 0.2 \times 0.1 = 0.09$$

$$\text{Misses per instruction} = \text{Miss Rate} \times \text{Mem. acc per instr.}$$

$$\text{Memory accesses per instruction}_{A/B} = 1 + 0.2 = 1.2$$

$$\text{Miss Rate}_A = \frac{0.124}{1.2} = 0.1 = \underline{10\%}$$

$$\text{Miss Rate}_B = \frac{0.09}{1.2} = 0.075 = 7.5\%$$

$$AMAT_A = 0.5\,ns + 0.1 \times 160 \times 0.5\,ns = 8.5\,ns$$

$$AMAT_B = 0.55\,ns + 0.075 \times 208 \times 0.55\,ns = 9.13\,ns$$

$$CPU\,time_A = IC \times (2.3 + 0.124 \times 160) \times 5\,ns = 110.7\,ns \times IC$$

$$CPU\,time_B = IC \times (2.3 + 0.09 \times 208) \times 5.5\,ns = 115.61\,ns \times IC$$

$$AMAT = \underbrace{tac}_{\text{Clock cycle time}} + \text{Miss Rate} \times \underbrace{\text{Miss Penalty (time)}}_{\text{Miss Penalty (c.c)} \times \text{Clock cycle time}}$$

$$CPU\,time = IC \times \Big(CPI_{ideal} + \underbrace{\text{Memory acc per instr} \times \text{Miss Rate} \times \text{Miss Penalty (c.c)}}_{\text{Misses per instruction}} \Big) \times \text{Clock cycle time}$$