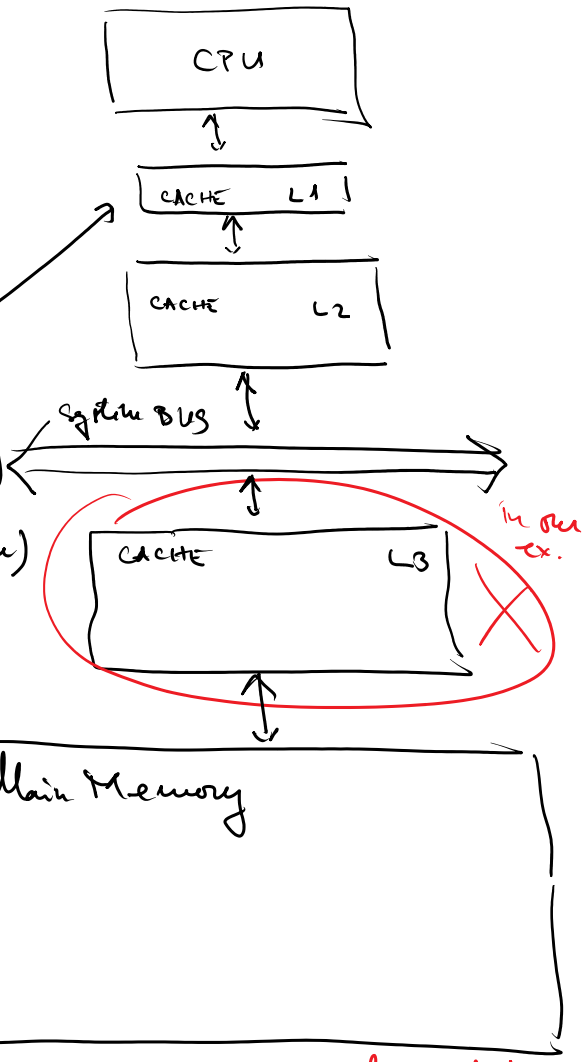
26 May 2020 11:53

3.5 Cache performance optimization

Miss Reduction → using multi-level caches



Example 1 (2-level cache system)

- CPI_{ideal} = 1.0 c.c. (all references hit the primary cache)
- Clock Rate = 4 GHz ⇒ $CCT = \frac{1}{4 \cdot 10^9 Hz} = \frac{1}{4} \cdot 10^{-9} s = \boxed{0.25\ ns}$
- MM access time = 100 ns (including all miss handling)
- Miss Rate per instruction = 2% (for the primary cache)
- How much faster will be the system (CPU + ~~CACHE~~)
  - 2nd level cache t_{ac} = 5 ns for each hit or a miss
  - miss rate per instr in 2nd level is 0.5%

$$\text{Miss Penalty}_{MM} = \left\lceil \frac{100\ ns}{0.25\ ns} \right\rceil = 400\ c.c.$$

$$CPU_{time} = IC \times CPI_{total} \times CCT$$ (CCT: does not change)

$$CPI_{total\ 1\text{-level}} = CPI_{ideal} + \text{Memory stall clock cycles}_{1\text{-level}} =$$
$$= 1.0 + \text{Miss Rate per instruction} \times \text{Miss Penalty}_{MM} =$$
$$= 1.0 + 0.02 \times 400 = 9\ c.c.$$

$$CPI_{total\ 2\text{-level}} = CPI_{ideal} + 1^{st}\text{ level stalls per instr.} + 2^{nd}\text{ level stalls per instr.} =$$
$$= 1 + 0.02 \times 20\ c.c. + 0.005 \times 400\ c.c. = 3.4\ c.c.$$

$$\text{Miss Penalty}_{2nd\ level} = \left\lceil \frac{5\ ns}{0.25\ ns} \right\rceil = 20\ c.c.$$

$$\frac{CPU\ time_{1\text{-level}}}{CPU\ time_{2\text{-levels}}} = \frac{9}{3.4} = \boxed{2.65}$$