Example

- MM = 4 GiB
- Byte addressable
- 1 word = 8B
- 1 block = 16 words
- Cache data size = 128 KiB
- Direct Mapping

a) Address Word format
b) Total cache size
c) Cache logic diagram

$MM_{size} = 4\,GiB = 2^2 \cdot 2^{30}\,B = 2^{32}\,B$ → Address word length.

Word offset => 1 word = 8B = 2^3 B → word offset length

1 block = 16 words = 2^4 w → Block offset length.

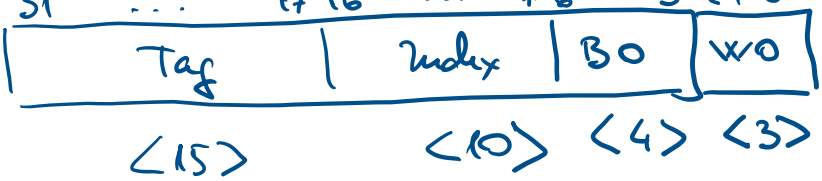
How many blocks / cache ?

128 KiB data cache = $2^7 \cdot 2^{10}\,B = 2^{17}\,B/cache = \frac{2^{17}\,B/cache}{2^7\,B/block} =$

1 block = $2^4 w = 2^3 \cdot 2^4\,B = 2^7\,B$

Index length = 2^{10} blocks / cache

a)



32 − 17 = 15

1B = 2^3 bits, 1 block = 2^7 B = $2^7 \cdot 2^3$ bits = 2^{10} bits = 1024

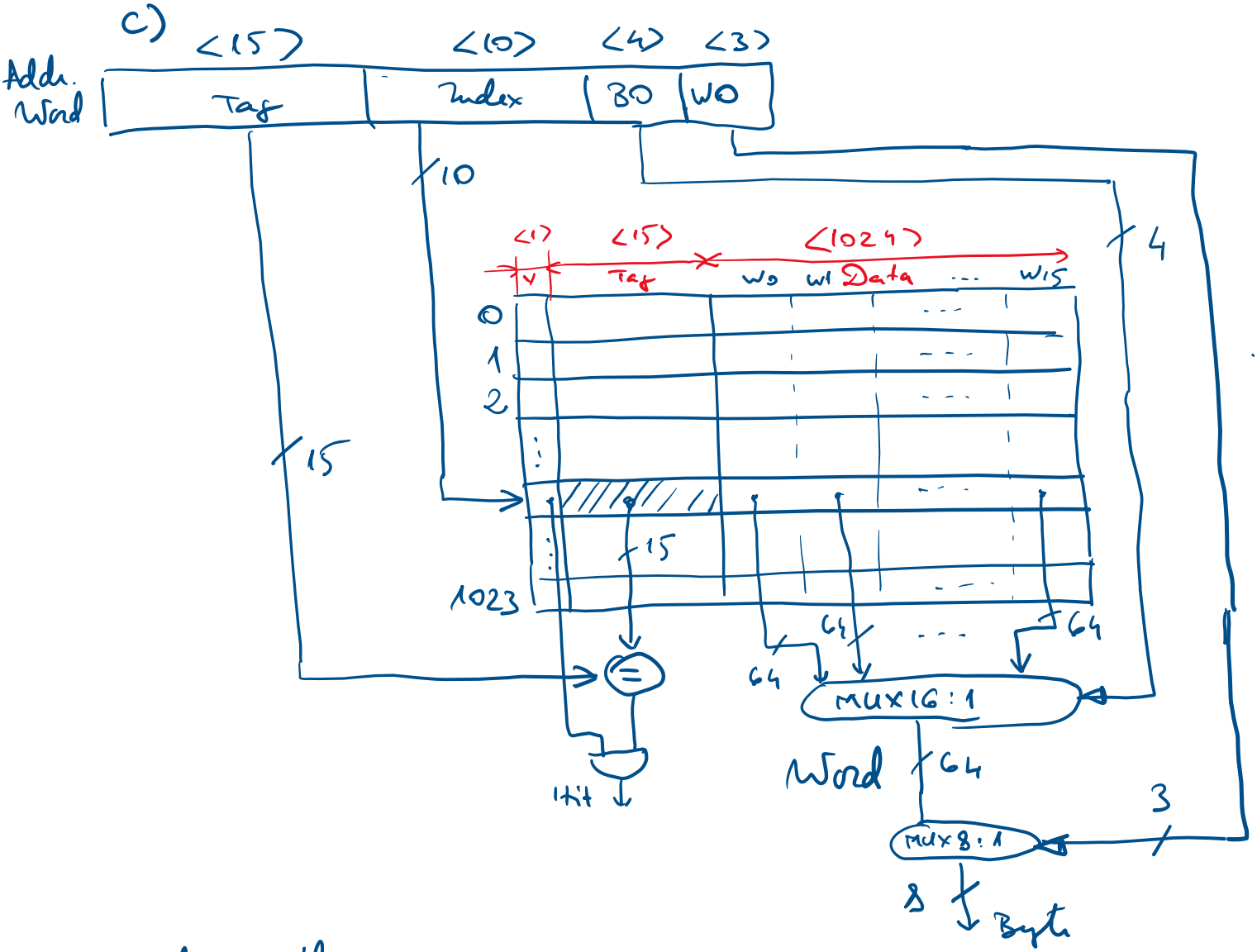
b) 1 cache line = 1 bit (V) + 15 bits (Tag) + 1024 bits (data)

1 cache line = $2B + 2^7 B$

Total cache size = $2^{10} \cdot (2B + 2^7 B) = 2 \cdot 2^{10} B + 2^7 \cdot 2^{10} B$

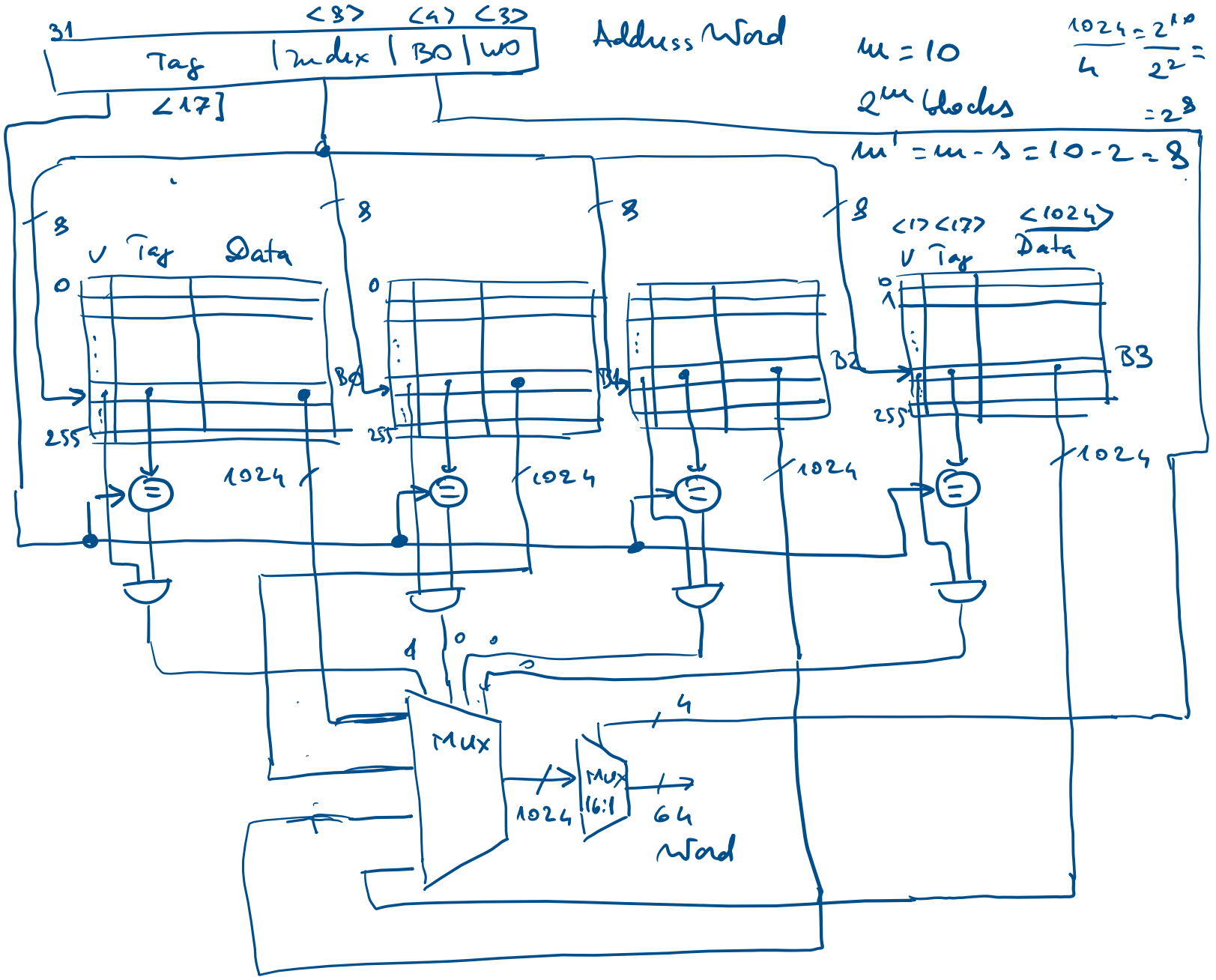
$= 2\,KiB + 128\,KiB = 130\,KiB$

c)



Only difference is 4-way SA

$k = 4 = 2^s \Rightarrow s = 2$


31
<8> <4> <3>
Tag
Index
B0
W0
<17>
Address Word
m = 10
2^m blocks
1024 = 2^10 / 4 = 2^2 = 2^8
m' = m - s = 10 - 2 = 8
8
V Tag Data
0
255
1024
B0
B1
B2
B3
<1> <17> <1024>
Data
MUX
1024
MUX 16:1
64
Word