Darío Caballero Polo

HAZARD ELIMINATION

ON A RISC-V32I 5-STAGE PIPELINED CPU

香港科技大學
THE HONG KONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

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Contents

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Introduction

Improve CPI of RISC-V32i 5-stage Pipelined CPU

Eliminate data & control stalls

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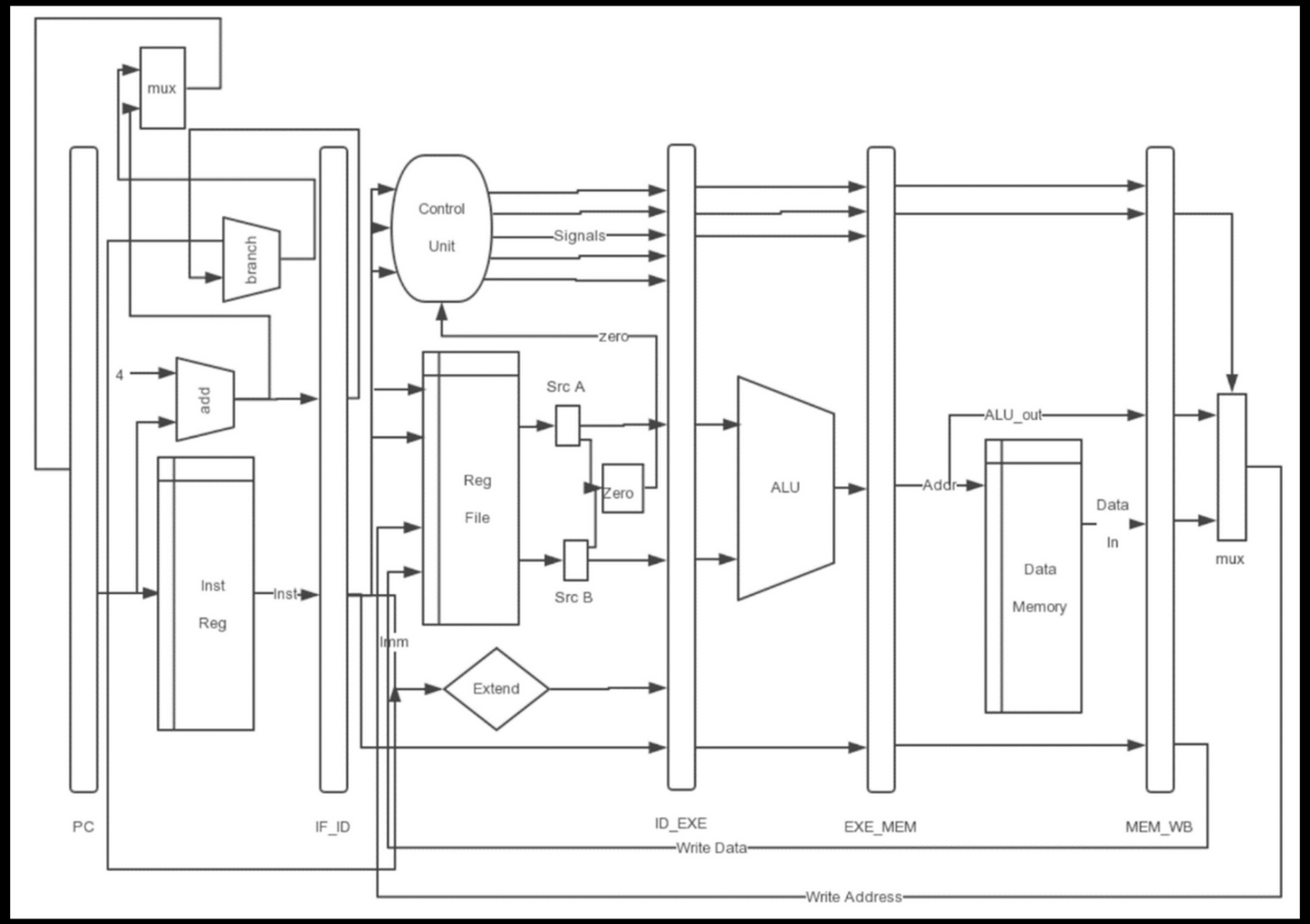

Related works

Linfeng Du RISC-V32i 5-stage Pipelined

Programmed in Verilog

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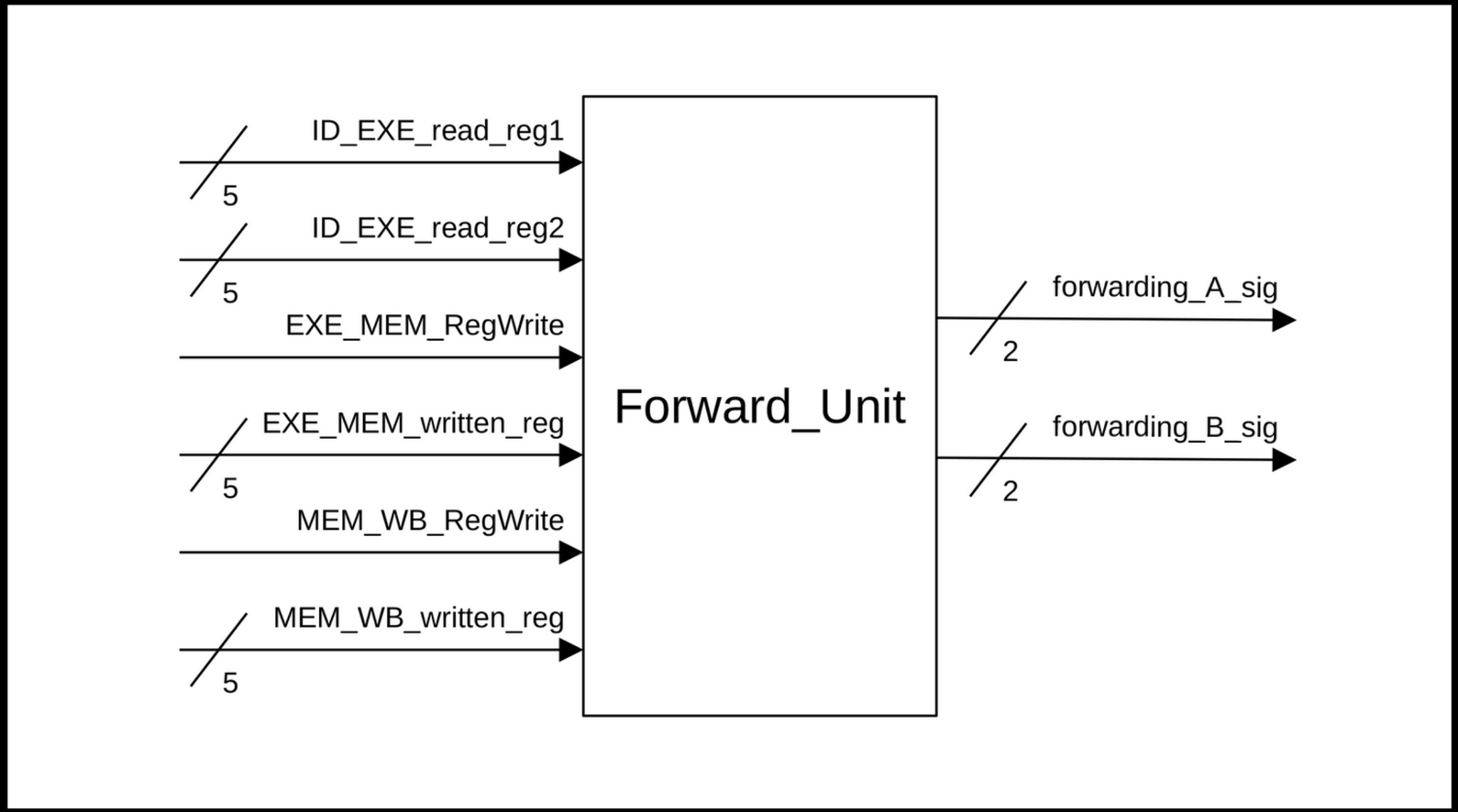
Methods

Data Forwarding

Branch Prediction

Data Forwarding

Forward Unit



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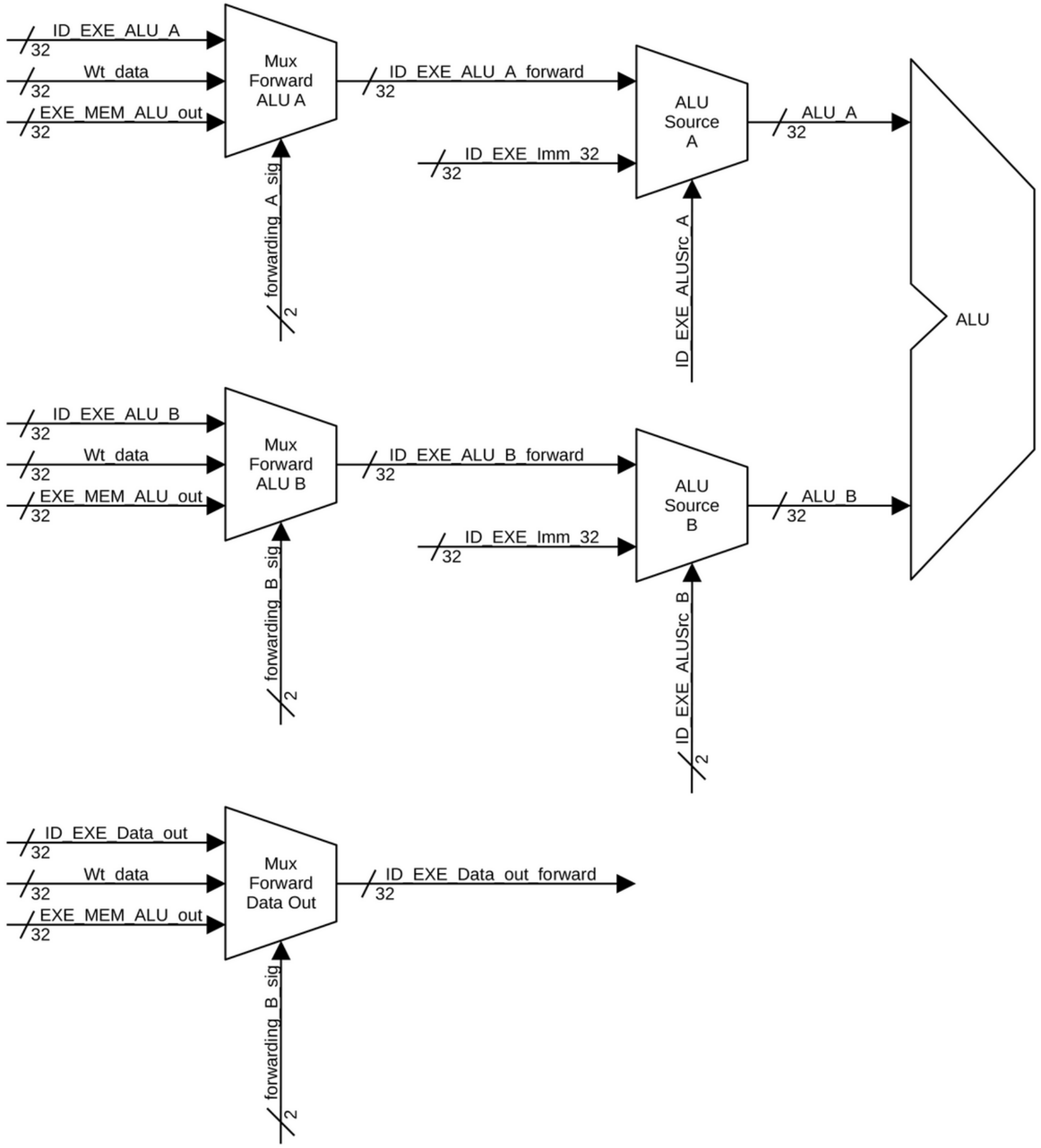
Data Forwarding

Multiplexing



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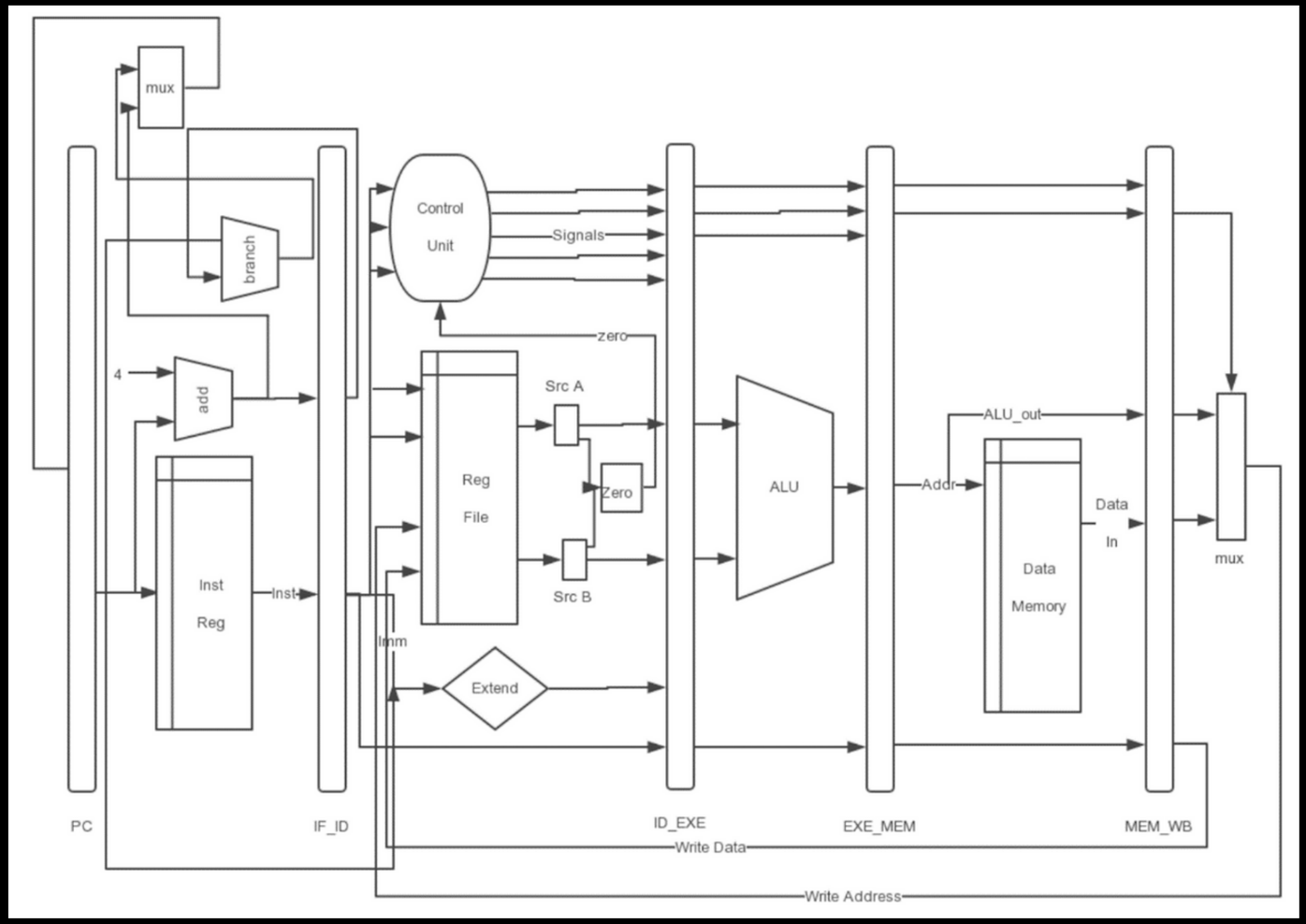
Data Forwarding

Multiplexing



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Data Forwarding

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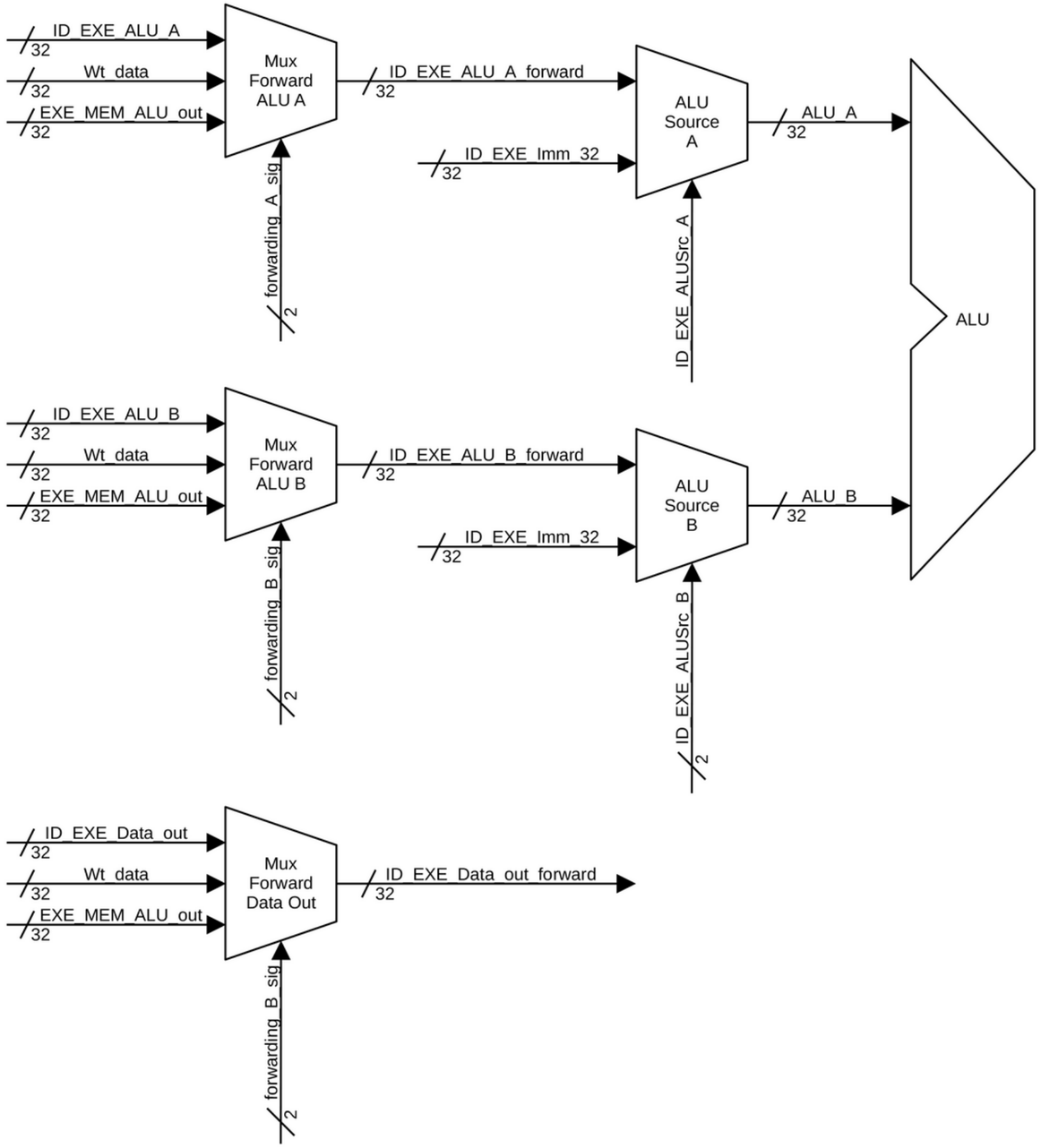

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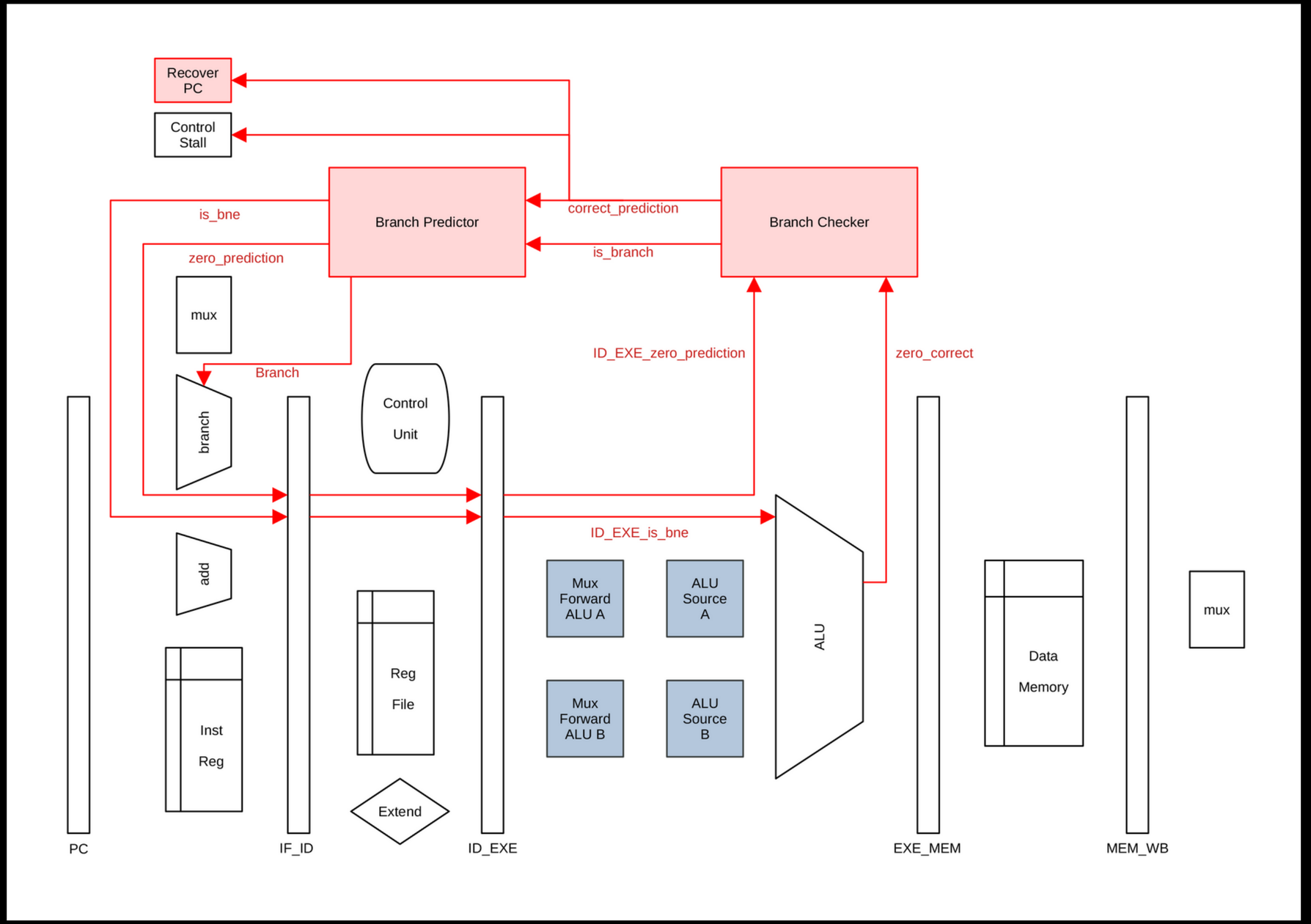
Branch Prediction

Overall Pipeline



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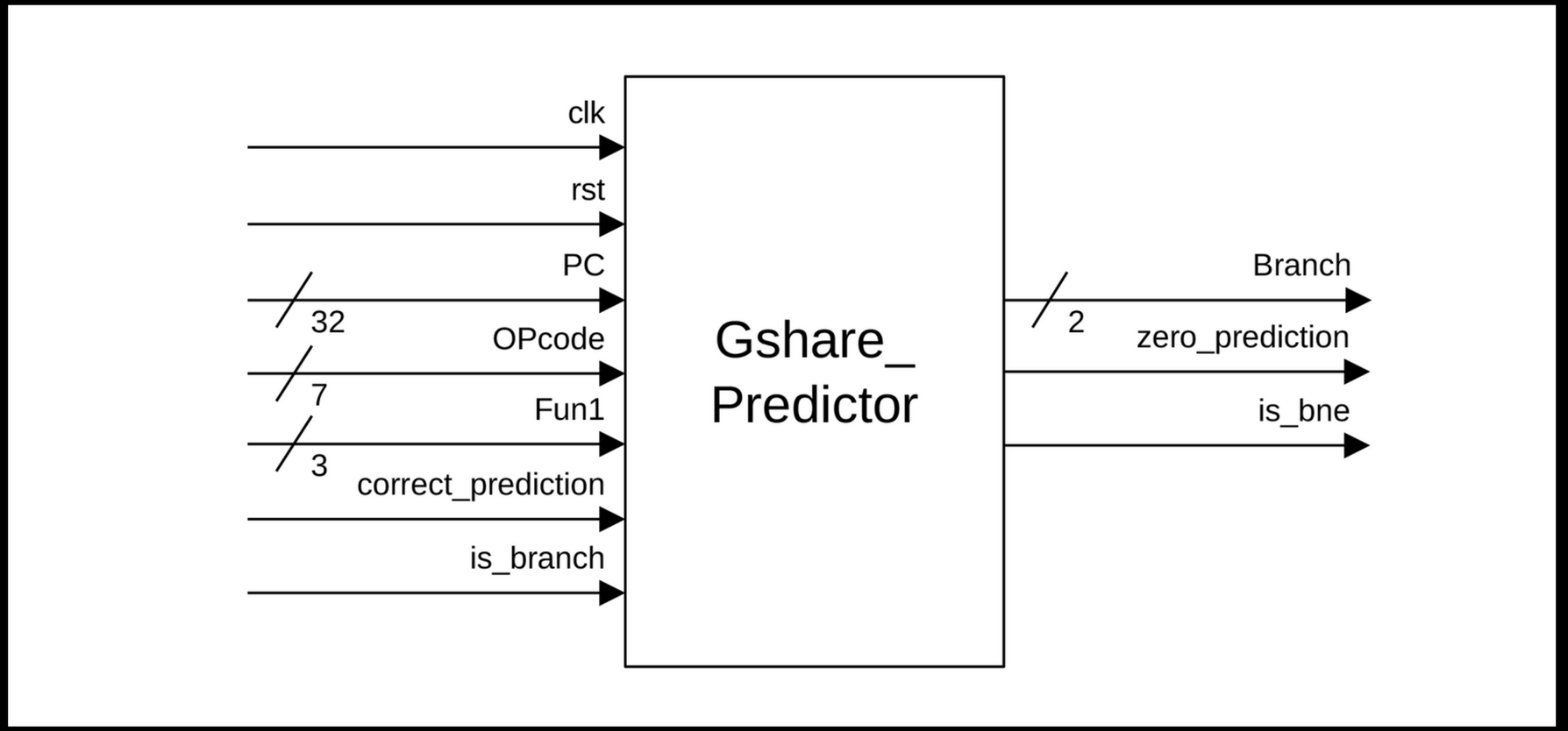
Branch Prediction

Branch Predictor



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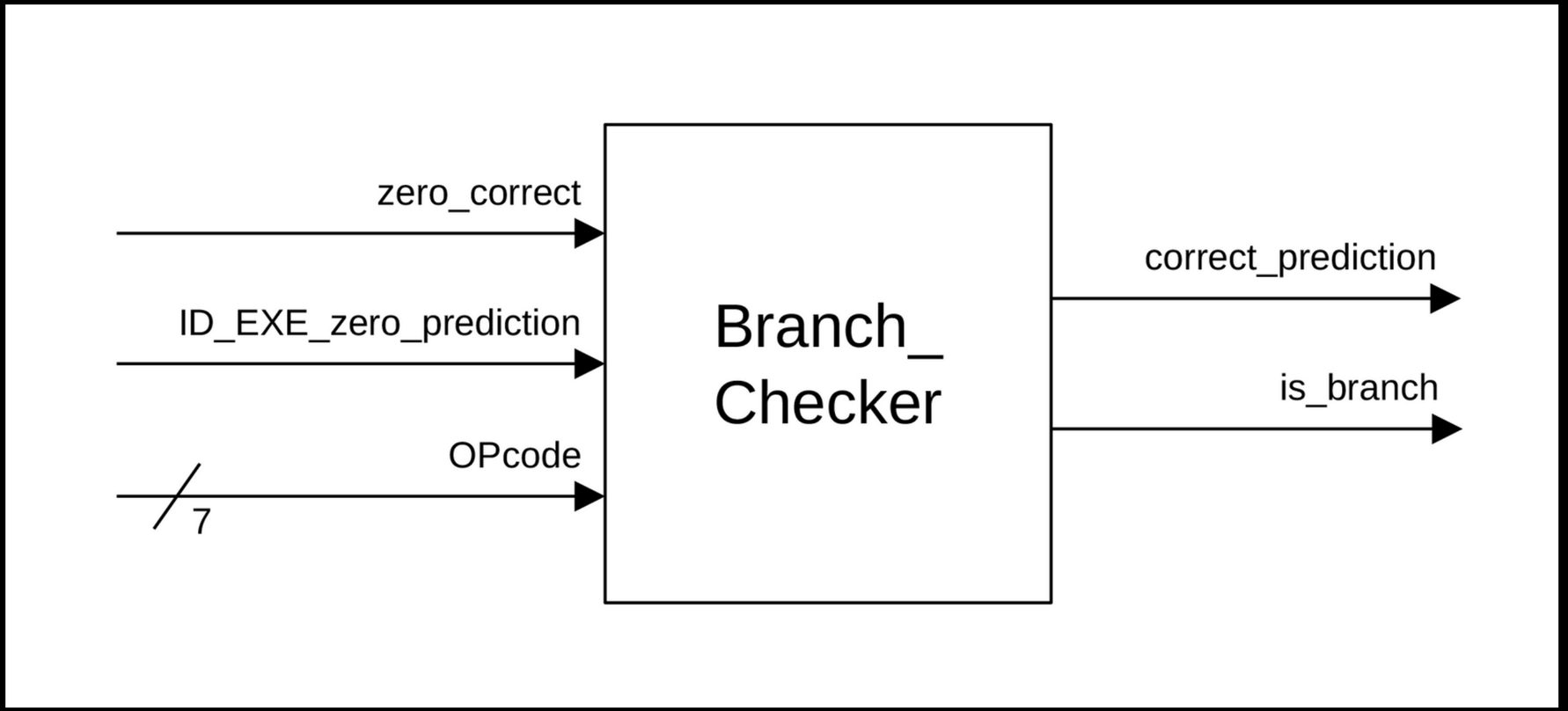
Branch Prediction

Branch Checker



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Evaluation

Data Forwarding

Branch Prediction

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Before Data Forwarding

Vec_Mul.asm:

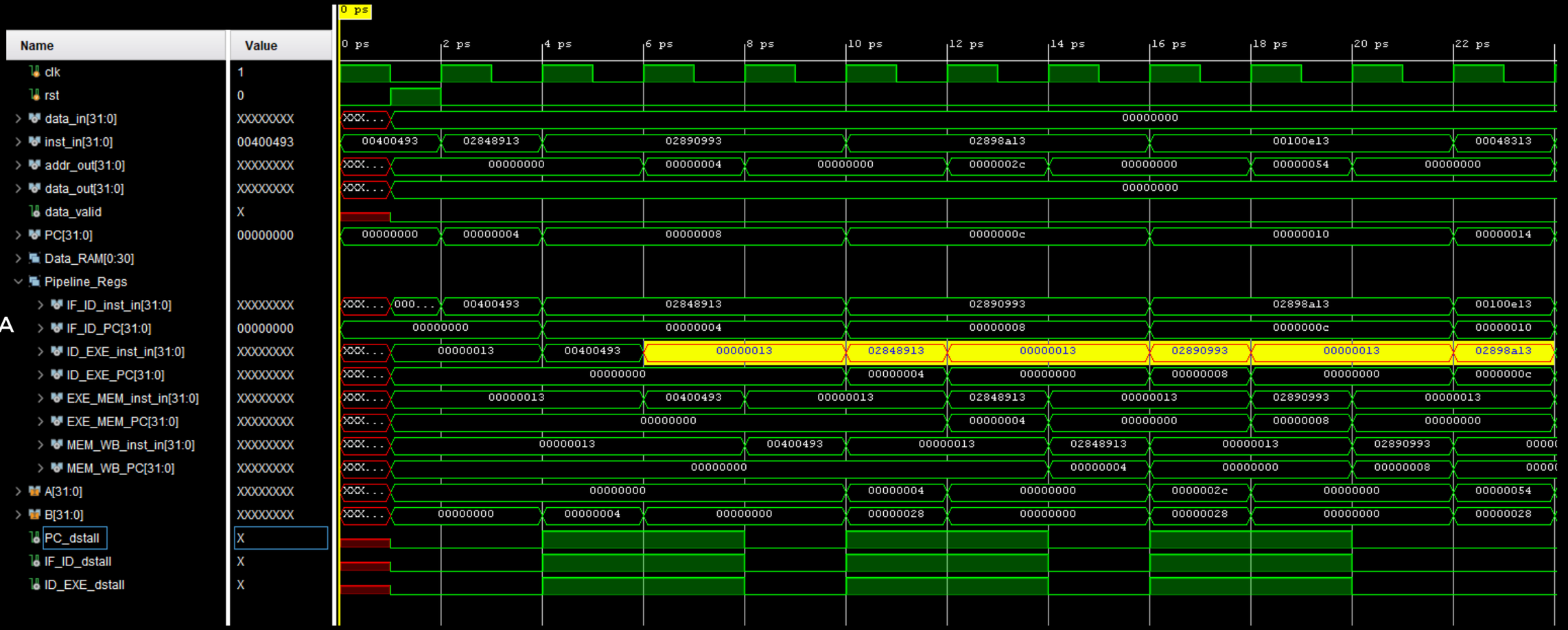
```
addi s1, x0, 4
addi s2, s1, 40
addi s3, s2, 40
addi s4, s3, 40

addi t3, x0, 1
addi t1, s1, 0
InitA:

sw t3, 0(t1)

addi t1, t1, 4
addi t3, t3, 1
slt t2, t1, s2
bne t2, x0, InitA

. . .
```



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After Data Forwarding

Vec_Mul.asm:

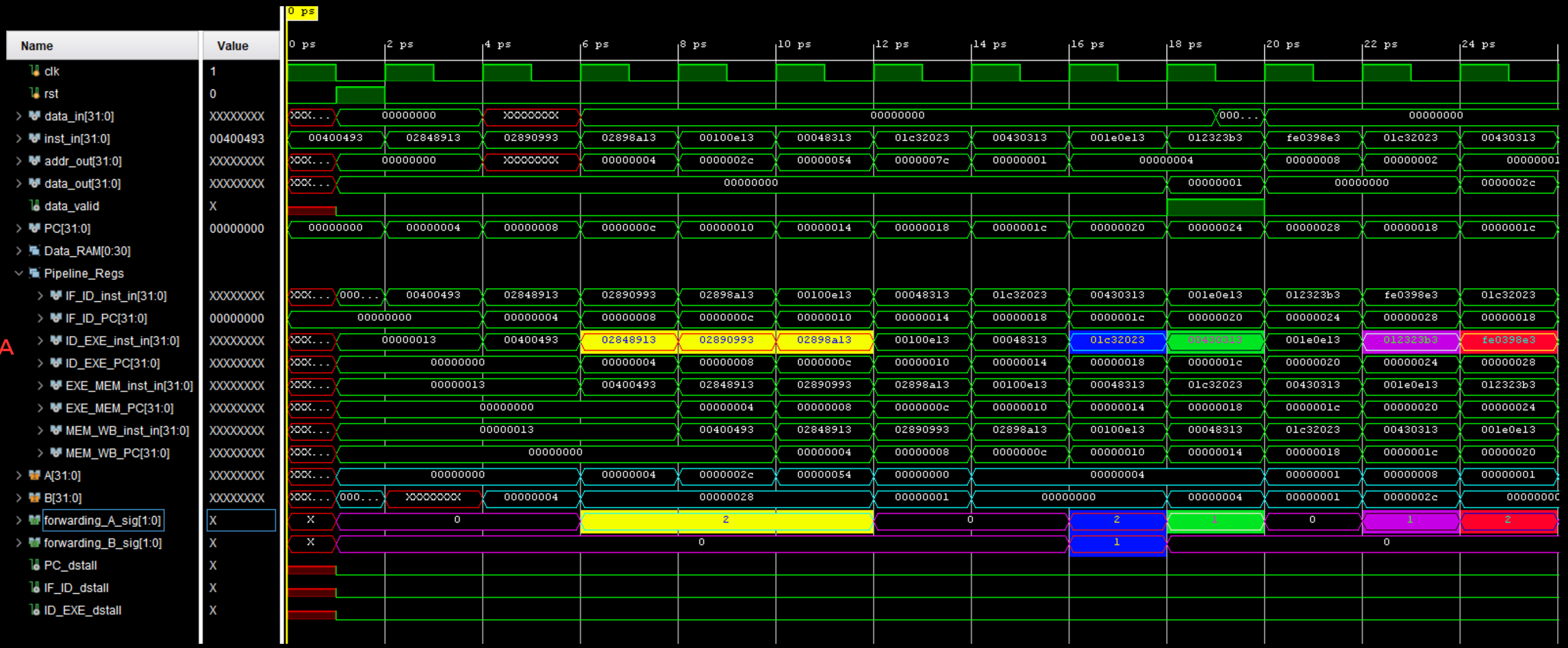
```
addi s1, x0, 4
addi s2, s1, 40
addi s3, s2, 40
addi s4, s3, 40

addi t3, x0, 1
addi t1, s1, 0
InitA:

sw t3, 0(t1)

addi t1, t1, 4
addi t3, t3, 1
slt t2, t1, s2
bne t2, x0, InitA

. . .
```



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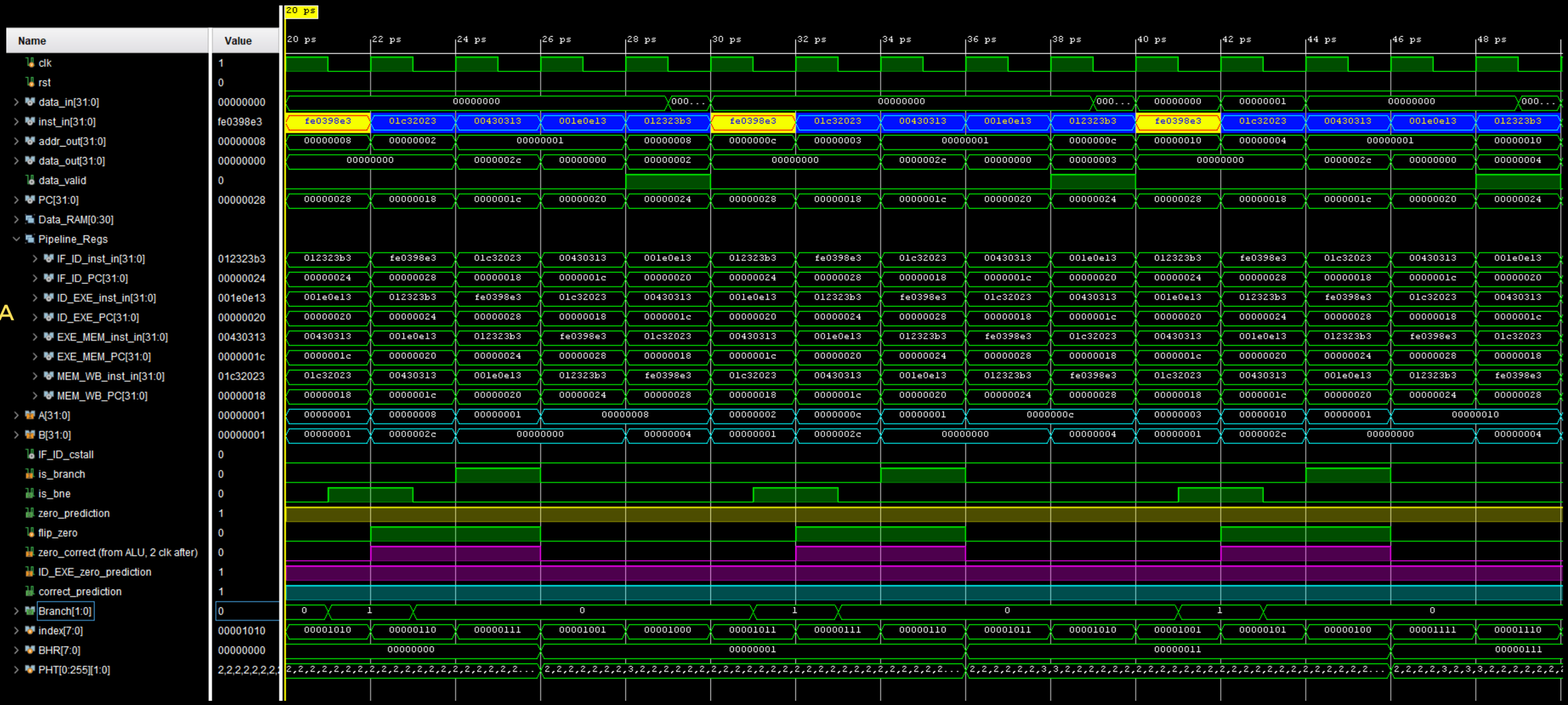
Correct Branch Prediction

Vec_Mul.asm:

```
. . .

addi t3, x0, 1
addi t1, s1, 0

InitA:
sw t3, 0(t1)

addi t1, t1, 4
addi t3, t3, 1
slt t2, t1, s2
bne t2, x0, InitA

addi t3, x0, 1
addi t1, s2, 0

InitB:
sw t3, 0(t1)

addi t1, t1, 4
addi t3, t3, 1
slt t2, t1, s3

. . .
```



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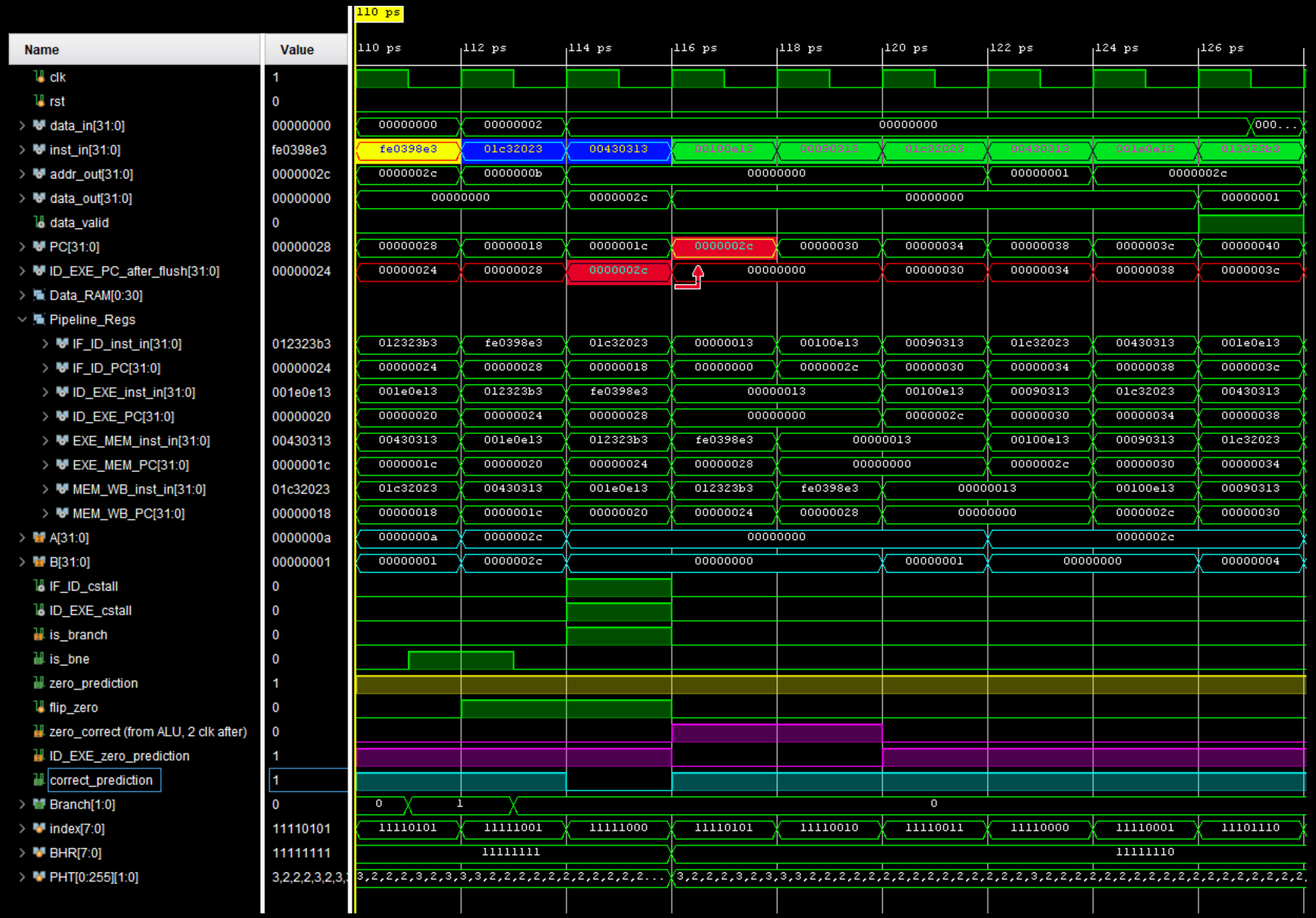
Incorrect Branch Prediction

Vec_Mul.asm:

```
. . .

addi t3, x0, 1
addi t1, s1, 0

InitA:
sw t3, 0(t1)

addi t1, t1, 4
addi t3, t3, 1
slt t2, t1, s2
bne t2, x0, InitA

addi t3, x0, 1
addi t1, s2, 0

InitB:
sw t3, 0(t1)

addi t1, t1, 4
addi t3, t3, 1
slt t2, t1, s3

. . .
```



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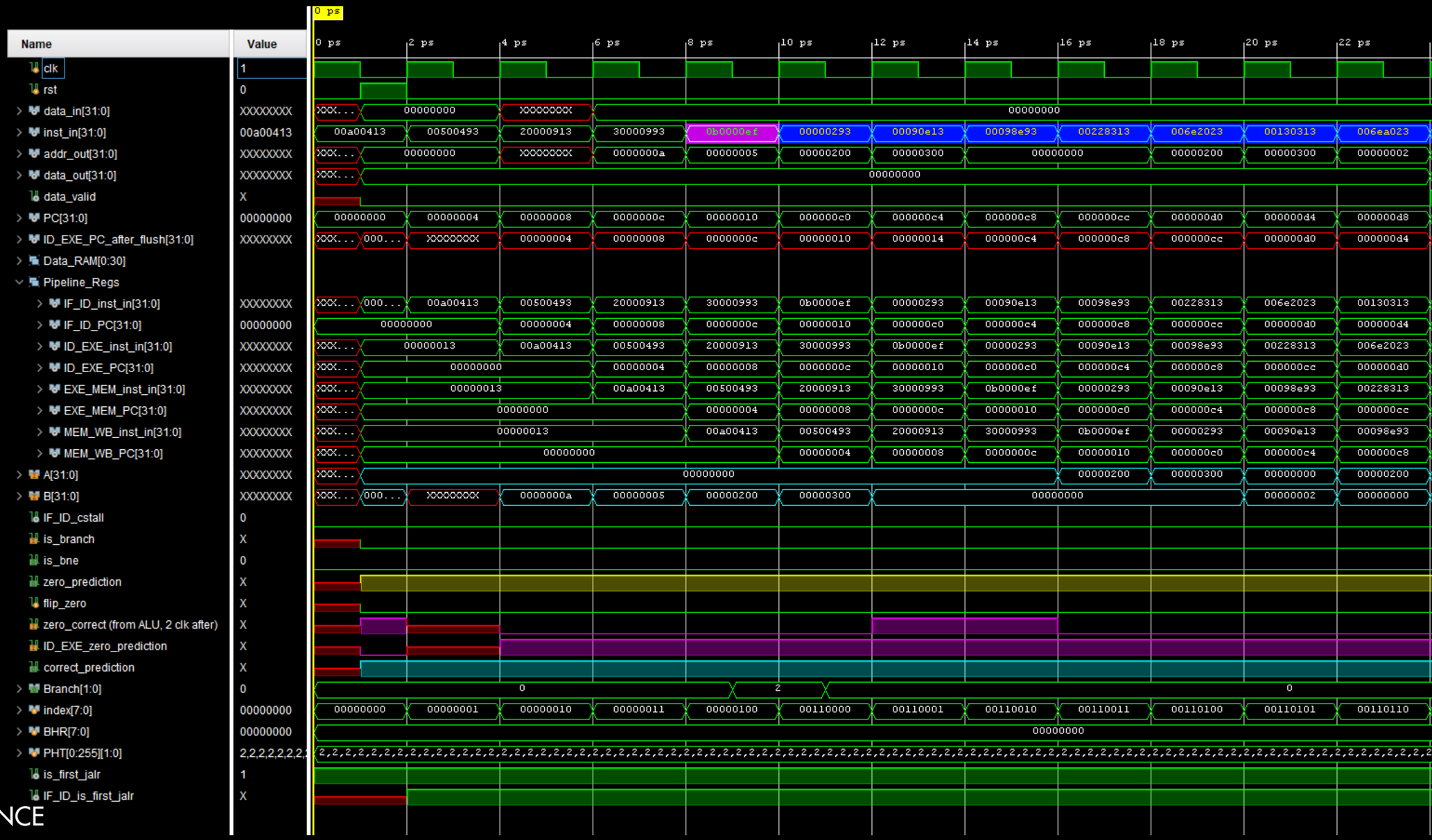
JAL instruction

```
Jacobi-1d.asm:
. . .
jal ra, init_array  // 0b0000ef
jal ra, kernel      // 008000ef
jal ra, continue    // 0d8000ef

kernel:
addi t4, s0, -1// fff40e93
addi t0, x0, 0

k_loop_t:
addi t1, x0, 1

k_loop_i1:
addi t2, t1, -1
. . .
init_array:
addi t0, x0, 0 // t0: i     // 00000293
addi t3, s2, 0 // addr of A
addi t4, s3, 0 // addr of B
init_loop_i:
addi t1, t0, 2 // data for A[i]
sw t1, 0(t3) // A[i] = i + 2
addi t1, t1, 1 // data for B[i]
sw t1, 0(t4) // B[i] = i + 3
addi t3, t3, 4
addi t4, t4, 4
addi t0, t0, 1
bne t0, s0, init_loop_i   // fe8292e3
jalr x0, ra, 0            // 00008067
. . .
```



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JALR instruction

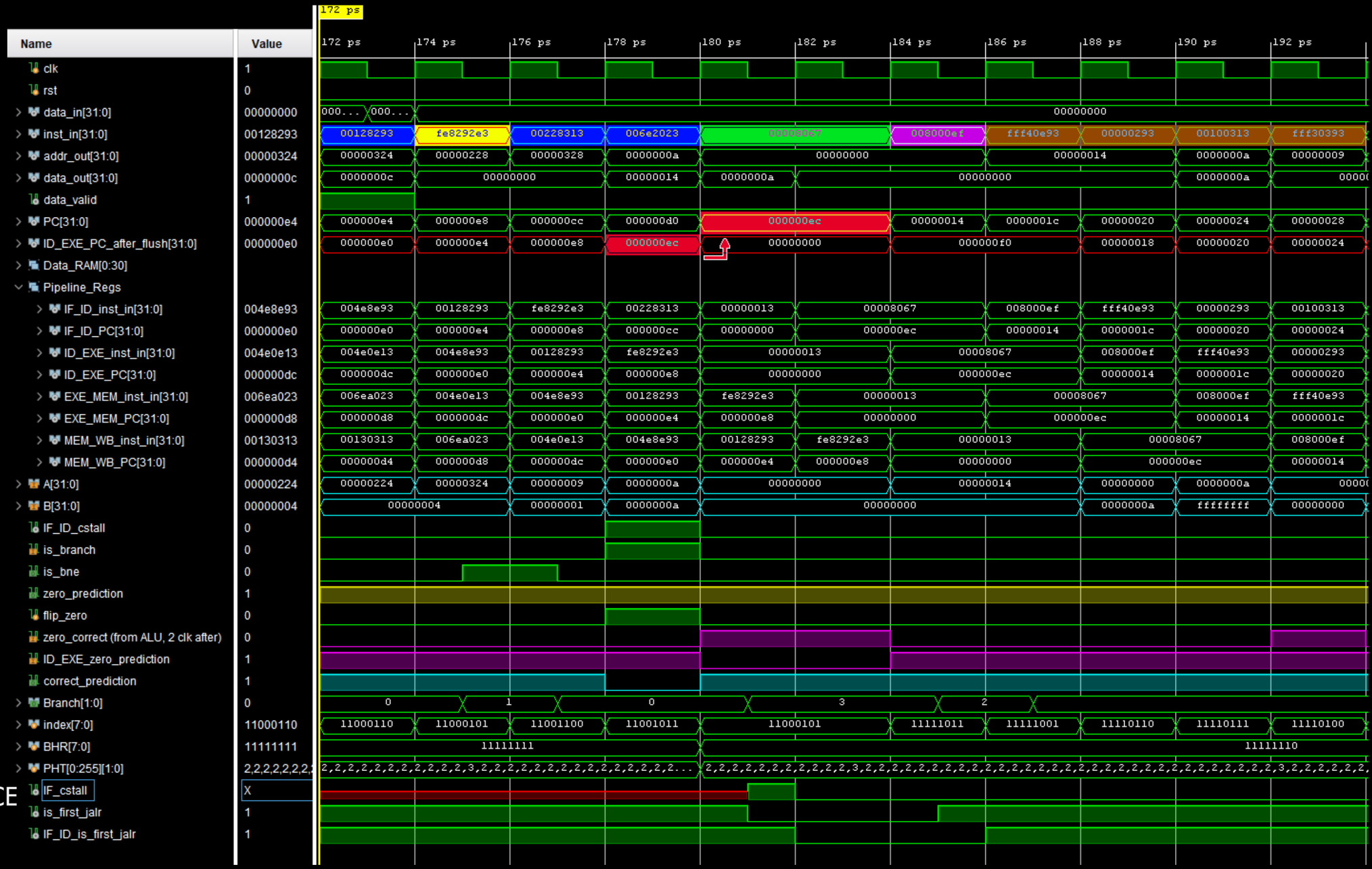
Jacobi-1d.asm:

```
. . .
jal ra, init_array  // 0b0000ef
jal ra, kernel     // 008000ef
jal ra, continue   // 0d8000ef

kernel:
addi t4, s0, -1// fff40e93
addi t0, x0, 0

k_loop_t:
addi t1, x0, 1

k_loop_i1:
addi t2, t1, -1
. . .
init_array:
addi t0, x0, 0 // t0: i     // 00000293
addi t3, s2, 0 // addr of A
addi t4, s3, 0 // addr of B
init_loop_i:
addi t1, t0, 2 // data for A[i]
sw t1, 0(t3) // A[i] = i + 2
addi t1, t1, 1 // data for B[i]
sw t1, 0(t4) // B[i] = i + 3
addi t3, t3, 4
addi t4, t4, 4
addi t0, t0, 1
bne t0, s0, init_loop_i   // fe8292e3
jalr x0, ra, 0              // 00008067
. . .
```



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Overall Speedup

	Non-optimized	Optimized	Speedup
Vec_Mul	850 clk	462 clk	1.840
Jacobi-1d	3585 clk	1748 clk	2.051

Conclusions

Significant improvement
~ x2 Speedup

Follow up: Superscalar architecture
CPI < 1

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THANKS FOR LISTENING

ANY QUESTIONS?

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