# Computer Architecture Chapter 2: MIPS – part 2



Adapted from Computer Organization the Hardware/Software Interface – 5th



## Representing Instructions

- Instructions are encoded in binary
  - Called machine code
- MIPS instructions
  - Encoded as 32-bit instruction words
  - Small number of formats encoding operation code (opcode), register numbers, ...
  - Regularity!
- Register numbers
  - \$t0 \$t7 are reg's 8 15
  - \$t8 \$t9 are reg's 24 25
  - \$s0 \$s7 are reg's 16 23



### MIPS R-format Instructions

ор	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

- Instruction fields
  - op: operation code (opcode)
  - rs: first source register number
  - rt: second source register number
  - rd: destination register number
  - shamt: shift amount (00000 for now)
  - funct: function code (extends opcode)



## R-format Example

ор	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

add \$t0, \$s1, \$s2

special	\$s1	\$s2	\$tO	0	add
0	17	18	8	0	32
000000	10001	10010	01000	00000	100000

 $00000010001100100100000000100000_2 = 02324020_{16}$ 



### Hexadecimal

- Base 16
  - Compact representation of bit strings
  - 4 bits per hex digit

0	0000	4	0100	8	1000	С	1100
1	0001	5	0101	9	1001	d	1101
2	0010	6	0110	а	1010	е	1110
3	0011	7	0111	b	1011	f	1111

- Example: eca8 6420
  - 1110 1100 1010 1000 0110 0100 0010 0000



### MIPS I-format Instructions

ор	rs	rt	constant or address
6 bits	5 bits	5 bits	16 bits

- Immediate arithmetic and load/store instructions
  - rt: destination or source register number
  - Constant:  $-2^{15}$  to  $+2^{15}$  1
  - Address: offset added to base address in rs
- Example: lw \$t0, 32(\$s3)

35 <sub>d</sub>	19 <sub>d</sub>	8	32
opcode	\$s3	\$t0	address



## Design Principle

- Design Principle 4: Good design demands good compromises
  - Different formats complicate decoding, but allow 32-bit instructions uniformly
  - Keep formats as similar as possible



## MIPS Instructions Format Summary

Instr.	Туре	ор	rs	rt	rd	shamt	function	address
add	R	0	reg	reg	reg	0	32 <sub>d</sub>	n.a.
sub	R	0	reg	reg	reg	0	34 <sub>d</sub>	n.a.
addi	I	8 <sub>d</sub>	reg	reg	n.a.	n.a.	n.a.	constant
lw	I	35 <sub>d</sub>	reg	reg	n.a.	n.a.	n.a.	address
st	I	43 <sub>d</sub>	reg	reg	n.a.	n.a.	n.a.	address

- R-format: arithmetic instructions
- I-format: data transfer instructions



## Example

• Write MIPS code for the following C code, then translate the MIPS code to machine code A[300] = h + A[300];

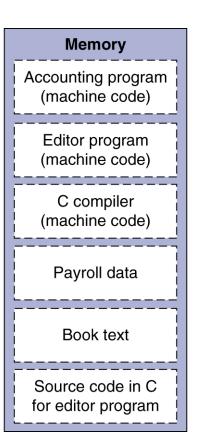
Assume that \$t1 stores the base of array
 A and \$s2 stores h



## Stored Program Computers

#### **The BIG Picture**





- Instructions represented in binary, just like data
- Instructions and data stored in memory
- Programs can operate on programs
  - e.g., compilers, linkers, ...
- Binary compatibility allows compiled programs to work on different computers
  - Standardized ISAs



## **Logical Operations**

Instructions for bitwise manipulation

Operation	С	Java	MIPS
Shift left	<<	<<	sll
Shift right	>>	>>>	srl
Bitwise AND	&	&	and, andi
Bitwise OR			or, ori
Bitwise NOT	~	~	nor

Useful for extracting and inserting groups of bits in a word



## **Shift Operations**



- *shamt*: how many positions to shift
- Shift left logical
  - Shift left and fill with 0 bits
  - -s11 by *i* bits multiplies by  $2^{i}$
- Shift right logical
  - Shift right and fill with 0 bits
  - -srl by *i* bits divides by  $2^{i}$  (unsigned only)



## **AND Operations**

- Useful to mask bits in a word
  - Select some bits, clear others to 0

and \$t0, \$t1, \$t2

```
$t2 | 0000 0000 0000 0000 00<mark>00 11</mark>01 1100 0000
```

\$t0 | 0000 0000 0000 00<mark>00 11</mark>00 0000 0000



## **OR Operations**

- Useful to include bits in a word
  - Set some bits to 1, leave others unchanged

```
$t2 | 0000 0000 0000 0000 00<mark>00 11</mark>01 1100 0000
```

\$t0 | 0000 0000 0000 0000 00<mark>11 11</mark>01 1100 0000



## **NOT Operations**

- Useful to invert bits in a word
  - Change 0 to 1, and 1 to 0
- MIPS has NOR 3-operand instruction

$$-$$
 a NOR b == NOT ( a OR b )

nor \$t0, \$t1, \$zero

Register 0: always read as zero

- \$t1 | 0000 0000 0000 0001 1100 0000 0000
- \$t0 | 1111 1111 1111 1100 0011 1111 1111



## **Conditional Operations**

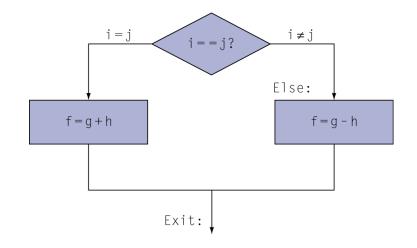
- Branch to a labeled instruction if a condition is true
  - Otherwise, continue sequentially
- beq rs, rt, L1
  - if (rs == rt) branch to instruction labeled L1;
- bne rs, rt, L1
  - if (rs != rt) branch to instruction labeled L1;
- j L1
  - unconditional jump to instruction labeled L1



## Compiling If Statements

• C code:







Assembler calculates addresses

## **Compiling Loop Statements**

• C code:

```
while (save[i] == k) i += 1;
```

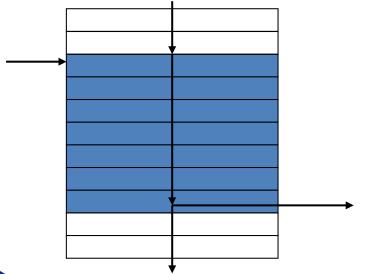
- i in \$s3, k in \$s5, base address of save in \$s6
- Compiled MIPS code:

```
Loop: sll $t1, $s3, 2 add $t1, $t1, $s6 lw $t0, 0($t1) bne $t0, $s5, Exit addi $s3, $s3, 1 j Loop Exit: ...
```



#### **Basic Blocks**

- A basic block is a sequence of instructions with
  - No embedded branches (except at end)
  - No branch targets (except at beginning)



- A compiler identifies basic blocks for optimization
- An advanced processor can accelerate execution of basic blocks



## More Conditional Operations

- Set result to 1 if a condition is true
  - Otherwise, set to 0
- slt rd, rs, rt
  - if (rs < rt) rd = 1; else rd = 0;
- slti rt, rs, constant
  - if (rs < constant) rt = 1; else rt = 0;
- Use in combination with beq, bne

```
slt $t0, $s1, $s2 # if ($s1 < $s2)
bne $t0, $zero, L # branch to L</pre>
```



## **Branch Instruction Design**

- Why not blt, bge, etc?
- Hardware for <, ≥, ... slower than =, ≠</li>
  - Combining with branch involves more work per instruction, requiring a slower clock
  - All instructions penalized!
- beq and bne are the common case
- This is a good design compromise



## Signed vs. Unsigned

- Signed comparison: slt, slti
- Unsigned comparison: sltu, sltui
- Example
  - $-\$s0 = 1111\ 1111\ 1111\ 1111\ 1111\ 1111\ 1111$
  - $-\$s1 = 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0000\ 0001$
  - -slt \$t0, \$s0, \$s1 # signed  $-1 < +1 \Rightarrow $t0 = 1$
  - -sltu \$t0, \$s0, \$s1 # unsigned
    - $+4,294,967,295 > +1 \Rightarrow $t0 = 0$



# **Procedure Calling**

- Steps required
  - Place parameters in registers
  - Transfer control to procedure
  - Acquire storage for procedure
  - Perform procedure's operations
  - Place result in register for caller
  - Return to place of call



## Register Usage

- \$a0 \$a3: arguments (reg's 4 7)
- \$v0, \$v1: result values (reg's 2 and 3)
- \$t0 \$t9: temporaries
  - Can be overwritten by callee
- \$s0 \$s7: saved
  - Must be saved/restored by callee
- \$gp: global pointer for static data (reg 28)
- \$sp: stack pointer (reg 29)
- \$fp: frame pointer (reg 30)
- \$ra: return address (reg 31)

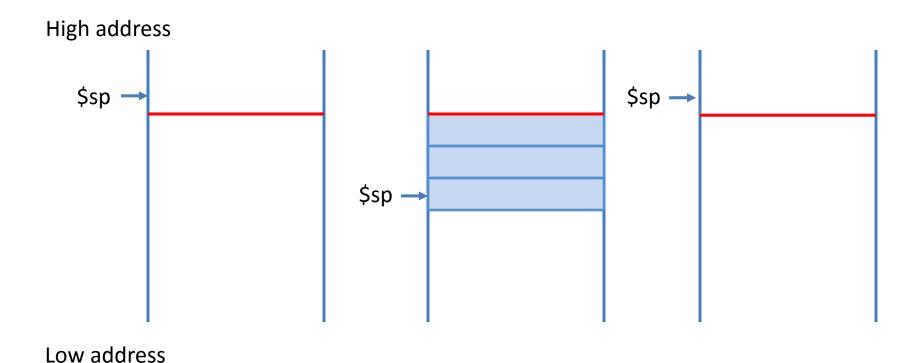


#### Procedure Call Instructions

- Procedure call: jump and link jal ProcedureLabel
  - Address of following instruction put in \$ra
  - Jumps to target address
- Procedure return: jump register
   jr \$ra
  - Copies \$ra to program counter
  - Can also be used for computed jumps
    - e.g., for case/switch statements



## Stack Address Model



**Empty stack** 

Three elements stack

Empty stack



# Leaf Procedure Example

C code:

```
int leaf_example (int g, h, i, j)
{ int f;
  f = (g + h) - (i + j);
  return f:

    Arguments g, ..., j in $a0, ..., $a3
```

- f in \$s0 (hence, need to save \$s0 on stack)
- Result in \$v0



# Leaf Procedure Example

#### MIPS code:

```
leaf_example:
 addi $sp, $sp,
       $s0, 0($sp)
  SW
       $t0, $a0, $a1
 add
       $t1, $a2, $a3
 add
       $s0, $t0, $t1
  sub
       $v0, $s0, $zero
 add
 1w
       $50, 0(\$sp)
       $sp, $sp, 4
  addi
       $ra
```

Save \$s0 on stack

Procedure body

Result

Restore \$s0

Return



#### Non-Leaf Procedures

- Procedures that call other procedures
- For nested call, caller needs to save on the stack:
  - Its return address
  - Any arguments and temporaries needed after the call
- Restore from the stack after the call



## Non-Leaf Procedure Example

C code: int fact (int n) if (n < 1) return f; else return n \* fact(n - 1); Argument n in \$a0 Result in \$v0



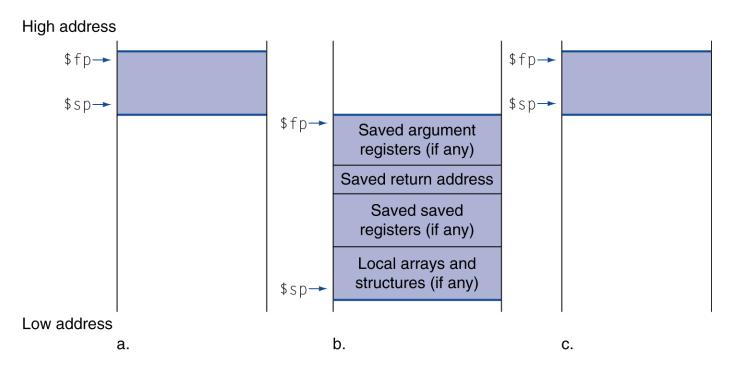
## Non-Leaf Procedure Example

#### MIPS code:

```
fact:
   addi $sp, $sp, -8
                        # adjust stack for 2 items
                        # save return address
   sw $ra, 4($sp)
   sw $a0, 0($sp)
                        # save argument
   slti $t0, $a0, 1
                        # test for n < 1
   beq $t0, $zero, L1
   addi $v0, $zero, 1
                        # if so, result is 1
   addi $sp, $sp, 8
                        # pop 2 items from stack
   jr $ra
                        # and return
L1: addi $a0, $a0, -1
                        # else decrement n
   jal fact
                        # recursive call
   lw $a0, 0($sp)
                        # restore original n
   lw $ra, 4($sp)
                        # and return address
   addi $sp, $sp, 8
                        # pop 2 items from stack
   mul $v0, $a0, $v0
                        # multiply to get result
   jr $ra
                        # and return
```



## Local Data on the Stack



- Local data allocated by callee
  - e.g., C automatic variables
- Procedure frame (activation record)
  - Used by some compilers to manage stack storage



## Memory Layout

- Text: program code
- Static data: global variables
  - e.g., static variables in C,
     constant arrays and strings
  - \$gp initialized to address allowing ±offsets into this segment
- Dynamic data: heap
  - E.g., malloc in C, new in Java
- Stack: automatic storage

