Computer Architecture

Chapter 1: Computer Abstractions and Technology Exercises

Dr. Phạm Quốc Cường

Adapted from Computer Organization the Hardware/Software Interface – 5th

Computer Engineering – CSE – HCMUT

Ex1. Chip Manufacturing

- Given the following table

Chip	Die size (mm^2)	Estimated defect rate (per cm^2)	Manufacturing size (nm)	Transistors (millions)
IBM Power5	389	0.30	130	276
Sun Niagara	380	0.75	90	279
AMD Opteron	199	0.75	90	233

a) What is the Yield for the Sun Niagara and AMD chips, assume that $\alpha = 4$?

b) Why does the Sun Niagara have a worse yield than the AMD Opteron, even though they have the same defect rate?

Ex2. Chip Manufacturing

- You are trying to figure out whether to build a new fabrication facility for your IBM Power5 chips. It costs $1 billion to build a new fabrication facility. The benefit of the new fabrication is that you predict that you will be able to sell 3 times as many chips at 2 times the price of the old chips. The new chip will have an area of 186 mm^2, with a defect rate of 0.7 defects per cm^2. Assume the wafer has a diameter of 300 mm. Assume it costs $500 to fabricate a wafer in either technology. You were previously selling the chips for 40% more than their cost.

a) What is the cost of the old and the new PowerPC chips?

b) What was/is the profit on each old/new PowerPC chip?

c) If you sold 500,000 old Power5 chips per month, how long will it take to recoup the costs of the new fabrication facility?

Ex3. Performance

- Suppose we have made the following measurements:
  - Frequency of FP operations = 25%
  - Average CPI of FP operations = 4.0
  - Average CPI of other instructions = 1.33
  - Frequency of FPSQR= 2%
  - CPI of FPSQR = 20
- Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5. Compare these two design alternatives using the processor performance equation.

Ex4. Performance

- Assume a program requires the execution of:
  - 50×10^6 FP instructions,
  - 110×10^6 INT instructions,
  - 80×10^6 L/S instructions,
  - and $1^6 \times 106$ branch instructions.
- The CPI for each type of instruction is 1, 1, 4, and 2, respectively. Assume that the processor has a 2 GHz clock rate.

a) By how much must we improve the CPI of FP instructions if we want the program to run two times faster?

b) By how much must we improve the CPI of L/S instructions if we want the program to run two times faster?

c) By how much is the execution time of the program improved if the CPI of INT and FP instructions is reduced by 40% and the CPI of L/S and Branch is reduced by 30%?