Procesorul MIPS – Pipeline

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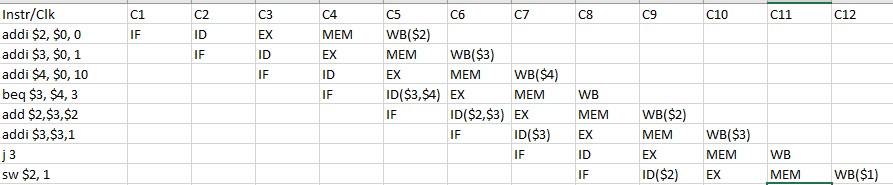
Grupa: 30226

1. **Tabel cu descrierea regiștrilor de pipeline**

|  |  |  |  |
| --- | --- | --- | --- |
| REG\_IF\_ID(31 – 0) | REG\_ID\_EX(85 – 0) | REG\_EX\_MEM(58 – 0) | REG\_MEM\_WB(36 – 0) |
| Instruction(31 – 16) | RegDst(0) | MemtoReg(0) | MemtoReg(0) |
| PC + 1(15 – 0) | ALUSrc(1) | RegWrite(1) | RegWrite(1) |
|  | Branch(2) | MemWrite(2) | ReadData(17 – 2) |
|  | Bgez(3) | Branch(3) | ALURes(33 – 18) |
|  | Bltz(4) | Bgez(4) | WriteAddress(36 – 34) |
|  | Slt(5) | Bltz(5) |  |
|  | ALUOp(8 – 6) | BranchAddress(21 – 6) |  |
|  | MemWrite(9) | Zero(22) |  |
|  | MemtoReg(10) | Sign(23) |  |
|  | RegWrite(11) | ALURes(39 – 24) |  |
|  | sa(12) | RD2(55 – 40) |  |
|  | PC + 1(28 – 13) | WriteAddress(58 – 56) |  |
|  | RD1(44 – 29) |  |  |
|  | RD2(60 – 45) |  |  |
|  | ExtImm(76 – 61) |  |  |
|  | Func(79 – 77) |  |  |
|  | rt(82 – 80) |  |  |
|  | rd(85 – 83) |  |  |

Programul original:

|  |  |
| --- | --- |
| **Instr. Nr.** | **Program** |
| 0 | addi $2, $0, 0 |
| 1 | addi $3, $0, 1 |
| 2 | addi $4, $0, 10 |
| 3 | beq $3, $4, 3 |
| 4 | add $2,$3,$2 |
| 5 | addi $3,$3,1 |
| 6 | j 3 |
| 7 | sw $2, 1 |

Tabel – Analiza hazardurilor

Pentru a evita hazardurile au fost introduse doua instructiuni care nu se executa

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1. **Codul modificat pentru evitarea hazardului**

**B"001\_000\_010\_0000000", -- addi $2, $0, 0 #2100 -- s = 0;**

**B"001\_000\_011\_0000001", -- addi $3, $0, 1 #2181 -- i = 1;**

**B"001\_000\_100\_0000011", -- addi $4, $0, 10 #2203 -- n = 10;**

**B"000\_000\_000\_000\_0\_000", --noop**

**B"000\_000\_000\_000\_0\_000", --noop**

**B"100\_011\_100\_0000011", -- beq $3, $4, 3 #8E03 -- while(i<n){**

**B"000\_010\_011\_010\_0\_000", -- add $2, $3, $2 #09A0 -- s = s+i;**

**B"001\_011\_011\_0000001", -- addi $3, $3, 1 #2d81**

**B"111\_0000000000101", -- j 5 #E003**

**B"011\_000\_010\_0000001", -- sw $2, 1 #6101**

**others => x"1111"**

1. **Schema RTL**

