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Study of Signal Integrity and Radiated Emission of Single Ended and Differential High Speed Digital Signals Crossing a Slot

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***Abstract*—With increasing board complexity and operating frequencies, signal integrity (SI) and radiated emission (RE) compliance for high speed digital board is becoming a challenge to printed circuit board (PCB) designers. Together with higher routing density and multiple on-board power supplies, routing traces across split planes are unavoidable. In this paper, SI performance and RE of single ended and differential signals propagating across slots are studied. Using both experimental and numerical simulation approaches, the impacts of single ended and differential high speed digital signals across a split plane are investigated and analysed.**

I. Introduction

Radiated emission (RE) from high speed digital boards has always been a critical electromagnetic compatibility (EMC) design issue for designers [1]-[2]. RE arises mainly from a digital signal propagating down the clock and signal traces [3]. To suppress radiated emissions, extra care and effort is needed to ensure discontinuities on the transmission lines are minimized. Major causes of discontinuities include bends, interchanging layers, and split planes [4]-[6]. In most practical PCB designs, it is common for traces to be routed across a slot. Routing transmission lines across split planes is not only a concern for EMC compliance but also SI performance too.

This paper aims to provide a comprehensive study to investigate the impacts of different signalling implementations across a split plane. The study will be carried out using digital signal's voltage waveforms, near field emission profile and far field RE. To facilitate the study, two different PCBs, as shown in Fig. 1(a) and (b) were fabricated.

(a) (b)

Fig. 1. PCBs for the study of different signalling standards across a split plane (a) PCB 1 using LVTTL single ended signals (b) PCB 2 using LVDS differential signals

The digital circuitries are implemented on the 4-layer board having a dimension of 51 mm by 114 mm for PCB 1. PCB 2 is slightly wider, having a trace width of 64 mm due to implementation of additional SMA connectors. The boards are 1.5 mm thick and FR4 is used as the substrate, where its relative permittivity is 4.5. However, in terms of PCB design, both boards are similar, except for the signal driver. PCB 1 adopts a single ended signalling scheme implemented with LVTTL [7], while PCB 2 uses a differential signalling scheme with LVDS and the center-to-center spacing between adjacent traces is 0.4 mm [8]. The three cases where the signal is propagated across a slot are:

- Slot 1: 1 cm x 2 cm
- Slot 2: 2 cm x 2 cm
- Slot 3: 4 cm x 2 cm

For all three cases, the trace length of the microstrip line is designed to be 60 mm long. They have a trace width of 0.2 mm placed 0.1524 mm above the reference plane.

II. Full Wave Simulation

The PCB layout for each board in Fig. 1 is imported into a 3D EM solver for full wave simulation. The platform used in this study is CST Microwave Studio (MWS) [9]. Discrete ports and lumped elements are added into the model to act as input ports and termination loads. Fig. 2 shows the PCB layout of PCB 1 modelled in CST MWS for the study.

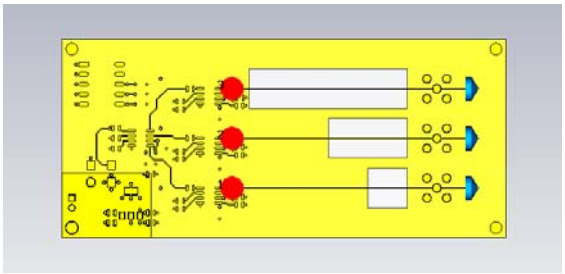


Fig. 2. PCB layout imported into CST MWS simulation platform for PCB 1

In the simulation of single ended signalling across various slots, the source used is an ideal voltage source (indicated by the red spots) with trapezoidal waveform of amplitude 1 V, rise and fall times t_r and t_f = 1 ns, and hold time t_h = 3 ns. The trace was terminated by a 50 Ω load (indicated by the blue spots) to minimize impedance mismatch. Fig. 3 shows the simulated input and output voltage waveforms across the different slots in PCB design 1 using single ended signalling scheme. For the simulation of differential signalling scheme across various slots, an ideal current source is used to excite the pair of differential lines [10]. The current waveform is trapezoidal, having a rise time of 1 ns and its amplitude is 3.5 mA. To calculate the differential output voltage across the

traces, a 100 Ω resistance was used. These are the typical values for a LVDS driver in order to provide a 350 mV across the terminating resistor at the receiver [11]. Fig. 4 shows the simulated voltage waveforms when a differential signal is propagated across the various slots in PCB design 2. Generally, the degradation in signal rise time is less pronounced than that of single ended signalling scheme.

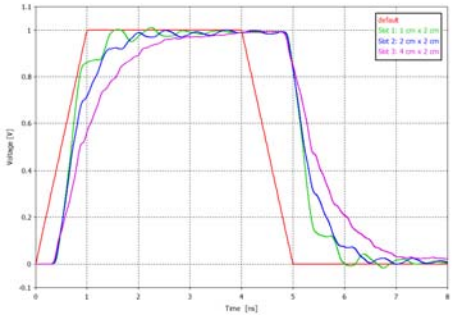


Fig. 3. Simulated input and voltage waveforms due to single ended signalling scheme across different slots in PCB design 1

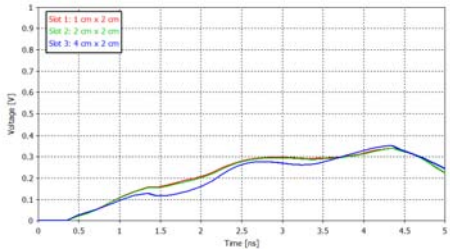


Fig. 4. Simulated output voltage waveforms due to differential signalling scheme across different slots in PCB design 2

From the time domain waveforms, it can be seen that degradation in rise and fall time of the signal is observed. The reduction in the transition time is caused by the per unit length inductance associated with the slot, which can be calculated as follows [12]:

$$L_{slot} = \frac{\mu_0}{2\pi}\left[\ln\left(\frac{3w+s}{3w+t}\right)+1.5\right] \quad (1)$$

where t is the thickness of the trace, w is the trace width, s is the length of the slot, and μ_0 = 4π x 10^7 H/m is the permeability of free space. With that, the degradation of signal rise time can be computed as follows [13]:

$$t_{r,slot} = \sqrt{t^2{}_{slot} + t^2{}_r} = \sqrt{(2.2L_{slot}/2Z_0)^2 + t_r^2} \quad (2)$$

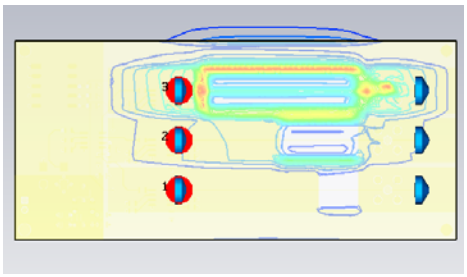
The associated inductance and overall rise time of the three cases with different slot sizes are calculated and given in Table I. From the table, it can be seen that degradation in rise time due increasing slot length is insignificant. However, if we were to compare the cases with and without slot, the ideal t_r of 1.2 ns is significantly increased to 1.7 ns.

TABLE I

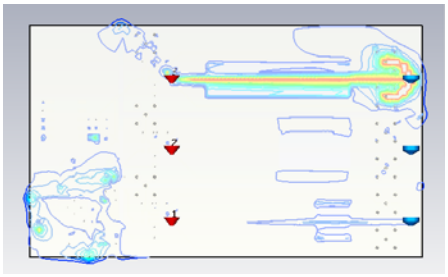
CALCULATED INDUCTANCE AND OVERALL RISE TIME DUE TO SLOT

Description	Inductance [nH]	Calculated t_r [ns]
Slot 1: 1 cm x 2 cm	54.66	1.70
Slot 2: 2 cm x 2 cm	62.71	1.82
Slot 3: 4 cm x 2 cm	70.90	1.97

The simulated surface current distribution along slot 3 at 1 GHz for PCB 1 and PCB 2 are shown in Fig. 5(a) and Fig. 5(b), respectively. It can be seen from the two surface current plots that return current of the single ended trace is concentrated around the edges of the slot; whereas for the case of differential signal, the return current does not depend on the power or ground plane as reference. In terms of RE, differential signalling offers better performance than single ended signals when crossing over a slot.



(a)



(b)

Fig. 5. Surface current plots of a signal transiting across the 4 cm x 2 cm slot at 1 GHz (a) Single ended signals (b) Differential signals

III. EXPERIMENTAL RESULTS

In this section, the effects of different signals across various split planes are validated experimentally based on signal integrity (SI), near field (NF) plot and far field (FF) RE in a semi-anechoic chamber (SAC).

A. *Signal integrity measurement*

The voltage waveforms of the signals were measuring using a high speed oscilloscope, Tektronix DPO7354 (3.5 GHz). Fig. 6 shows the measured time domain signals of single ended LVTTL signal across the various slots.

Generally, it can be seen that degradation in fall time is observed as the length of the slot increases. Despite not showing the sharp transition as calculated using CST, the measurement results are fairly consistent with the simulation results. The typical output characteristic of the CDCVF 2505 driver can be found in [14]. For CMOS devices, the total output impedance of the driver is approximately 37 Ω (PMOS = 12 Ω, S_{series} = 25Ω). Hence, using voltage division, the maximum measured output voltage is estimated to be $\frac{50}{50+37}\times 3.3V = 1.90V$.

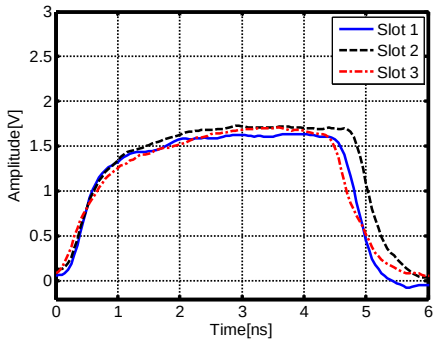


Fig. 6. Measured output voltage waveforms for LVTTL single ended signals across different slots

Fig. 7 shows the measured time domain signal of a differential LVDS signal across slot 1 and slot 3. For LDVS drivers, it operates as a constant current source, and its output voltage is proportional to the load resistance connected across it. The measurements show that there is very little distortion in the output voltages when acrossing different slots.

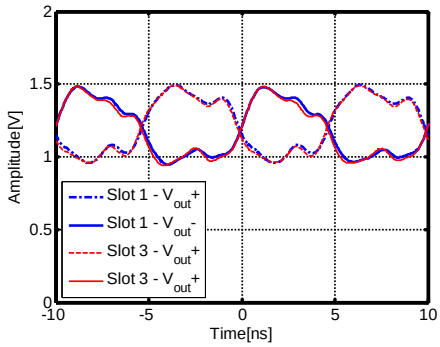


Fig. 7. Measured single ended voltage waveforms for LVDS differential signals across Slot 1 – 1 cm x 2 cm and Slot 3 – 4 cm x 2 cm

B. Near-field emissions plot

In this section, the near field plots of signals transiting across different split planes are presented and discussed. The NF emissions from the test boards are carried out using Detectus AB NF EM scanner [15]. Both frequency emission and spatial emission are measured for the study. The module is controlled by a computer via a GPIB cable and R&S spectrum analyser, ZVB8 (9 kHz – 3.5 GHz) is used to capture the emissions. Fig. 8 shows the setup of the test board on the NF scanner module. The test boards are powered up by a power supply providing a stable +5 V DC voltage to it.

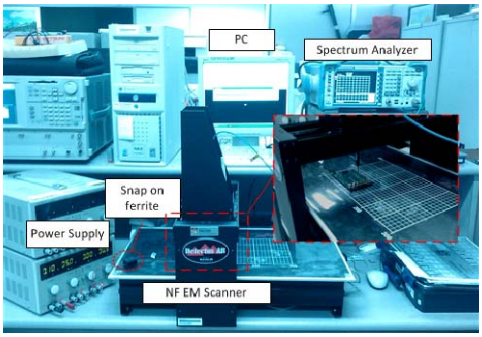
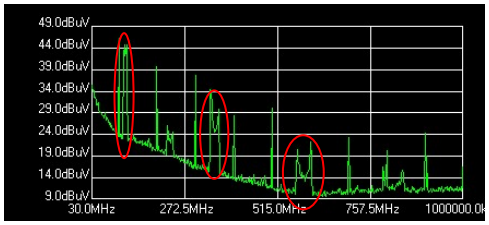


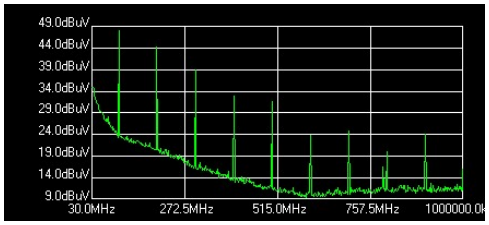
Fig. 8. Measurement setup for scanning NF emissions from test boards (a) Front view (b) Closed up of probes above the test board

For this study, the NF plots for the single ended and differential signalling schemes crossing the 4 cm x 2 cm slot are presented as larger slot size offers better viewing resolution for the study. The magnetic fields in *x* and *y* axes are measured with probes placed 20 mm above the board.

Fig. 9 shows the results of the frequency-domain emission plots obtained from the NF scanner for the test boards when the signals are crossing a slot of dimension 4 cm x 2 cm. It is interesting to look at the frequency domain plots for the case when the signals are transmitted across the 4 cm x 2 cm slot. As the boards are driven by a clock of 100 MHz, harmonics at multiples of 100 MHz are expected. However, from the frequency emission plots, it can be seen that due to the discontinuity introduced by the slot, a broadband noise is observed as highlighted by the red circles.



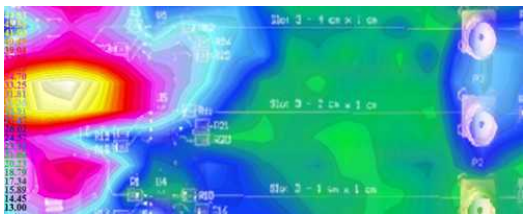
(a)



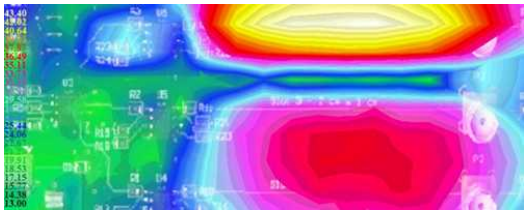
(b)

Fig. 9. Near field frequency emission plots of a signal transmission across a 4 cm x 2 cm slot using (a) Single ended signalling (b) Differential signalling

Fig. 10 shows the results of the spatial emission plots obtained from the NF scanner for the test boards when the signals are crossing a slot of dimension 4 cm x 2 cm. The near field spatial emission plots for differential signalling across the 4 cm x 2 cm slot is excluded as the spatial emission plot do not indicate any noticeable variation.



(a)



(b)

Fig. 10. Near field spatial emission plots of a single ended signal across a 4 cm x 2 cm slot using (a) 100 MHz in y-direction (b) at 115 MHz in y-direction

From Fig. 9(a), at 100 MHz, the emission is mainly from the clock circuit. There is not much emission seen due to the signal crossing the slot. At approximately 115 MHz, which is the onset of the fundamental frequency of the broadband noise, the effect of slot is observed. It is also noticed that as the signal is excited across the slot, the noise generated may be picked up at adjacent traces, which is undesirable from SI point of view.

C. Far-field emissions plot

In this section, the far field radiated emissions are measured in a semi-anechoic chamber from 30 MHz to 1 GHz. The experimental setup for measuring far field emissions from the boards is shown in Fig. 10. The SA is set to peak hold so as to capture the maximum emissions from the board as the turntable is rotated with the log-periodic antenna is raised from a height of 1 m to 4 m. Emissions in both horizontal and vertical polarizations were measured.

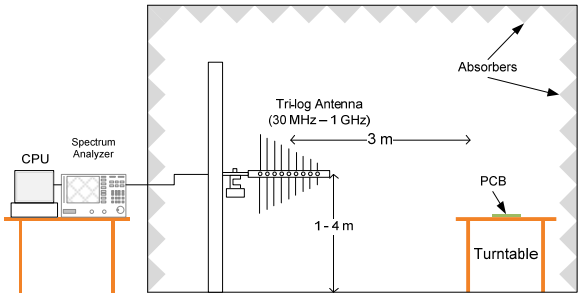
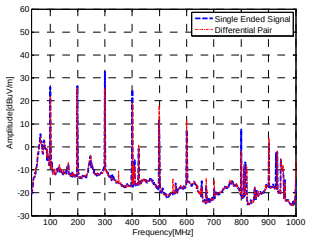


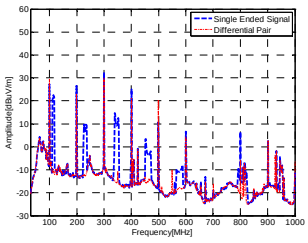
Fig. 10. Experimental setup of measuring far field emissions from the boards in an SAC

To ensure repeatability with a constant current source throughout the measurement, the boards are powered by a power supply through a 3.3V regulator. To minimize unnecessary coupling form due to the power supply, the cables interfacing the power supply to the boards are twisted and kept short. In addition, a clamp on ferrite sleeve is used. In Fig. 11, the peak-hold far field emissions of the single ended signals are plotted in blue while the differential signals are plotted in red.

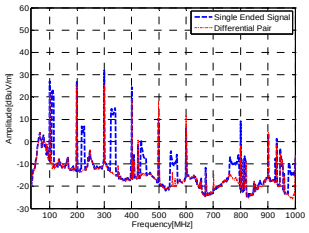
The red plot is also the same for all the different test conditions. The main source of emissions is contributed by the clock driver circuitries, while the differential signals generally do not contribute much noise. The blue plot on the other hand is different for all the different test cases. In can be seen that, a single trace crossing a slot do not create much emissions. However, the following may not hold when multiple signals are excited across the slots as depicted in Fig. 12(d).



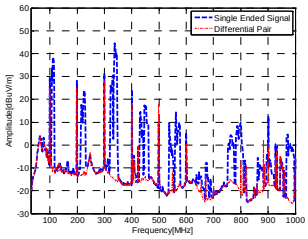
(a)



(b)



(c)



(d)

Fig. 11. Far-field emissions measurement setup using semi-anechoic chamber for the two PCBs when the signal is excited across (a) Slot 1 (b) Slot 2 (c) Slot 3 (d) All 3 slots

IV. CONCLUSIONS

The effects of different signalling schemes crossing slots are studied both numerically and experimentally. For the case of single ended signalling, rise time degradation and broadband emission are observed. There is also an increase in radiated emission and it cannot be ignored for complex high speed digital system. A good solution to overcome such problem is to use differential transmission. It is demonstrated experimentally in this paper that due to the presence of a proper return path, no additional radiated emissions is generated for a differential signal crossing over slot.

REFERENCES

[1] B. Young, "Digital Signal Integrity Modeling and Simulation with Interconnects and Packages," Prentice Hall, 2000.

[2] M. I Montose, "EMC and the printed circuit: Design, theory, and layout made simple", IEEE Press, 1999.

[3] S. Radu, and D. Hockanson, "An investigation of PCB radiated emissions from simultaneous switching noise", in IEEE Int. Symp. on EMC, vol. 2, pp. 893-898, Aug 1999.

[4] H. J. Liaw, and H. Merkelo, "Crossing the planes at high speed. Signal integrity issues at split ground and power planes", in IEEE Circuits and Devices Magazine, vol. 13, no. 6, pp. 22-26, Nov. 1997.

[5] R. W. Y. Chang, K. Y. See, Y. L. Tan, "Impacts of bends and ground return vias on interconnects for high speed GHz designs", in 19th Int. Zurich Symp. on EMC, pp. 502-505, May 2008.

[6] W. F. Pan, S. Conner, and B. Archambeault, "Predicting noise voltage from trace crossing split planes on printed circuit boards", in IEEE Int. Symp. on EMC, pp. 45-50, Aug 2009.

[7] CDCVF2505 datasheet, www.ti.com [online]

[8] SN65LVDS 179 datasheet, www.ti.com [online]

[9] www.cst.com [online]

[10] S. Caniggia, and F. Maradei, "Crosstalk investigation in differential interconnects by circuit and numerical simulations", in Proc. of Int. Symp. on EMC Kyoto, pp. 277-280, 2009.

[11] TIA/EIA-644 Standards, Electrical characteristics of low voltage differential signaling (LVDS) interface circuit, 2001.

[12] S. Caniggia, and F. Maradei, "Signal integrity and radiated emission of high-speed digital systems", John Wiley and Sons, 2008.

[13] H. Johnson, and M. Graham, "High speed digital design – A handbook of black magic", Prentice Hall, 1993.

[14] CDCVF2505 Application Note, Design and layout guidelines for the CDCVF2505 clock driver, Nov 2000.

[15] www.detectus.se [online]