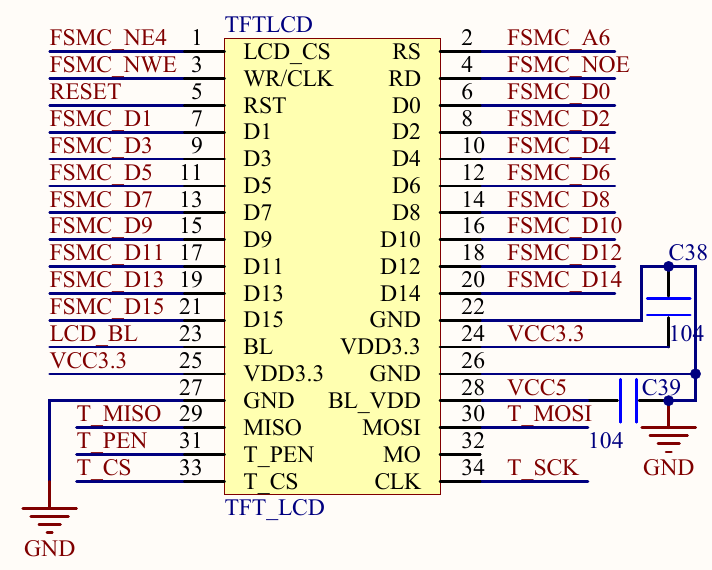
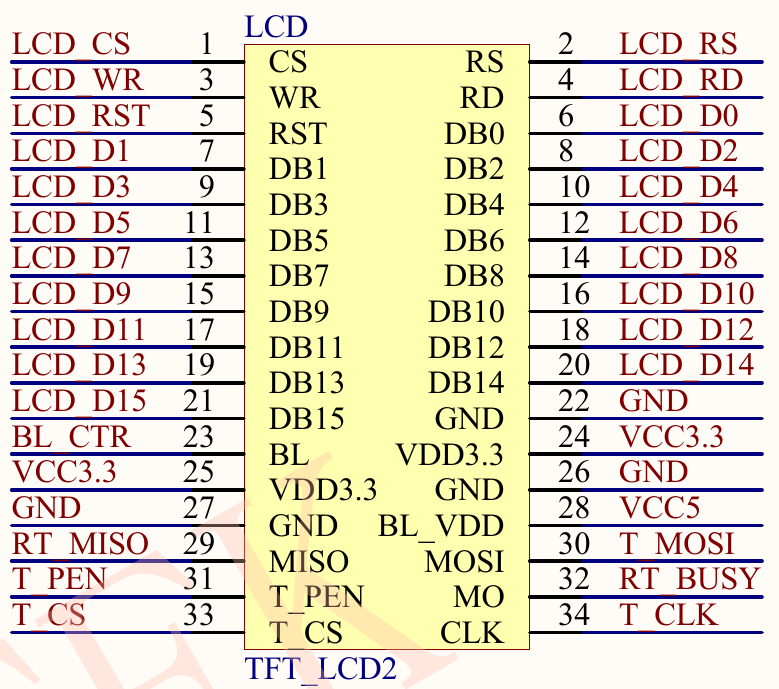
**STM32F407ZGT6-6-TFTLCD-Basic**

# Circuit Connection

****

LCD\_BL连在PB15上, 是GPIO;

上图是原子F4主板上的接口图, 与之对应的LCD上的连接是:

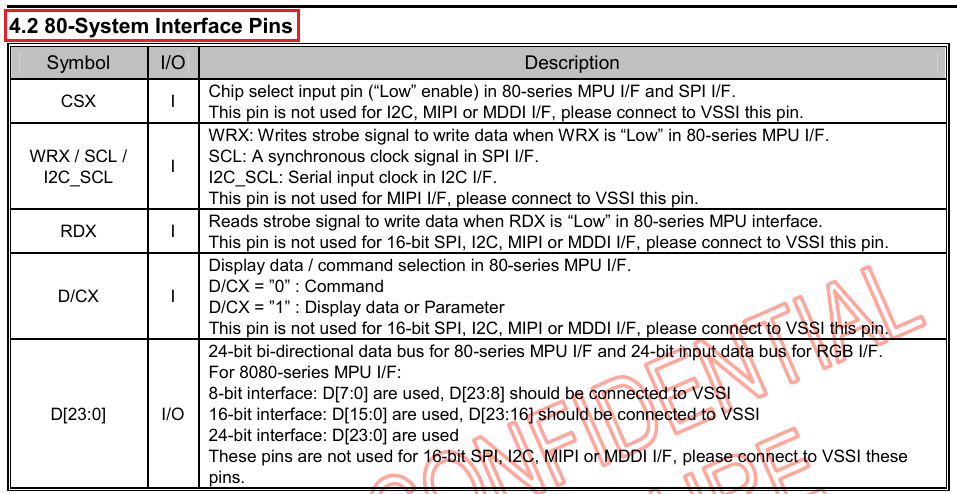


# LCD Controller Datasheet

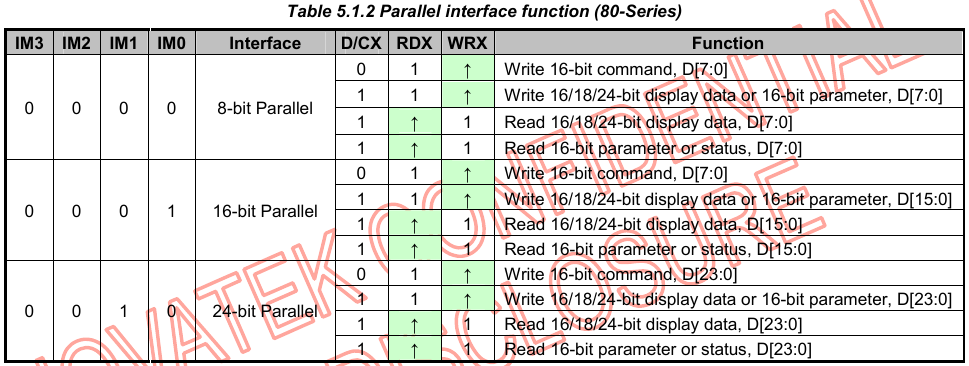
**我的板子的LCD是4.3英寸的, ID是5510**. 它的Controller是NT35510.

NT3550支持很多种不同的Interface, 我这里用的是8-/16-/24-bits 80-series MPU interface.

## 2.1 MPU Interface

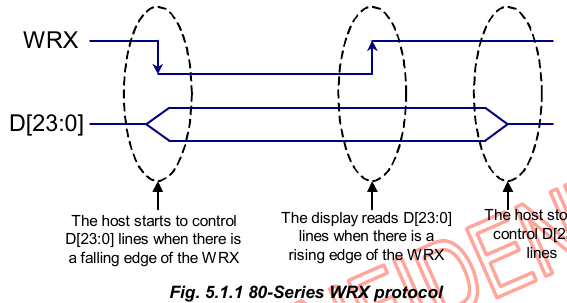


The **8080-series** bi-directional interface can be used for communication between the micro controller and LCD driver chip. **Interface bus width can be selected with IM3,IM2, IM1 and IM0**.



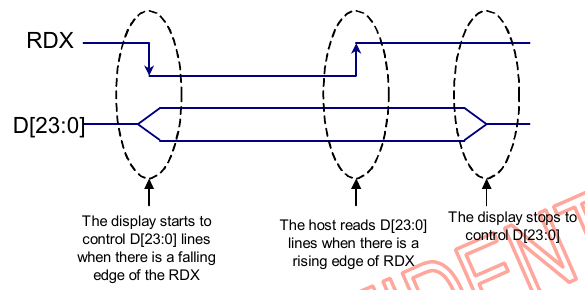
### WRITE CYCLE SEQUENCE

The write cycle means that the host writes information (command or/and data) to the display via the interface. **Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX)** and data signals (D[23:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (=’0’) and vice versa it is data (=’1’).

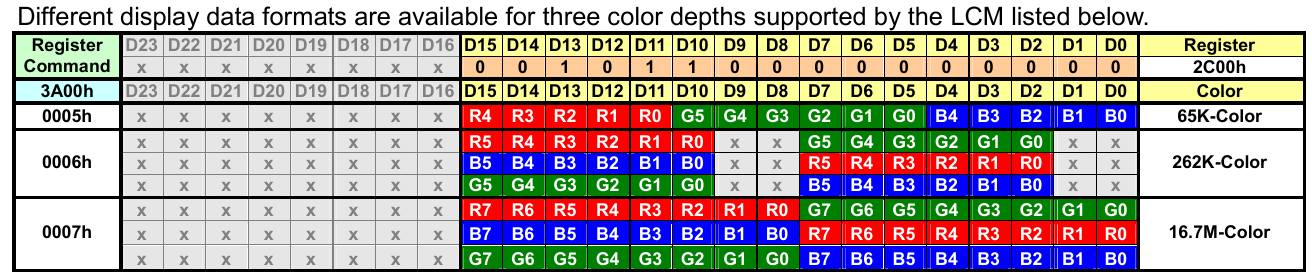


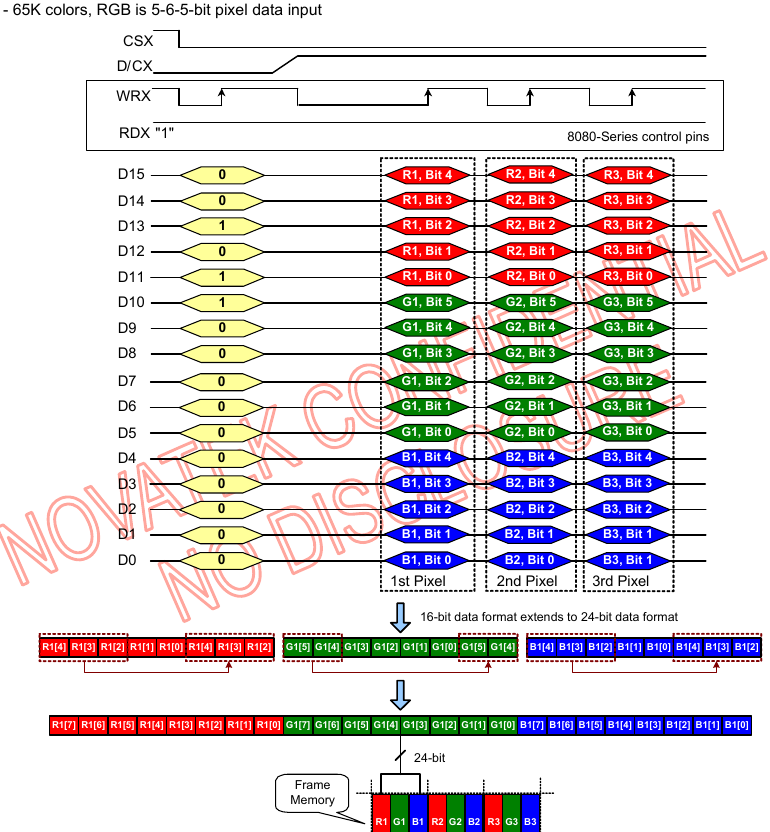
### READ CYCLE SEQUENCE

The read cycle (RDX high-low-high sequence) means that the host reads information from display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

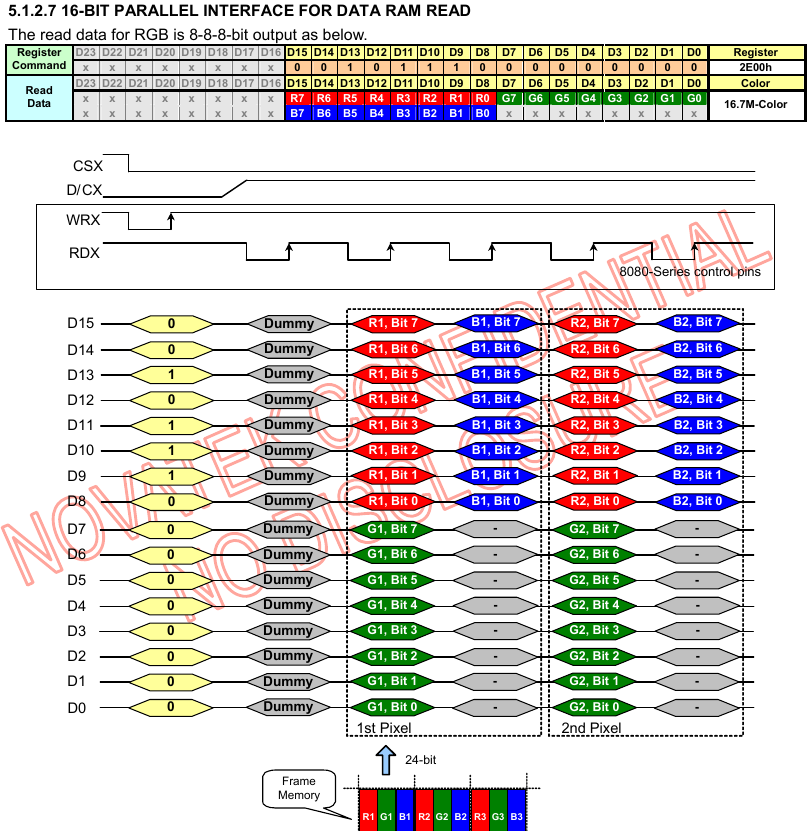


### 16-BIT PARALLEL INTERFACE FOR DATA RAM WRITE



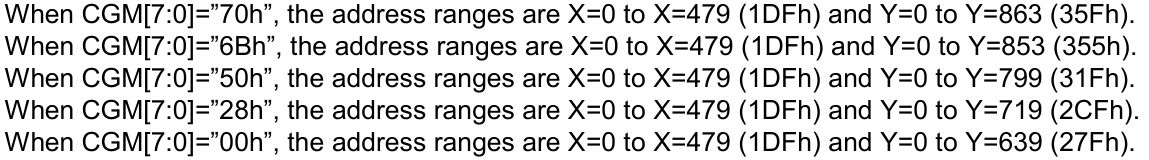


### 16-BIT PARALLEL INTERFACE FOR DATA RAM READ



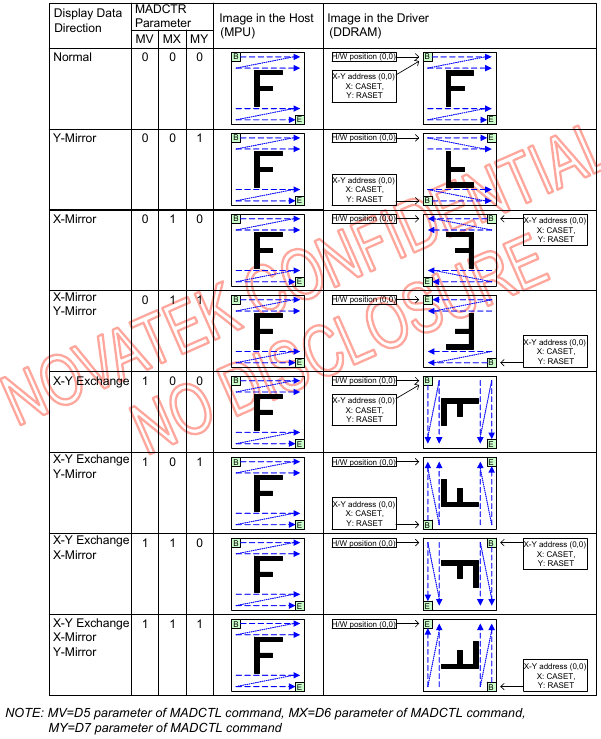
## 2.9 Frame Memory

The NT35510 has an integrated **480 x 864** x 24-bit graphic type static RAM. This 9,953,280 bit memory allows to store on-chip a 480 x RGB x **864**, 480 x RGB x **854**, 480 x RGB x **800**, 480 x RGB x **720** and 480 x RGB x **640** image with an 24-bit resolution (16.7M-color).

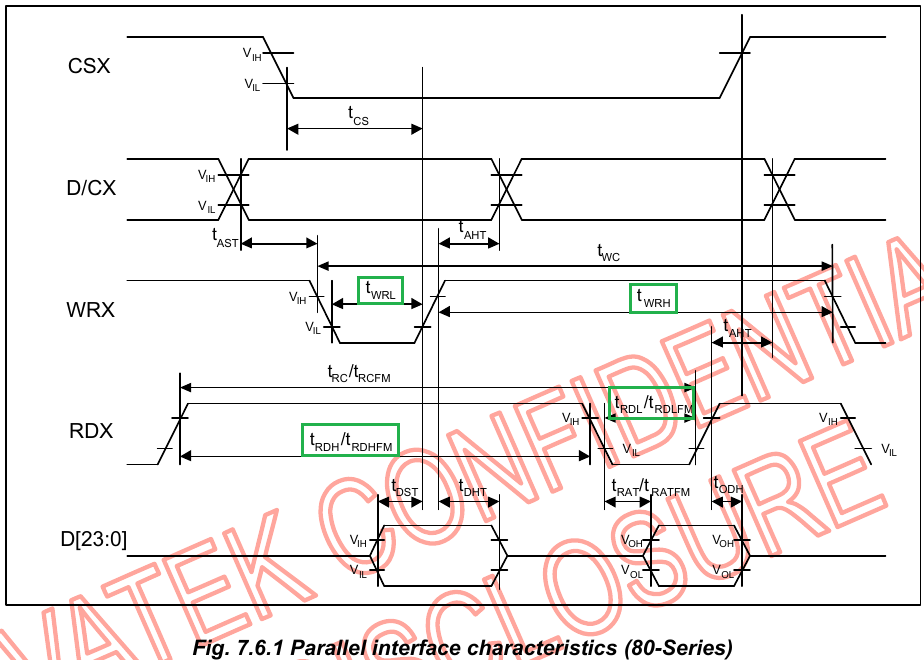


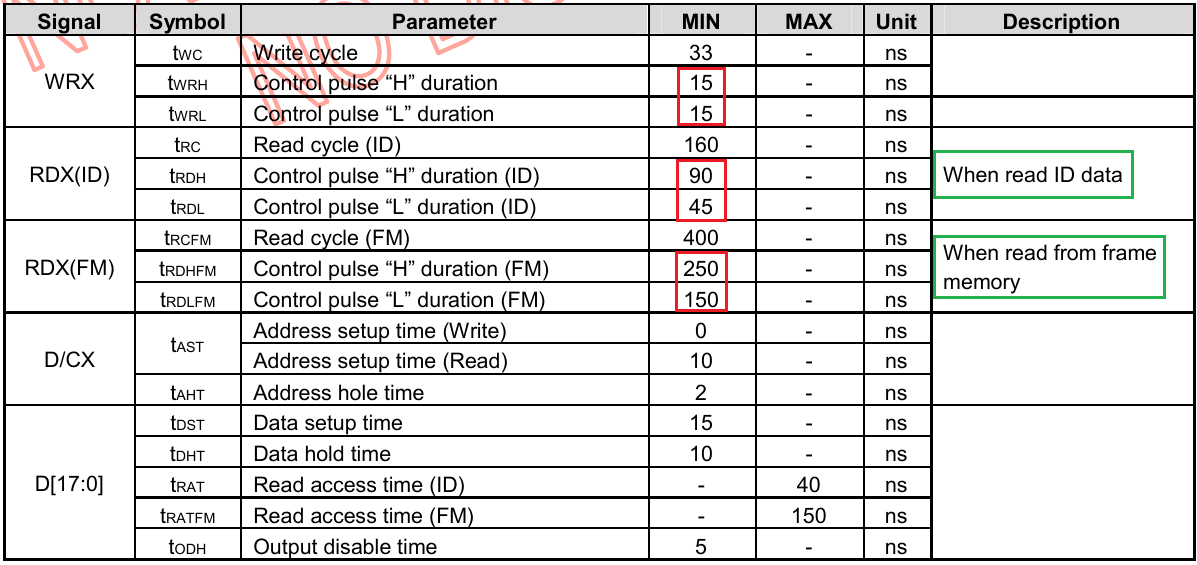
**Before writing to the RAM a window must be defined.** The window is programmable via the command registers **XS, YS** designating the start address and **XE, YE** designating the end address. For example, the whole display contents will be written when CGM[7:0]=”50h”, if the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=479 (1DFh), YE=799 (31Fh).

### 2.9.3 Interface to Memory Write Direction



## 7.6 Parallel Interface Characteristics (80-Series MCU)





The figures above are the timing of NT35510. In our code example, we are using FSMC Mode A for Read and Write, and its diagrams are:

Diagram, schematic

Description automatically generated

Diagram

Description automatically generated

Here, ADDSET is a 4-bit register portion while DATAST is a 8-bit register. Considering we are using 168MHz HCLK, and its CLK cycle is around 6ns. Our code example sets the two time period of **Write** to 18ns, while for **Read**, setting the ADDSET to 96ns, and DATAST to 360ns. However, according to test, DATAST can be set to as low as 30ns.

# FSMC Read/Write to LCD Controller

typedef struct

{

uint16\_t LCD\_REG;

uint16\_t LCD\_RAM;

} LCD\_TypeDef;

#define LCD\_BASE ((uint32\_t)(**0x6C000000** | **0x0000007E**))

#define LCD ((LCD\_TypeDef \*) LCD\_BASE)

This code example uses **FSMC\_Bank1\_NORSRAM4**. According to Reference Manual documents：

Diagram

Description automatically generated

Bank1 – SubBank 4 starts with 0x6C000000.

FSMC uses address signals HADDR[27:0] to address in Bank 1 256M space. HADDR[27:26] determines which sub-bank, and **HADDR[25:1] is assigned to FSMC\_ADDR[24:0] when data width is 16-Bit**.

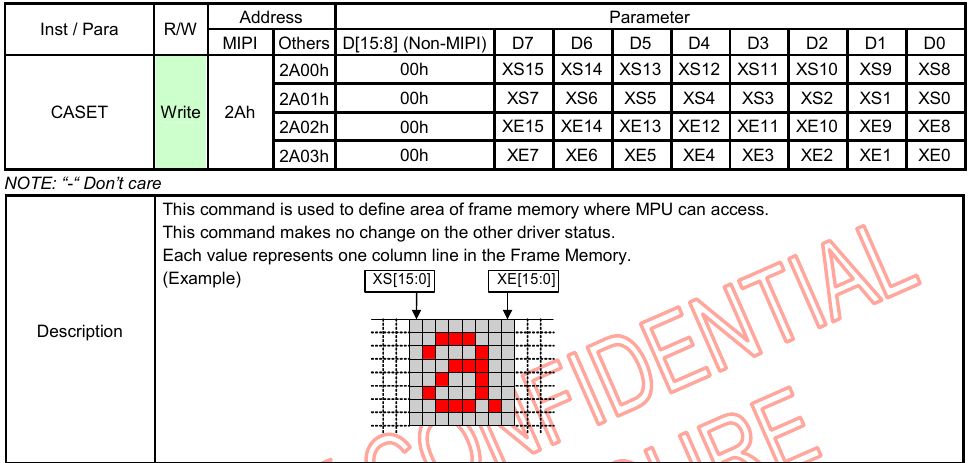
0x7E is 0111 1110, so **LCD\_REG** is @ [**0111 111**]0, and **LCD\_RAM** is @ [**1000 000**]1. **Pay attention to the address in [], there is transition of A6 from 0 (Command) to 1 (Data and parameters).**

# LCD Init

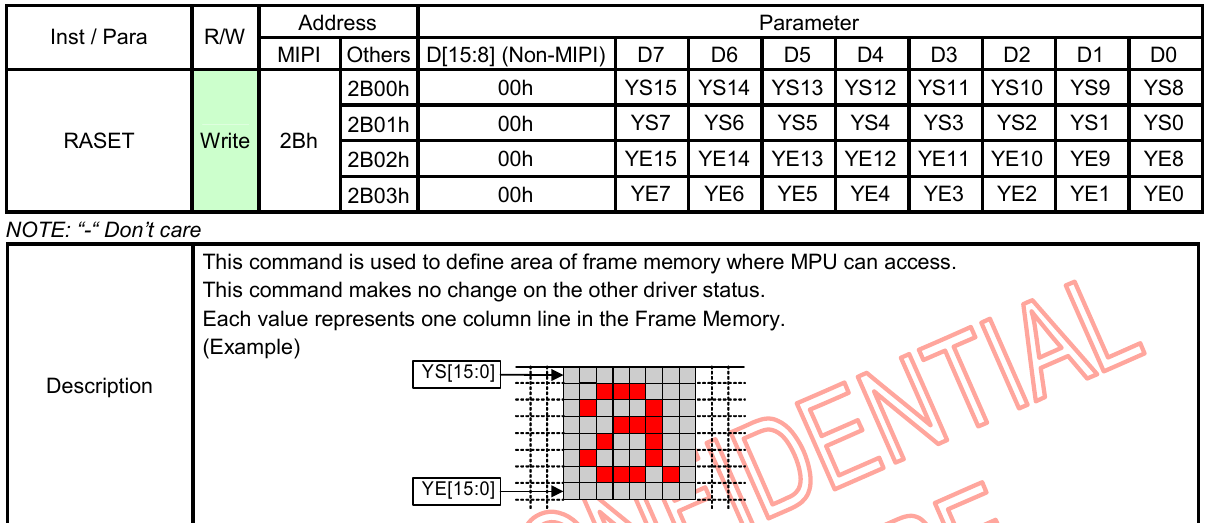
Here we will talk about several registers.

**LCD resolution setting is WIDTH = 480 (X-Axis), HEIGHT = 800 (Y-Axis).**

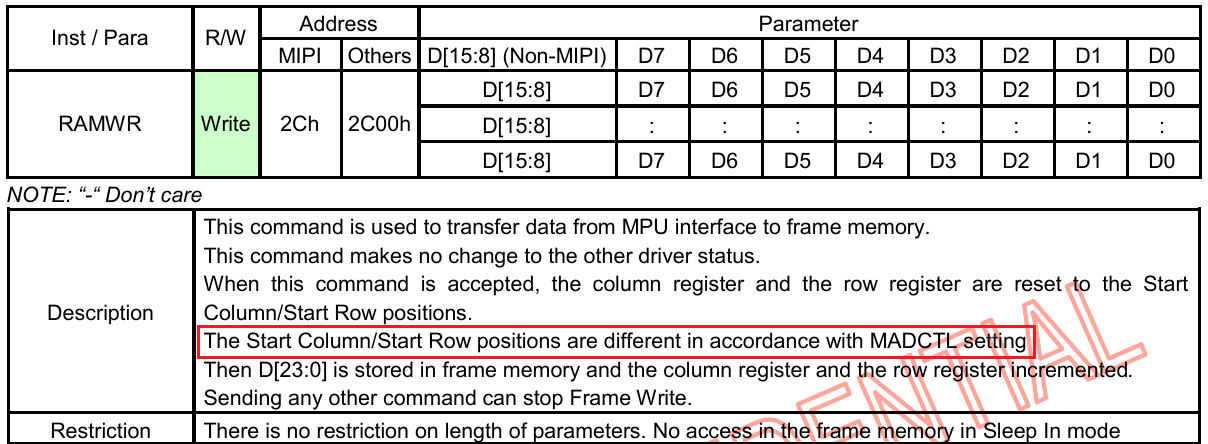
## Column Address Set (2A00h~2A03h)



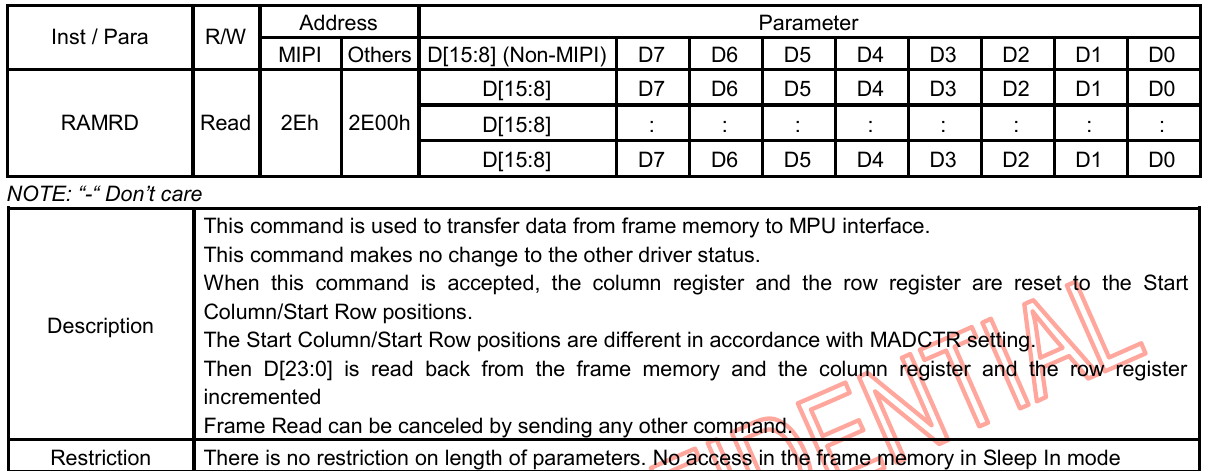
## Row Address Set (2B00h~2B03h)



## Memory Write (2C00h)

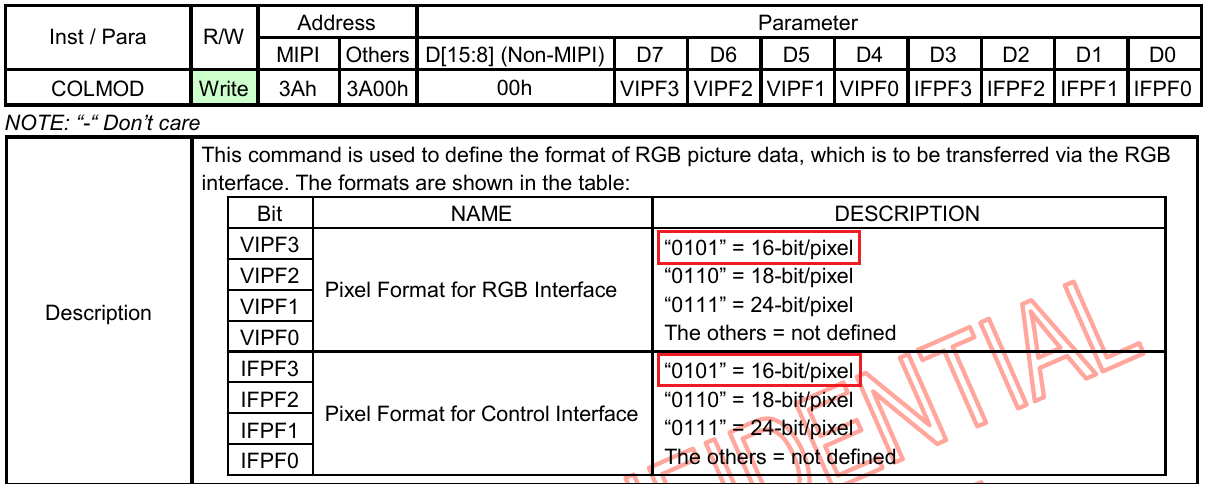


## Memory Read (2E00h)

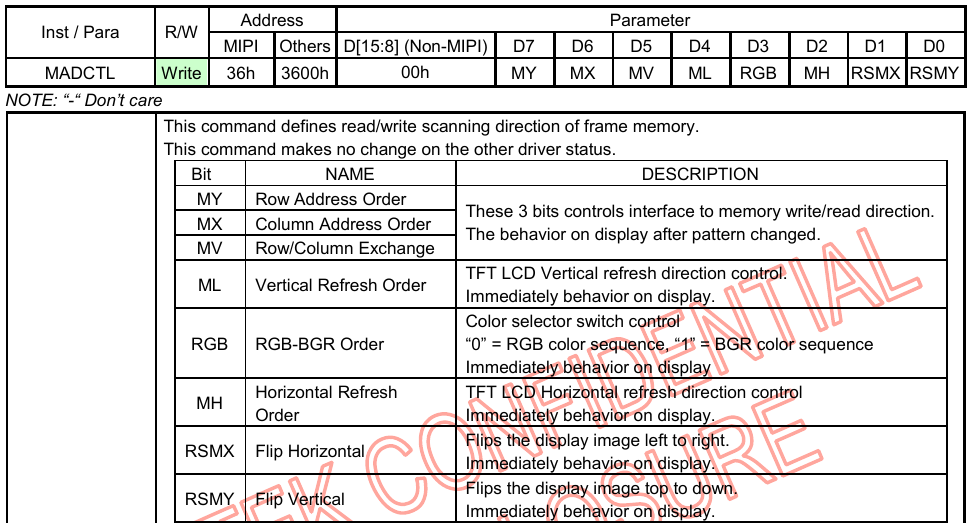


**Memory Write and Memory Read is working with the coordination of X-Y axis.**

## Interface Pixel Format (3A00h)

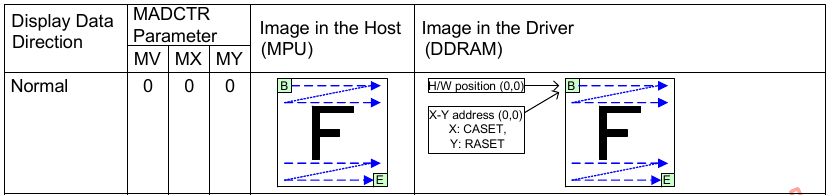


## MADCTL: Memory Data Access Control (3600h)



**This register is set to 0x0000 in our code example.**

* **MV-MX-MY is used to set the orientation between MPU and GRAM.**



* **ML-MH is used to set the refresh orientation.**

