AVR040: EMC Design Considerations

Scope

This application note covers the most common EMC problems designers encounter when using microcontrollers. It will briefly discuss the various phenomena. The reference literature covers EMC design in more detail, and for designers who are going to build products that need to be EMC compliant, further study is highly recommended. A good EMC design requires more knowledge than what can be put into a short application note.

Unlike many other design issues, EMC is not an area where it is possible to list a set of rules. EMC compliance cannot be guaranteed by design; it has to be tested.

It is recommended that readers unfamiliar with EMC design read this document more than once, as some of the subjects described early in this document are more easily understood if the reader has already read the rest of the document.

1 Introduction

Electromagnetic compatibility is a subject most designers did not have to worry about a few years ago. Today, every designer putting a product on the global market has to consider this. There are two main reasons for this:

- The electromagnetic environment is getting tougher.

  High-frequency radio transmitters, like mobile telephones, are found everywhere. More and more systems are using switching power supplies in the power circuit, and the overall number of electronic appliances is increasing every year.

- Electronic circuits are becoming more and more sensitive.

  Power supply voltages are decreasing, reducing the noise margin of input pins. Circuit geometries get smaller and smaller, reducing the amount of energy required to change a logic level, and at the same time reducing the amount of noise required to alter the logic values of signals.

From a designer's point of view, EMC phenomena have to be considered in two different ways:

- How the environment may affect the design (immunity).
- How the design may affect the environment (emission).

Traditionally, the only government regulations have been on the emission side: An electronic device is not allowed to emit more than a certain amount of radio frequency energy to avoid disturbing radio communication or operation of other electronic equipment. Most countries in the world have regulations on this topic.

Additional demands on noise immunity earlier were found only for special applications, like medical equipment, avionics and military applications.

From 1995, Europe introduced regulations on immunity for all electronic products, known as the EMC directive. The purpose of this directive is:

- To ensure that no product emits or radiates any disturbances that may interfere with the function of other equipment.
- To ensure that all products withstand the disturbances present in their operating environment.

At the same time, enforcement of EMC requirements was strengthened: every product made in or imported to Europe must prove to fulfill both emission and immunity requirements before it can be put on the market.

Countries in other parts of the world are also about to introduce similar legal requirements.

The limits for acceptable emission and immunity levels for different product classes and environments are given in various international standards. A more detailed description of these is found in the reference literature.

The EMC directive applies to finished products, but not to components. As a component will not work without being put into a system, the demands are put on the finished system. How the problems are solved internally is left to the designer.

As a result of this, the test procedures required for CE-marking are well suited for testing finished products, but they cannot be used directly for testing components like microcontrollers. The same applies for the test procedures required for FCC approval. The test boards the components are mounted on during test will influence EMC test data for components. These results should therefore only be regarded as informative.

On the other hand, there are test standards (military, automotive and others) that are made to test components directly. These standards specify standardized test boards to make sure that measurements on different manufacturer's components can be compared. These tests are not a requirement according to the EMC directive.

2 EMC Phenomena and EMC Testing

Unlike many other design issues (for instance, power calculations), there are no exact rules for EMC design saying, "Do it like this and it will work." Instead, there are a lot of design suggestions saying, "Do it like this and it may work," or "This is more likely to work, but at a higher cost."

For most applications, it is not possible to prove EMC compliance without actual lab testing. Several new CAD packages include EMC simulations. These may be good design help, saving some extra trips to the test lab, but they cannot replace the final compliance test.

This chapter will give a short introduction to the most common EMC phenomena encountered in MCU system designs. To make it easier to understand the different phenomena, the phenomena and the tests used to emulate them are described together.

2.1 ESD (Immunity Test)

ESD (electrostatic discharge) is a phenomenon most people have experienced. This is what happens if you feel a small electric shock when you touch your kitchen sink or

another grounded object. What happens is that your body has been charged with a small electrostatic charge (easily achieved by walking on synthetic fiber carpets). This charge is released when you touch an object with a different charge or an object connected to ground. For a human being to actually feel the discharge, the voltage must be about 4 kV or more, and it is not difficult to achieve tens of kV.

Figure 2-1. ESD Test Generator
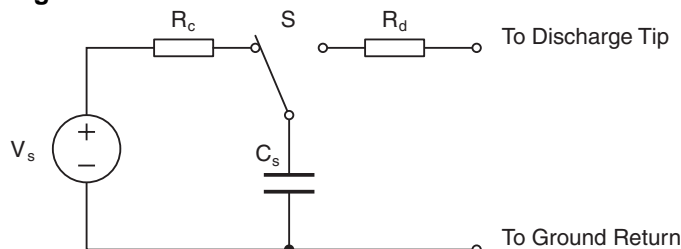
A simple way of modeling this phenomenon is to use a capacitor that will hold the same charge as the body and a series resistor that will release this charge the same way the body does.

Figure 2-1 shows a principle schematic of this setup. C_S is the storage capacitor that equals the capacitance of the human body, R_D is the discharge resistance that equals the resistance of the human body. V_S is a high-voltage power supply, and R_C the series resistance of this power supply. When the switch S is connected to R_C, the capacitor is charged. When the switch S is connected to R_D, the capacitor is discharged through R_D and the device under test, which is connected to or placed near the discharge tip. The value of R_C is of no practical value for what amount of energy is stored in the capacitor or for how this is transferred to the device under test.

Integrated circuits are usually tested according to MILSTD-883.

Here R_C is 1 - 10 MΩ, R_D is 1.5 kΩ and C_S is 100 pF. This is the so-called Human Body Model, which tries to emulate the ESD an integrated circuit may experience as a result of manual handling during board production. The traditional test voltage V_S a CMOS device is expected to handle is ±2 kV. Newer devices like AVR microcontrollers are often rated to ± 4 kV or more.

Another model, the Machine Model, tries to emulate the ESD an integrated circuit will experience from automatic handlers. Here C_S is twice as big, 200 pF. The current limiting resistor R_D is zero (!), but an inductor up to 500 nH may be inserted instead. R_C is 100 MΩ. In this model, the rise time of the current is much higher, and most devices fail at voltages higher than ±500V.

ESD compliance according to the EMC directive is based on IEC 1000-4-2. This standard specifies a Human Body model that tries to emulate the ESD a product will experience as a result of normal use. The component values are therefore slightly tougher here than in MIL-STD-883: R_C is 100 MΩ, R_D is 330Ω and C_S is 150 pF. This means that a product built by circuits rated at 4 kV may not necessarily pass IEC 1000-4-2 at 4 kV without adding some kind of external protection.

Another important difference here: MIL-STD-883 only requires that the device is not damaged by the test. The demand of the EMC directive is stronger: the product shall continue to operate as intended, without being disturbed by the ESD pulse. This requirement is tough, as a high-voltage ESD transient on an input pin may easily change the logic value of the pin. This means that the designer of a microcontroller-based system must either design hardware to make sure that ESD transient never

reaches the I/O pins, or write software that detects and handles such incorrect readings.

2.2 Fast Transient Burst (Immunity Test)

Fast transients or bursts are generally a power line phenomenon, but it can also be a problem on signal lines due to inductive or capacitive coupling. It can occur when a power switch or a relay with an inductive load is operated: When the current is disconnected, a series of small sparks will put high-voltage spikes on the power line.
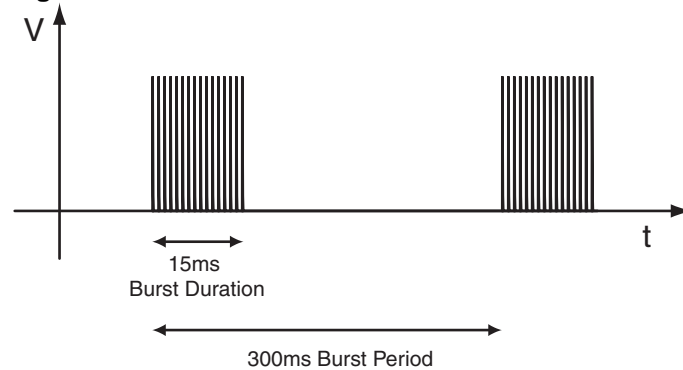
Figure 2-2. Fast Transient Burst
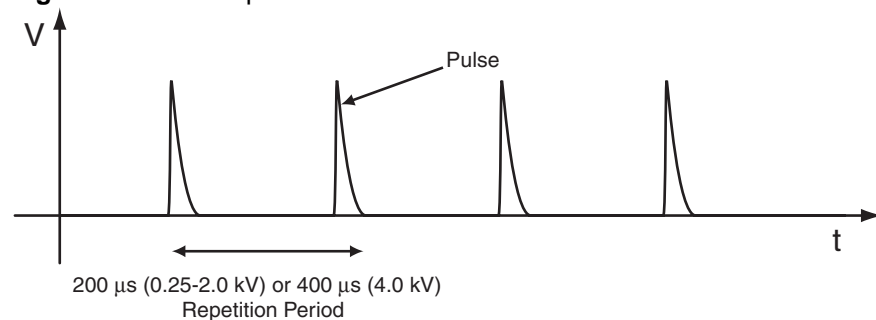

Figure 2-3. Close-up of Burst

Figure 2-2 shows the fast transient burst pulse train used for EMC testing. Figure 2-3 shows a close-up of a burst. Note that the pulse is only about 50 ns wide, this is much smaller than the figure indicates. See IEC 1000-4-4 for details of the pulses and the test setup.

Test voltages on power supply lines are typically 1 kV for protected environment, 2 kV for industrial environment. Severe industrial environments may require up to 4 kV transient testing.

Test voltages on I/O lines are half the values used for power supply lines.

On an I/O line, the pulse may seem similar to an ESD pulse, but there are some very important differences:

- The energy of a single transient pulse may be higher than an ESD pulse at the same voltage, depending on the coupling path into the system.
- ESD testing is performed once or only a few times, with several seconds cool-down time between each pulse. The fast transient pulse is repeated at 5 kHz (2.5 kHz @ 4 kV) for 15 ms: this is one burst. The burst is repeated every 300 ms.

2.3 Surge Immunity Test

This is the mother of all transient tests. It tries to emulate what happens when lightning hits (near) the power network, and the energies involved are high. The capacitance of the energy storage capacitor is up to 20 µF, 200,000 times bigger than the 100 pF used in an ESD test. The test setup is not identical to the one shown in Figure 2-1, a few pulse-shaping components are added, but the basic principle is the same. See IEC 1000-4-5 for details of this test setup.

The surge test is performed only on power supply lines, so this is typically a power supply design issue. However, note that if the design is made to operate on DC power, powered from any approved DC power supply, the designer may still have to incorporate surge protectors on the DC input. The protection of a commercial power supply may be limited to only protecting the power supply itself, resulting in heavy surges on its DC output.

Don't get confused by the similarities between 4 kV ESD testing, 4 kV fast transient burst testing and 4 kV surge. The voltages are the same, but the energy behind them is totally different. Dropping a small rock on your foot may hurt, but you will still be able to walk. Dropping a large rock from the same height will most likely cause severe damage to your foot. Doing this 250 times per second will reduce your shoe size permanently. When the surge boulder falls, you'd rather be somewhere else.

2.4 RF Emission Tests

Radio frequency emissions or noise are among the most difficult problems to handle when designing with fast digital circuits. Problems do not occur only as noise radiated to the outside world. Handling noise issues internally in the system is equally important.

The tests are split into two different types: radiated emission and conducted emission. This split is mainly done to make the tests practical to implement and because conducted emission dominates in the low-frequency range, while radiated emission dominates in the high-frequency range.

Radiated emission is radiated directly from the system and its signal/power cables. This is high-frequency radiation, as a normal PCB is too small to be a good antenna for low frequencies. The EMC directive requires measurements in the range 30 MHz to 1 GHz. American FCC rules require measurements at higher frequencies for certain applications. Lower frequencies are measured directly on the cables.

The high frequencies will typically be generated by harmonics of digital oscillators and I/O pins. Note that the upper frequency generated by a digital circuit is not limited by the clock frequency of the device, but by the rise time of the signals. Lowering the clock speed of the system will therefore not lower the bandwidth of the noise, but will lower the power radiated at high frequencies. (Reducing the number of noisy transitions will reduce the total power of the noise.)

Conducted emission is measured on cables. The EMC directive requires measurements in the range 150 kHz to 30 MHz. Some test standards require measurements down to 9 kHz. Noise in this frequency range is typically from switch mode power supplies and from the base frequencies of digital oscillators and I/O pins.

Long cables will, of course, also act as antennas for both low frequency and high-frequency signals. But if the LF signals are damped sufficiently to be below the limits of the conducted emission test, the radiation from the cable will be negligible. It is therefore not necessary to measure radiated emission in the range below 30 MHz.

Similarly, conducted HF noise on the cables will show in the radiated emission test. If the noise is sufficiently damped to be below the limit for radiated emission, the conducted noise on the cable will be negligible.

Test setups and limits for different applications are given in various standards issued by the International Special Committee on Radio Interference (CISPR). CISPR 22, for instance, covers information technology equipment.

2.5 RF Immunity Test

This test is done to verify that a product can operate as intended even if it is exposed to a strong radio transmitter. The test limit for immunity is much higher than the test limit for emission, so the fields involved are strong.

Be aware that the RF fields a system may be exposed to can be higher than the test limits required for EMC approval. The test limit for conducted RF fields is 3V/m for household applications. A GSM cell phone transmitting at maximum power will produce this field strength at a distance of 3 meters. If the cell phone is closer, the field strength will be higher.

If the intended use of the system may include operation while someone is using a cell phone nearby, it is therefore a good idea to test the system for higher immunity levels than the minimum levels required. Industrial applications usually require 10V/m or higher.

Digital systems usually do not experience problems with this test, but analog parts of the system may.

As for RF emission, the RF immunity tests are split into two different types: radiated and conducted emission.

The test setup for radiated disturbances is given in IEC 1000-4-3; for conducted disturbances the test setup is given in IEC 1000-4-6.

3 Dealing with EMC Phenomena

For most engineers, EMC design is a relatively new subject. Before Europe introduced the EMC directive, it was possible for a company to build and sell their products without paying too much attention to the problem. As long as the products worked as intended and did not interfere with broadcast stations, everything was basically fine.

The three-year transition period from the time the directive was effective in 1992 until it was a requirement in 1995 did not do much to change this. In many companies, the real work did not start until there was no longer a choice. And then, the only option was the hard, expensive way: take an existing product, which perhaps was designed without any thoughts of EMC at all, and try to add the necessary filter, protectors, shielding and whatever to make it EMC compliant. This is the worst possible approach; the cost is high and the results are usually poor.

When designing a new product, it is very important to start thinking EMC from the beginning. This is when all the low-cost solutions are available. A good PCB layout does not cost more in production than a bad one, but the cost of fixing a bad one can be high. One of the most expensive mistakes a designer can make is to believe that EMC is something that can be dealt with after everything else is finished.

What approach to use depends, as always, on estimated system cost and production volume. For a low-volume system, the best way out may be to use expensive

components and system solutions to reduce design time. For a high-volume, low-cost application, it may be better to spend more time and resources on the design to reduce the overall cost of the final product.

3.1 Design Help

If you don't feel that you have the necessary EMC know-how when you start a project, it can be a good idea to get some help from experts. This will keep you from making mistakes that may cost you a fortune to correct later on. There are a lot of consultants, agencies and companies specializing in EMC design and EMC training. Adding more people in the design phase will also reduce design time and time to market.

Good EMC design requires a lot of knowledge, but you do not have to acquire this knowledge the hard way; by trial and error. Others have done this already.

4 Design Rules

4.1 Identify the Noise Sources

A very important general rule is that all types of noise should be handled as close to the source as possible, and as far away from the sensitive parts of a circuit as possible. This, of course, means that the task of identifying these sources is very important.

4.1.1 Transmitted Noise

In many microcontroller systems, the microcontroller is the only fast digital circuit. In such systems, the most important internal noise source is the microcontroller itself, and the resources used for preventing conducted and emitted RF are best used close to the microcontroller. This will reduce the amount of RF energy that reaches I/O cables and other parts of the system that may act as transmitting antennas.

4.1.2 Received Noise

The sources of received noise are usually outside the system, and therefore out of reach for the system designer. The environment is what it is, and the first possibility for the system designer to do something about the noise is on the system inputs and on the power cables. For a system delivered with dedicated cables, it is even possible to start on the cable itself. A good example here is a computer monitor, where you quite often see a filter put next to the VGA plug you connect to your computer. On other systems, the first chance comes with the I/O connectors. For a hand-held, battery-powered application without any cables, this is not applicable, but then this problem is similarly smaller. If external noise can be prevented from entering the system at all, there will be no immunity problems.

4.2 The Path to Ground

The best way to avoid noise problems is to generate no noise in the first place, but this is usually not applicable. Most kinds of noise are side effects of intended behavior of other parts of the system, and therefore cannot be avoided.

All kinds of currents, AC or DC, high-power or low-power, signals or noise, are always trying to find the easiest path to ground. The basic idea behind many EMC design techniques is to control the path to ground for all signals, and make sure that this path

is away from signals and circuits that may be disturbed. For transmitted noise, this means making sure that the noise will find a path to ground before it leaves the system. For received noise, it means making sure that the noise will find a path to ground before it reaches sensitive parts of the system.

4.3 System Zones

Handling every EMC problem at once is a very complex task. It is therefore a good idea to split the system into smaller subsystems or zones, and handle these individually. The zones may, in some cases, only be different areas of the same PCB. The important part is to have control of what happens inside one zone, and how the zones interact. For each zone, the designer should have some idea about what kind of noise the zone may emit, and what kind of noise it may have to endure. All lines going in and out of a zone may require some kind of filter. It is also very important to be aware about how noise may be radiated from one zone to another. Local shielding of very noisy and/or very sensitive circuits may be necessary.

The split may be done in two ways or a combination of these:

- The zones may be put apart from each other to separate noisy circuits from sensitive ones. The typical example here is a line-powered system containing both analog and digital circuits, where the (switch mode) power supply, the digital circuits and the analog circuits are put on different areas of the PCB.

- The zones may be put inside each other. The noise going into and out of the innermost zone will then have to pass several layers of filters and/or shielding. The total noise reduction will then be much more efficient than what can be received by one layer. An example here is a particularly sensitive analog circuit, perhaps with its own shield, on the analog part of a PCB inside a shielded enclosure with filtered I/O connectors. Another example is a fast microcontroller with fast communication to a nearby memory, and slower communication to other parts of the system. Then the MCU and the memory can be defined as the inner zone – the noisiest part. All lines leaving this zone should then be filtered, making sure that none of them carry the highest-frequency noise further out. The next level of filters may then be on the edge of the "digital zone", and perhaps also a third layer of filtering on the system I/O ports is used to reduce emitted noise even further. Three layers of filters may sound expensive, but three simple filters may cost much less than an advanced "one-filter-handles-all" solution.

4.4 RF Immunity

Long I/O and power cables usually act as good antennas, picking up noise from the outside world and conducting this into the system. For unshielded systems, long PCB tracks may also act as antennas. Once inside the system, the noise may be coupled into other, more sensitive signal lines. It is therefore vital that the amount of RF energy allowed into the system be kept as low as possible, even if the input lines themselves are not connected to any sensitive circuit.

This can be done by adding one or more of the following:

- Series inductors or ferrite beads will reduce the amount of HF noise that reaches the microcontroller pin. They will have high impedance for HF, while having low impedance for low-frequency signals.

- Decoupling capacitors on the input lines will short the HF noise to ground. The capacitors should have low ESR (equivalent series resistance). This is more important than high capacitance values. In combination with resistors or inductors,

the capacitors will form low-pass filters. If the system is shielded, the capacitors should be connected directly to the shield. This will prevent the noise from entering the system at all. Special feed-through capacitors are designed for this purpose, but these may be expensive.

- Special EMC filters combining inductors and capacitors in the same package are now delivered from many manufacturers in many different shapes and component values.

4.5 ESD and Transients

Handling ESD is usually quite simple: make sure that the user cannot touch the sensitive parts of the system. This is, in most cases, taken care of by the equipment enclosure and only I/O pins leaving the system need special attention. However, ESD discharges may induce currents in nearby paths, causing incorrect values of the signals on these.

Keep in mind that both ESD pulses and other types of transients are very high-frequency phenomena, and that stray capacitance and inductance have a very important influence of their behavior. A transient on one line may also affect the behavior of other signals nearby.

The important thing is to make sure that the most efficient path to ground is one that does not affect the system. If, for instance, the most efficient path to ground for an ESD pulse is along the I/O line, to the microcontroller pin, through the ESD protection diode and then to ground, a logic high input may be read as low. If the system software cannot be made to handle this (and that is usually the case), the system requires some kind of hardware that will create a more controlled path to ground.

The RF filters listed above will, of course, also work on ESD and transients, and may, in some cases, be sufficient. But reducing a 4 kV spike to a 4V spike requires a very strong filter. It can by done by large series resistors, but that is not always an option. Large series resistors on input lines will increase the impedance of the ground path described above. This will reduce the amount of noise that reaches the microcontroller pin. The disadvantage of this is that the system also gets high impedance for low frequency and DC signals, and this is therefore not useful for I/O pins that are also used as outputs.

Then over-voltage protectors are a better solution. There are many types of these, most of them acting as very fast zener diodes. They will have very high impedance to ground as long as the I/O line voltage is within the specified limits, but will switch to a very low impedance value when the voltage is too high. A transient is then very effectively shorted to ground.

4.6 Power Supply, Power Routing and Decoupling Capacitors

One of the most common reasons for EMC problems with microcontroller products is that the power supply is not good enough. Correct and sufficient decoupling of power lines is crucial for stable microcontroller behavior, and for minimizing the emitted noise from the device.

Looking at the datasheet for an AVR microcontroller, one can be fooled to believe that power supply is not critical. The device has a very wide voltage range, and draws only a few mA supply current. But as with all digital circuits, the supply current is an average value. The current is drawn in very short spikes on the clock edges, and if I/O lines are switching, the spikes will be even higher.

The current pulses on the power supply lines can be several hundred mA if all eight I/O lines of an I/O port changes value at the same time. If the I/O lines are not loaded, the pulse will only be a few ns.

This kind of current spike cannot be delivered over long power supply lines; the main source is (or should be) the decoupling capacitor.
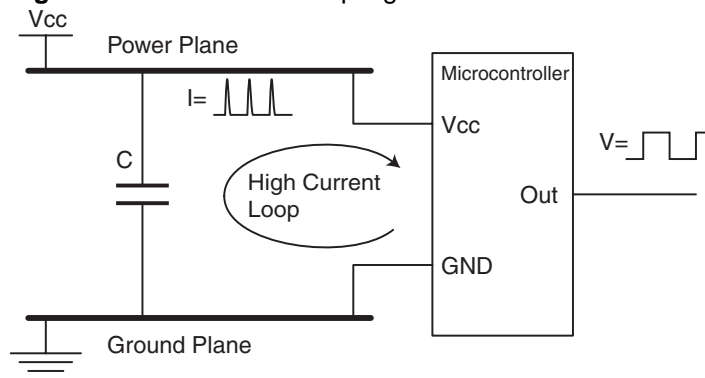
Figure 4-1. Incorrect Decoupling

Figure 4-1 shows an example of insufficient decoupling. The capacitor is placed too far away from the microcontroller, creating a large high current loop. The power and ground planes here are parts of the high current loop. As a result of this, noise is spread more easily to other devices on the board, and radiated emission from the board is increased even further. The whole ground plane will act as an antenna for the noise, instead of only the high current loop.

This will be the case if the power and ground pins are connected directly to the planes (typical for hole-mounted components) and the decoupling capacitor is connected the same way. The same is often seen for boards with surface-mount components if the integrated circuits are placed on one side of the board and the decoupling capacitors are placed on the other.

Figure 4-2. Correct Placement of Decoupling Capacitor
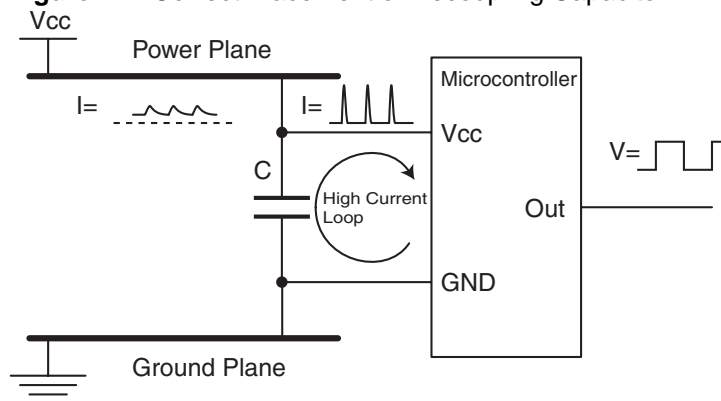

Figure 4-2 shows a better placement of the capacitor. The lines that are part of the high current loop are not part of the power or ground planes. This is important, as the power and ground planes otherwise will spread a lot of noise.

Figure 4-3 shows another improvement of the decoupling. A series inductor is inserted to reduce the switching noise on the power plane. The series resistance of the inductor must, of course, be low enough to ensure that there will be no significant DC voltage drop.

Generally, the AVR devices where power and ground lines are placed close together (like the AT90S8535) will get better decoupling than devices with industry standard pinout (like the AT90S8515), where the power and ground pins are placed in opposite corners of the DIP package. This disadvantage can be overcome by using the TQFP package, which allows decoupling capacitors to be placed very close to the die. For devices with multiple pairs of power and ground pins, it is essential that every pair of pins get its own decoupling capacitor.

Figure 4-3. Decoupling with Series Inductor
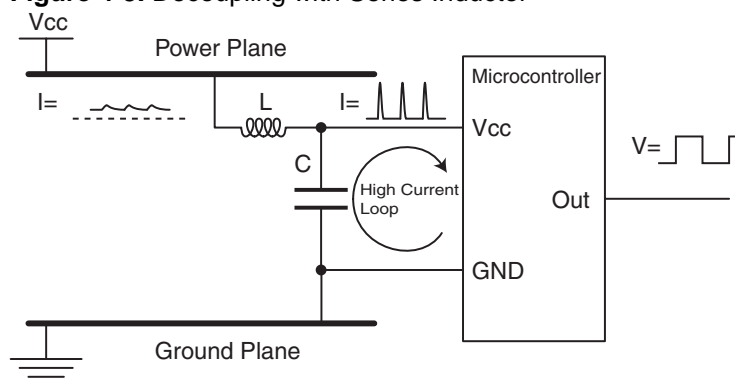
4.7 PCB Layout and Grounding

4.7.1 Current Loops and Signal Grounding

Current can only flow in loops. This is true for signals as well as for power supply current. Unfortunately, a current loop will emit noise, and the larger the loop, the larger the noise. Noise also increases with current and with frequency. A large loop is also more likely to receive noise. Loops should therefore be kept as small as possible. This means that every line that may emit or receive noise should have a return path to ground as close to the line as possible.

The best way to make sure that every noisy track has such a return path is to add a complete ground plane to the board. Then the area of the loop will only be the length of the track times the distance between the track and the ground plane. This area is usually much smaller than what can be achieved by routing ground paths, so the noise from a board with a ground plane is therefore much less than the noise from a board without a ground plane.

4.7.2 Ground Planes

In many designs, it looks like the ground plane is defined to be "all the copper not used for something else, connected to ground somewhere." This will not be an effective ground plane.

Note that for a high frequency signal, the return path in a ground plane will be exactly under the track, even if this path is longer than the direct route. This is because the return path will always be the path of least impedance, and for a high-frequency signal, this is the path with the smallest loop, not the path that has lowest DC resistance.

For circuits that include both digital and analog circuits, the ground plane may be divided into an analog ground plane and a digital ground plane. This will reduce the interference between the analog and digital parts of the system.

4.7.3 Board Zoning

System zoning, as described on System Zones can also be applied to a single PCB.

Noisy parts of a system, like a digital circuit or a switch mode power supply, should be made as small as possible, reducing the size of current loops that will act as emitting antennas. Similarly, sensitive parts of a system, like an analog measurement circuit, should be made as small as possible, reducing the size of current loops that will act as receiving antennas. And of course, the noisy part of a system should be kept as far away from the sensitive ones as possible.

Remember that in both cases the important part is reducing the size of the current loops, not the physical board area. Routing in ground planes to save space should therefore be avoided, unless thorough analysis shows that the ground return paths of other signals will not be affected.

4.7.4 Single-layer Boards

Single-layer boards are used in many commercial applications due to their low cost.

However, from an EMC point of view they are the most demanding boards to work with, as it is not possible to incorporate a ground layer on the board. This may increase the need for external components or shielding to achieve EMC compatibility, especially at high clock speeds. The layout of a single-layer board will require very good EMC design skills from the designer, as the layout very easily ends up having large loops that will act as antennas. It is always a good idea to use wires and straps to overcome some of the worst routing problems, but the task is still demanding.

4.7.5 Two-layer Boards

If possible, one of the layers should be used as a dedicated ground plane and only that.

If signals are routed in the ground plane, this may interfere with the return paths of the track on the other side. This kind of routing will therefore require detailed analysis of every track on the board, otherwise the whole ground plane may be wasted.

Figure 4-4. Ground Grid

Top Layer Track   Bottom Layer Track   Via
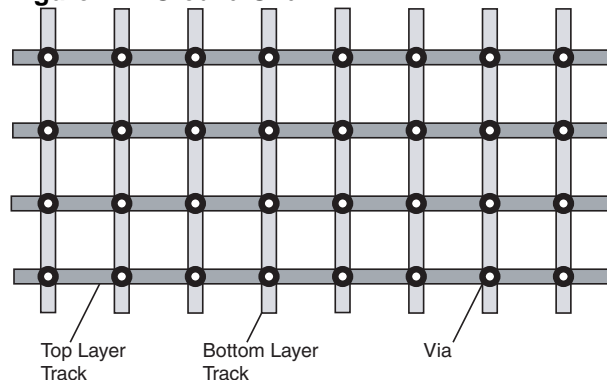
One way of designing a ground plane on a two-layer board and still allow routing on both layers, is to design a ground grid as shown in Figure 4-4. Here every path will have a ground return nearby, creating a relatively small loop. How large the cells and how wide the tracks should be will depend on the application. Higher currents and higher frequencies will require wider tracks and smaller cells.

It is very important to first put the ground grid in place, as it will be very difficult to make room for it after all other tracks have been placed. If required, a segment of the ground grid can be moved to the opposite side of the board to make routing easier or to make room for components. But it is "illegal" to delete segments. If a via or a track has to be moved, put an extra one in the grid to make sure that no cells are larger than the others.

A ground grid is not as good as a complete, unbroken ground plane, but it is better than routing ground just like any other signal.

Another way of designing a similar ground plane is to fill all unused space on both sides of the board and connect the ground planes together with vias wherever needed. It is very important to make sure that the ground plane at every part of the board covers at least one layer and that enough vias are used so the total ground area becomes as complete as possible. This way of creating a ground plane can also be combined with the ground grid described above. Start with a ground grid, then route the rest of the board and fill all unused areas with ground planes. Some of the vias in the ground grid may, in this case, be removed afterwards.

For a mixed signal board with both analog and digital circuits, it is recommended to use an unbroken ground plane for the analog part of the board, as this will provide better noise immunity for sensitive analog circuits.

4.7.6 Multi-layer Boards

When three or more layers are used, it is essential that one plane is used as a ground plane. It is also recommended to use one layer as a power plane if four or more layers are used. These two planes should then be placed next to each other in the middle of the board, to reduce power supply impedance and loop area. It is not a good idea to place the power and ground planes as the outer layers to act as shields. It does not work as intended, as high currents are running in the ground plane. A shield layer would have to be a second pair of ground layers.

4.8 Shielding

In some cases it is not possible to get the noise levels of a system low enough without adding a shield. In other applications a shield may be used because it is easier to use a shield than to achieve low noise levels by other means.

Depending on the application, the shield may cover the whole system or only the parts of the system that need it most. If the zone system is used in the design, it is easy to determine which zone(s) that need to be shielded.

In either case, the shield must be completely closed. A shield is like a pressurized container: almost good enough is as bad as nothing at all. As described earlier, all lines entering or leaving a zone need to be filtered. A single line that is not filtered will act like a single hole in a bucket of water. It will cause a leak.

A semi-closed shield, connected to ground, may still reduce noise. It will act as a ground plane, reducing the size of the loop antennas.

A common rule of thumb says that the maximum dimension of any mechanical slit or hole in the shield should be less than 1/10th of the minimum wavelength of the noise. In a system where the maximum significant noise frequency is 200 MHz, this wavelength is 150 cm, and the slits should be less than 15 cm. But such a hole will still cause some reduction of the effectiveness of the shield. A hole that does not

affect the effectiveness of the shield has to be less than 1% of the minimum wavelength, in this case 1.5 cm.

It may turn out that a 100%-effective shield is not required, though. The filters on the I/O and power lines are usually more important. In many applications, where high-frequency noise (>30 MHz) is dominant, it may not even be necessary to use a metal shield. A conductive layer on the inside of a plastic housing will, in some cases, be sufficient.

4.9 AVR-specific Solutions

Most of the items described earlier in this document are general. There are, however, a few important AVR-specific subjects a designer should keep in mind.

Note that the measures described in this document are not required in all cases. In most cases, only a minimum of external components (decoupling capacitor, etc) is required. In fact, the embedded low-cost solutions such as the BOD and internal pull-ups will do the trick in many designs.

4.9.1 General I/O Pin Protection

All general I/O-pins have internal ESD protection diodes to GND and Vcc, as shown in Figure 4-5. If exceeding pin voltage 'Absolute Maximum Ratings' in the datasheet, resulting currents can harm the device if they are not limited accordingly. For parts with LCD-driver, the same situation on SEG pins used for general I/O can also influence the LCD voltage level.

Figure 4-5. AVR I/O Pin Protection
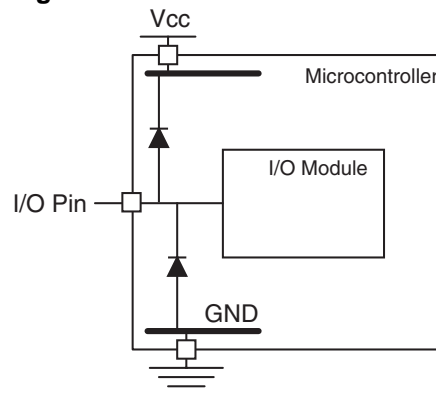
4.9.2 Reset Pin Protection

During parallel programming, a 12V signal is connected to the Reset pin. There is therefore no internal protection diode from Reset to V_{CC}; there is only one from GND to Reset. See Figure 4-6.

Figure 4-6. Reset Pin Input Protection
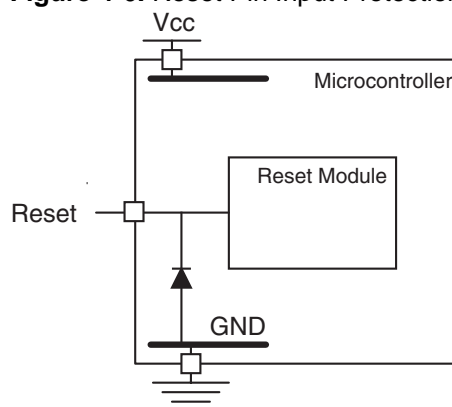
To achieve the same protection on Reset as on other I/O pins, an external diode should be connected from Reset to V_{CC}. A normal small-signal diode will do. In addition, a pull-up resistor (10K typical) and a small filter capacitor (4.7 nF) should be connected as shown in Figure 4-7.

All this, of course, is not needed if Reset is connected directly to V_{CC}, but then external reset and In-System Programming (ISP) is disabled, too.

If high ESD protection of Reset is not required, or is achieved by other components, the diode may be omitted. The resistor and capacitor are still recommended for optimum Reset behavior.

The diode must also be omitted if In-System Programming of devices like ATtiny11, which can only be programmed using 12V, is required. Then one of the ESD protection methods described earlier may be used instead.

Figure 4-7. Recommended Reset Pin Connection
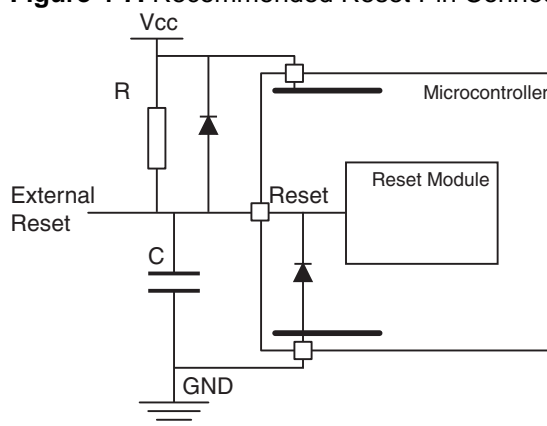
4.9.3 Oscillators

As the AVR microcontroller family is running directly on the clock Oscillator, the Oscillator frequency for a specific throughput is relatively low compared to devices that divide the clock by 4, 8, or 12. This reduces the emitted noise from the Oscillator, but the Oscillator still will be among the noisiest parts of the chip.

High-frequency Oscillators are quite delicate devices and are, therefore, sensitive to external noise.

In addition, the Oscillator pins are generally more sensitive to ESD than other I/O pins.

Fortunately, it is easy to avoid these problems.

Keep the Oscillator loop as tight as possible. Place the crystal/resonator as close to the pins as possible. Connect the decoupling capacitors (or the ground terminal of the resonator) directly to the ground plane. Even boards without ground plane should have a local plane under the oscillator. This plane must be connected directly to the ground pin of the microcontroller.

Care should also be taken when using an external clock to drive the AVR. If the clock source is far away from the AVR, the clock line will be a strong noise emitter and may also act as a receiving antenna for transients (and other types of noise) that may cause incorrect clocking of the AVR.

A buffer should therefore be placed on the clock line. A filter in front of the buffer will help remove incoming noise.

5 References

Tim Williams: "EMC for Product Designers," 2nd edition

Newnes, Oxford, 1996
ISBN 0 7506 2466 3

The EMC directive

89/336/EEC and 92/31/EEC

IEC Standards: IEC 1000 series and 61000 series

CISPR standards: All

6 Useful Links

6.1 Vendors

Murata

Home page: http://www.murata.com

Harris Suppression Products Group

(now a business unit of Littelfuse, Inc)
Home page: http://www.intersil.com/tvs/tvs.asp

TDK

Home page: http://www.tdk.com

EMC components:

http://www.component.tdk.com/components/emc.html

6.2 Organizations

IEC

The International Electrotechnical Commission
Home page: http://www.iec.ch

CENELEC

European Committee for Electrotechnical Standardization

Home page: http://www.cenelec.be

JEDEC

Joint Electron Device Engineering Council

Home page: http://www.jedec.org

SAE

Society of Automotive Engineers

Home page: http://www.sae.org

FCC

Federal Communications Commission

Home page: http://www.fcc.gov/

EIA

Electronic Industries Alliance

Home page: http://www.eia.org/

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Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
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Fax: (33) 4-42-53-60-01

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Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
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Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive
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74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

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Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
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Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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