Experiment EL1

Digital logic components

Before you start to perform an experiment you are obliged to have mastered the following theoretical subjects:

1. Definition of high and low logic states for TTL and CMOS logic circuits. [1-3,6]
2. Description of static properties of logic gates. The most important characteristics and parameters. [1-4]
3. What is DC noise immunity of logic gates? [1,2,6]
4. Graphic symbols of basic logic gates: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR, and buffet gate. [1-5]
5. Comparison of internal structure of NAND gates of TTL and CMOS family. [1-5]

Purpose

The purpose of this experiment is to investigate the static input, transfer, and output characteristics of a TTL logic gate.

Description of measurement method

In this experiment a single logic NOT gate from TTL (transistor-transistor logic) family will be investigated. The static characteristics of the gate will be studied by "step by step" strategy employing some digital multimeters (DMM) and the following components provided with the gate in the experimental kit:

a) the potentiometer P_1 working as a voltage divider, which allows you to adjust an input voltage in the range from 0 to 5V,
b) the potentiometer P_2 working as a resistive load, which allows you to adjust an output current in the range from 0 to about 15mA (slightly less than the maximum static output current given in TTL data sheet),
c) alternative load of the output of the gate in the form of inputs of further logic gates, where the number of inputs may be selected in the range from 1 to 12.

To find the input characteristic $I_{in} = f(U_{in})$ of the gate you will perform measurements of input current I_{in} for various selected values of the input voltage U_{in}. In the case of transfer characteristics $U_{out} = f(U_{in})$ you will investigate only one characteristic from the family, which is related to a certain selected load of the gate output. On the occasion of this study also the dependence of the current supply I_s on U_{in} will be registered. Moreover, two output characteristics $I_{out} = f(U_{out})$ will be investigated separately for the low and high output state.

Since several logic NOT gates are placed in a single chip, a circuit based on UCY 7430 chip with one 8-input NAND gate is applied. Such approach allows you to measure supply current I_s of the single gate without perturbation cased by another gates in the same chip. On the front panel of the experimental kit only one input of the NAND gate is brought out, while others are always held in high state.

Experimental procedure

A. Input characteristic of a logic gate

1. Connect the power supply (Z - DF1731SB3A), milliammeter (mA), voltmeter (V) and jumper to the experimental module with logic gate as in Fig. 1.
   WARNING:
   a) the experimental module must be supplied from the power supply channel that provides constant output voltage +5 V (sockets on the right side of the power supply). Do not use the outputs allowing voltage adjustment,
   b) Do not connect +5V voltage output directly to the output nor input of the gate.
   Ignoring these recommendations threatens to damage the device.
2. Set measuring range to 2 mA DC on the DMM milliammeter (measurement of I_{in}).
3. Set measuring range to 20 V DC on the DMM voltmeter (measurement of U_{in}).
4. After obtaining permission from your supervisor switch on the multimeters and power supply. Check out the status of the red LED located on the +5 V line in the experimental module.
5. Use the potentiometer P_1 to change the voltage U_{in} on the input of the NOT gate from 0 to 5V and determine the dependency of the input current I_{in} on U_{in}. Special attention should be paid to measure U_{in} in the range 1.3 ÷ 1.6 V, where small changes in U_{in} may cause sudden changes in I_{in}. Write down the results in Table 1.

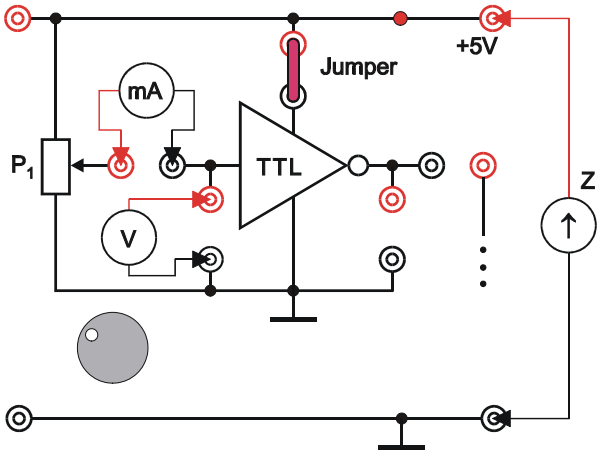

Fig. 1. Setup for measuring input characteristic of a logic gate.

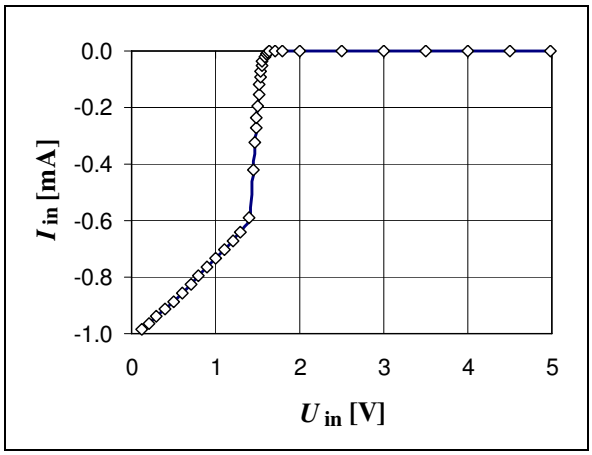

Fig. 2. Typical input characteristic of a TTL logic gate.

#	U_{in} [V]	I_{in} [mA]
1		
2		

Table 1. Data table for measurements of input characteristic of the logic gate.

B. Transfer characteristic and power dissipation of a logic gate

1. Connect the circuit shown in Fig. 3. Set measuring range to 200 mA DC on the DMM milliammeter (mA) and 20 V DC on the voltmeters (V1) and (V2).
2. If the supervisor did not recommend any other settings, use the rotary switch "n" to select a load of the gate output by n = 10 inputs of further logic gates.
3. Use the potentiometer P_1 to increase the input voltage U_{in} from 0 to 5V and determine the dependency of the output voltage U_{out} and quiescent supply current I_s on U_{in}. Special attention should be paid to measure U_{in} in the range 1.2 ÷ 1.5 V, where small changes in U_{in} may cause sudden changes in U_{out} and I_s. Write down the results in Table 2.

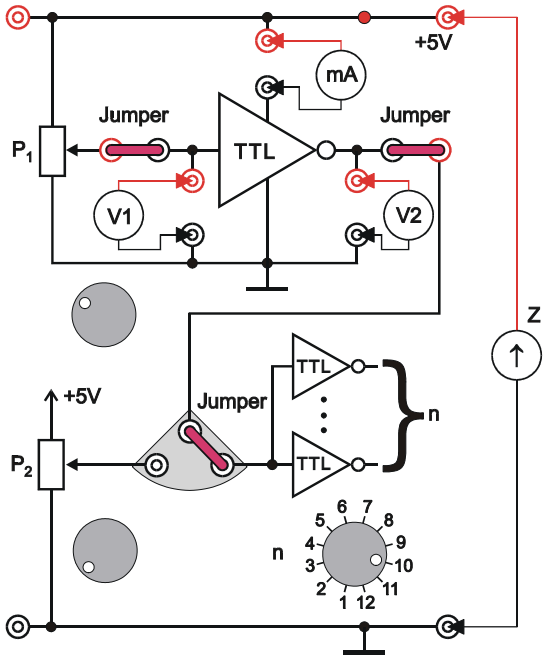

Fig. 3. Setup for measuring transfer characteristics and quiescent supply current of a logic gate.

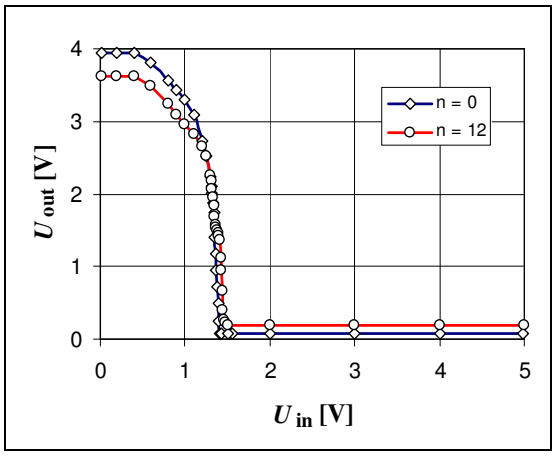

Fig. 4. Typical transfer characteristics of a TTL inverter.

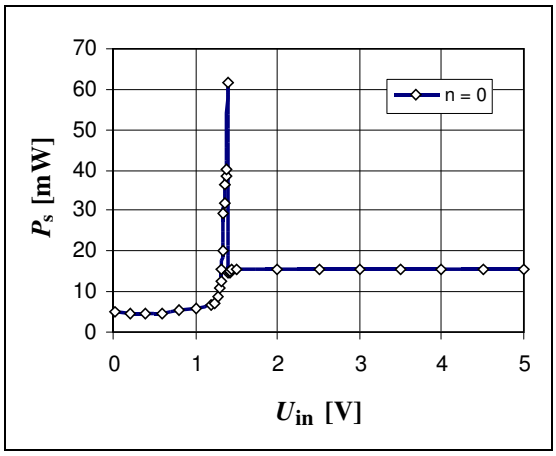

Fig. 5. Typical power dissipation of a TTL logic gate versus input voltage.

#	n = …			
	U_{in} [V]	U_{out} [V]	I_s [mA]	P_s [mW]

Table 2. Data table for measurements of transfer characteristics and power dissipation of the logic gate.

C. Output characteristic of a logic gate

1. Connect the circuit shown in Fig. 6. Set measuring range to 200 mA DC on the DMM milliammeter (mA) and 20V DC on the voltmeter (V).
2. Turn the potentiometer P_1 fully counter clock-wise to set the low state at the gate input.
3. Use the potentiometer P_2 to change the output current $I_{out,H}$ in the entire available range (from 0 to about 15 mA) and determine the dependency of the output voltage $U_{out,H}$ on $I_{out,H}$ for the high state at the gate output. Write down the results in Table 3.
4. Turn the potentiometer P_1 fully clock-wise to set the high state at the gate input. Repeat the procedure described in step 3 and write down the results $U_{out,L}$ and $I_{out,L}$ related to the low state at the output.

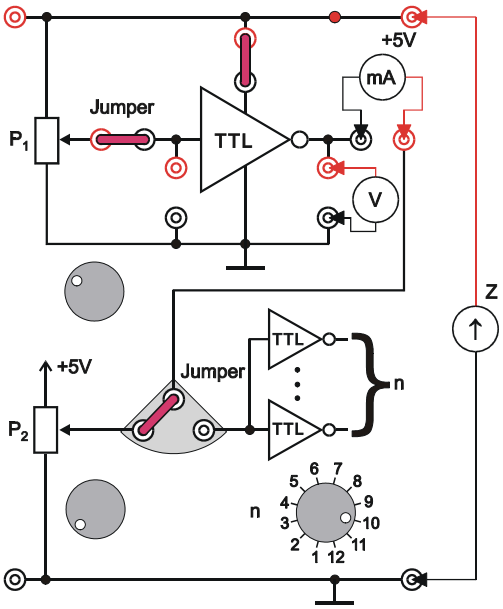

Fig. 6. Setup for measuring output characteristics of a logic gate for the resistive load.

#	the high output state		the low output state	
	$I_{out,H}$ [mA]	$U_{out,H}$ [V]	$I_{out,L}$ [mA]	$U_{out,L}$ [V]
1				
2				

Table 3. Data table for measurements of output characteristic of the logic gate for the resistive load.

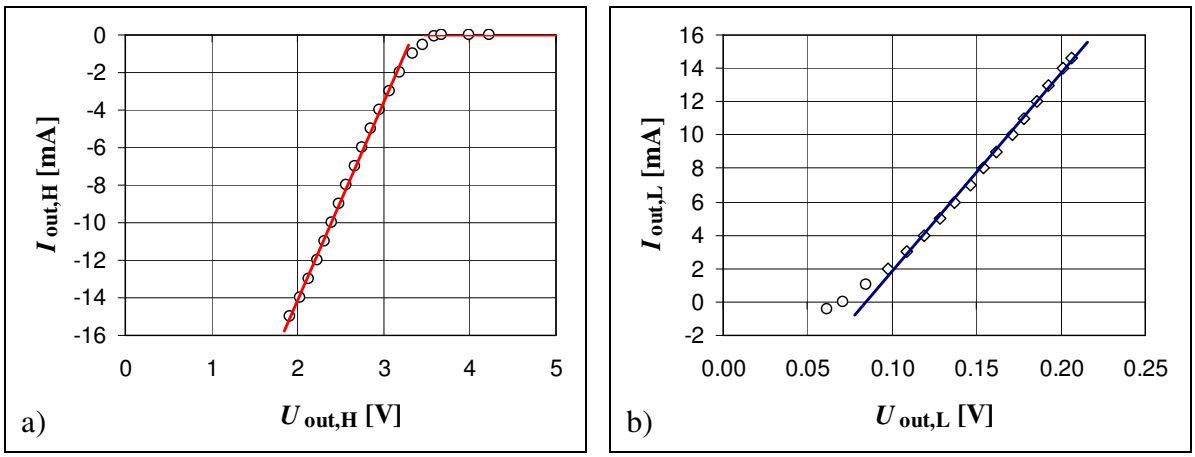

Fig. 7. Typical output characteristics of a TTL logic gate for a resistive load. **a)** the high output state, **b)** the low output state.

Report elaboration

Report has to be composed of:

1. Front page (by using a pattern).
2. Description of experiment purposes.
3. Short introduction (basic definitions, formulas, description of used marks and symbols).
4. Schematic diagrams of tested circuits.
5. List of used instruments and devices (id number, type, setting and range values).
6. Measuring results.
7. Plots, calculations, analysis, interpretation and sub-conclusions related to all required points of "Experimental procedure". In particular:
   7.1. Use the obtained results to plot the input characteristic $I_{in} = f_1(U_{in})$ for the investigated logic gate. Check out if the maximum number (16 mA /$I_{in,max}$) of driven inputs of gates is greater than the catalog value of 10, which takes into account a certain reserve for dispersion of parameters and growth of power dissipation at higher frequencies. $I_{in,max}$ is the maximum input current read from your plot and 16 mA is the maximum permitted output current given in TTL data sheet.
   7.2. Plot the transfer characteristic $U_{out} = f_2(U_{in})$ for the selected number n of the inputs of driven gates. Find in the literature the voltage ranges assumed to represent the low (logical 0), high (logical 1), and unknown logic states at inputs of TTL digital circuits. Check out if the investigated gate correctly transpose the entire voltage range corresponding to the low state at the input to the high state at its output and the entire range for high state at the input to the low state at the output. If so, calculate DC noise immunity (here DC means the long-lasting signals in comparison to the propagation time through a gate). Low level DC noise immunity is defined as the difference $U_{IL} - f_2(U_{IH})$, where U_{IL} is the boundary voltage between the low and unknown logic states and U_{IH} is the boundary between the low and unknown logic states. High level DC noise immunity is given by the formula $f_2(U_{IL}) - U_{IH}$. The smaller of these two differences is DC noise immunity guaranteed for any state. In order to ensure correct transmission of a logic state from the output to the input of next gate, DC noise immunity must be higher than the disruptions in transmission line.
   7.3. Calculate the power dissipated in the gate $P_s = U_s I_s$, where I_s is the measured supply current and $U_s = 5$ V is the supply voltage. Plot the calculated power versus the input voltage $P_s = f_3(U_{in})$.
   7.4. Plot the output characteristics $I_{out} = f_4(U_{out})$ of the investigated gate separately for the low and high output states. Based on your graphs, determine whether there exists a boundary output current, which leads to unknown logic state at the output when the input has any determinated state.
   7.5. Calculate differential output resistances $\partial U_{out} / \partial I_{out}$ of the gate for the low and high output states. In calculations ignore all data that have a bad fit to the linear trends at the plots made in previous step. Do not find differential resistance taking only two selected measuring points! To improve the accuracy of your calculations use the least square method to find the slope of the straight lines at the output characteristics. The differential resistance is reciprocal of the slope.
8. Remarks and final conclusions.

References

[1] J. Kalisz, *Podstawy elektroniki cyfrowej*, WKiŁ, Warszawa 2002.
[2] W. Marciniak, *Przyrządy półprzewodnikowe i układy scalone. Zasady działania, technologia i zastosowania*, WNT, Warszawa 1979.
[3] P. Horowitz, W. Hill, *Sztuka elektroniki*, WKiŁ, Warszawa 2001,
[4] A. Rusek, *Podstawy elektroniki*, część 2, Wydawnictwa Szkolne i Pedagogiczne, Warszawa, 1983.
[5] U. Tietze, Ch. Schenk, *Układy półprzewodnikowe*, WNT, Warszawa 1987.
[6] A. Charoy, *Zakłócenia w urządzeniach elektronicznych*, tom 1, WNT, Warszawa 1999.