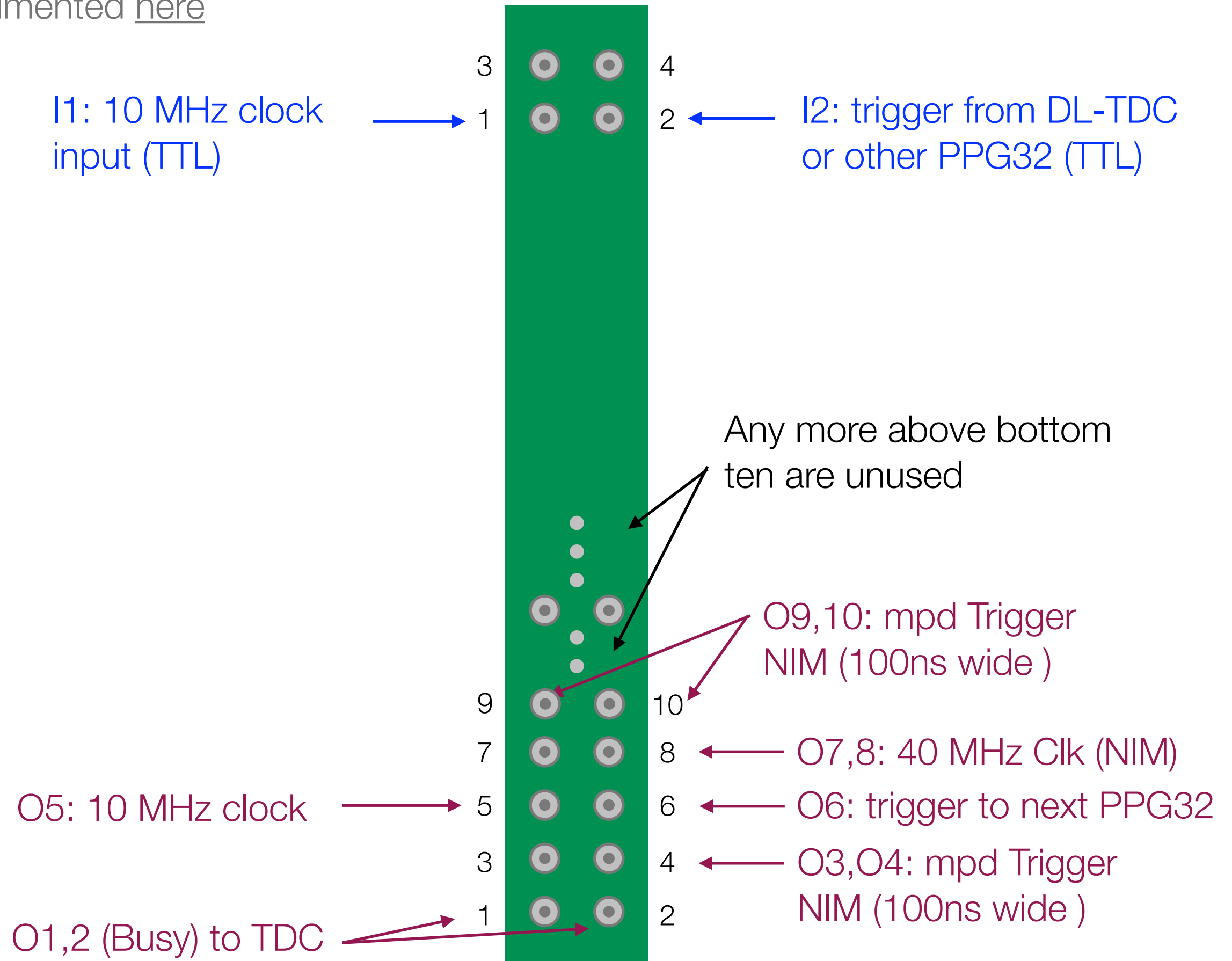


PPG32 I/O v4 Oct 10/25

Documented [here](#)



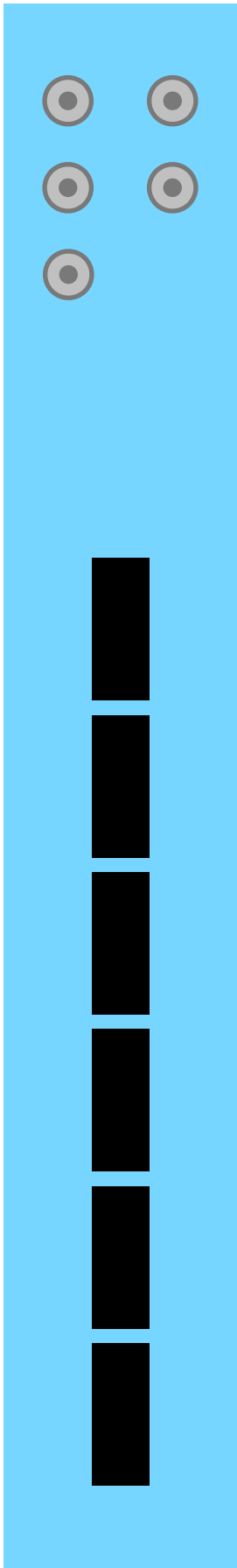
MPD I/O

Trigger in: latch or input
synched with 40 MHz
clock from PPG32

Busy signal?
Not used by us

Clock in: 40 MHz
clock. **MUST BE
LVTTTL SIGNAL** at
risk of breaking MPD

I0
O0
Clk



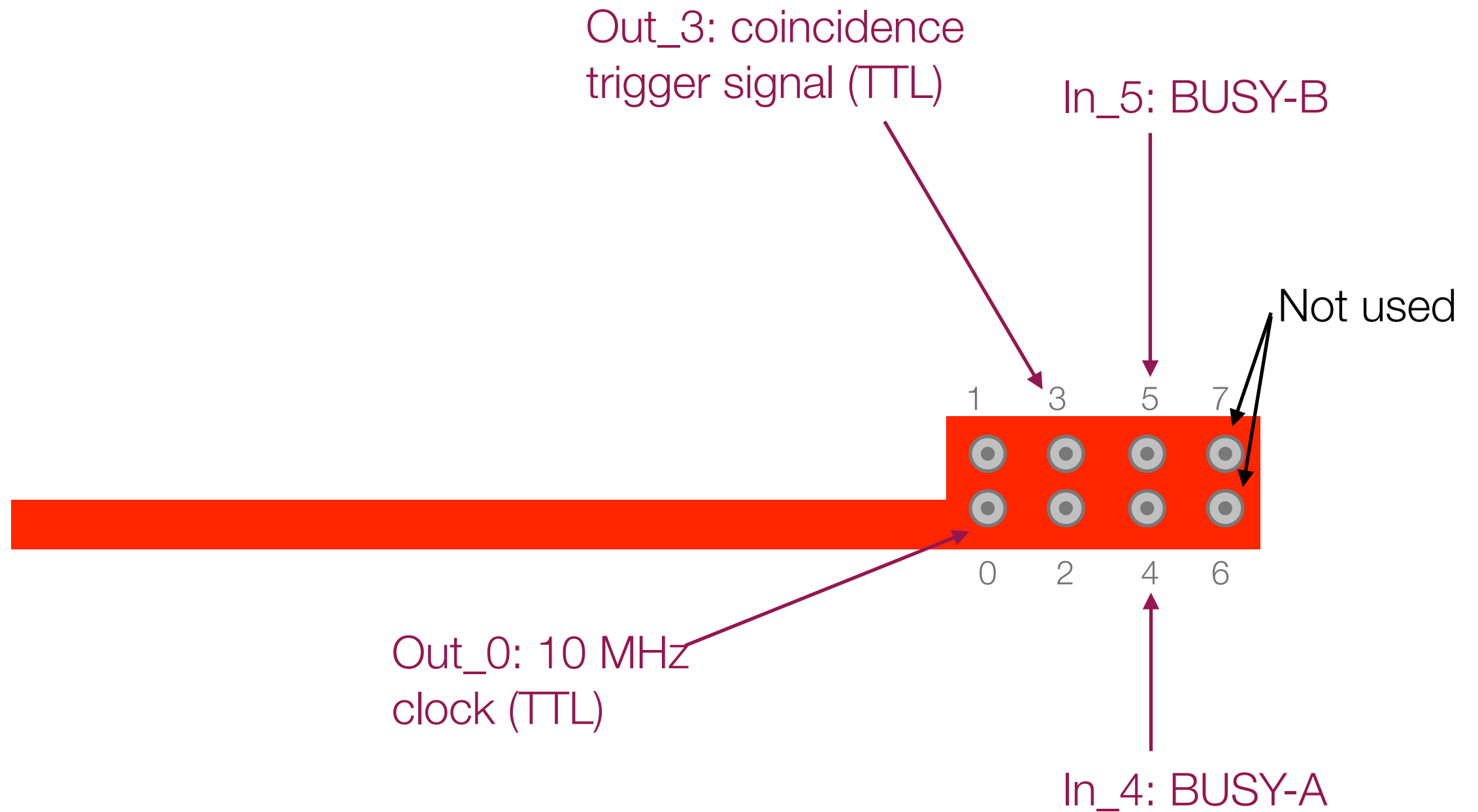
I1
O1

D1
D0
A3
A2
A1
A0

← Sync? Not used by us
← 40 MHz clock out

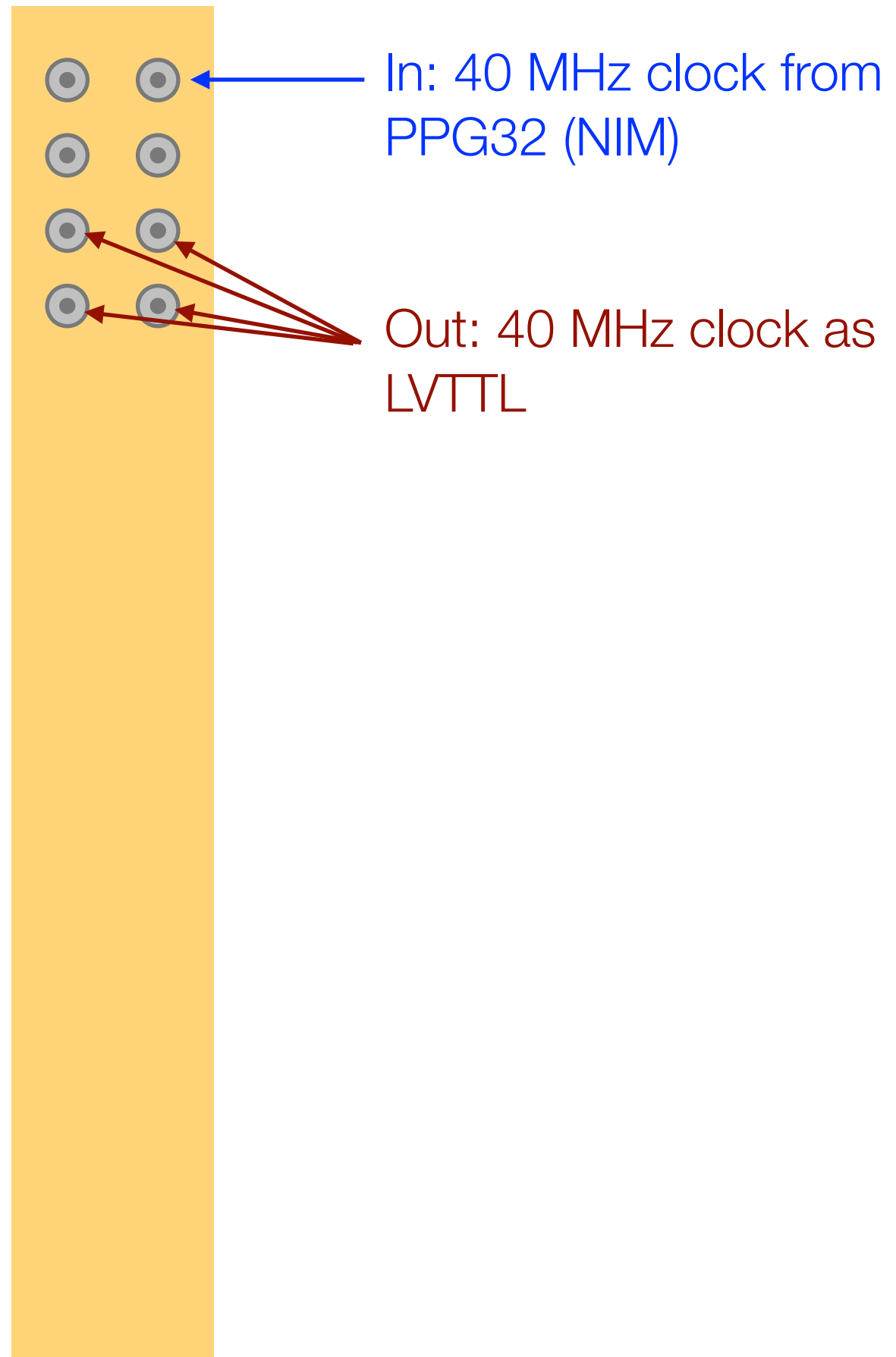
HDMI
cables

Chronobox I/O v4 Oct 10/25

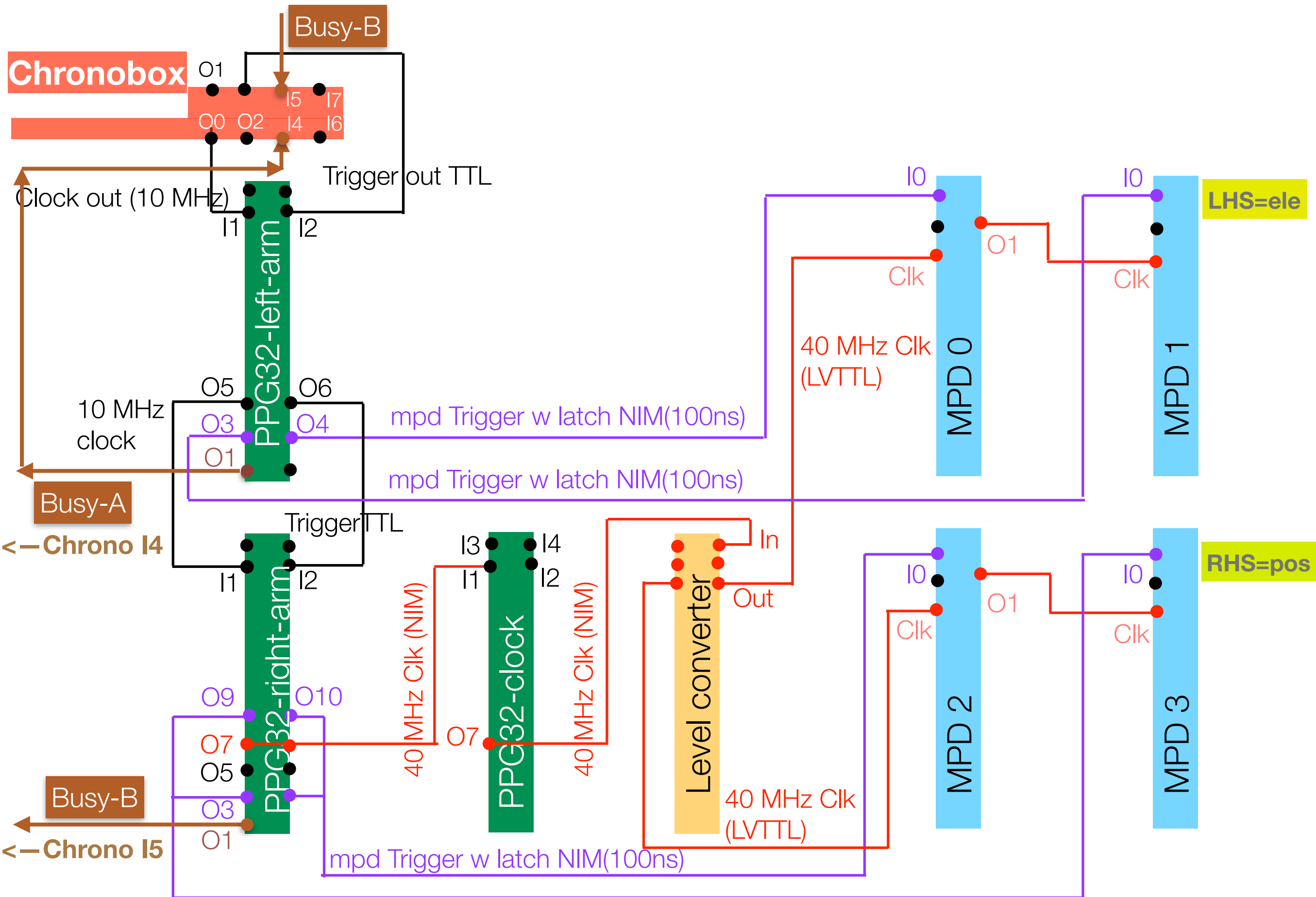


Level converter I/O

Necessary to ensure
PPG32s only receives
LVTTTL clock signals



Cabling diagram v4 Oct 10/25

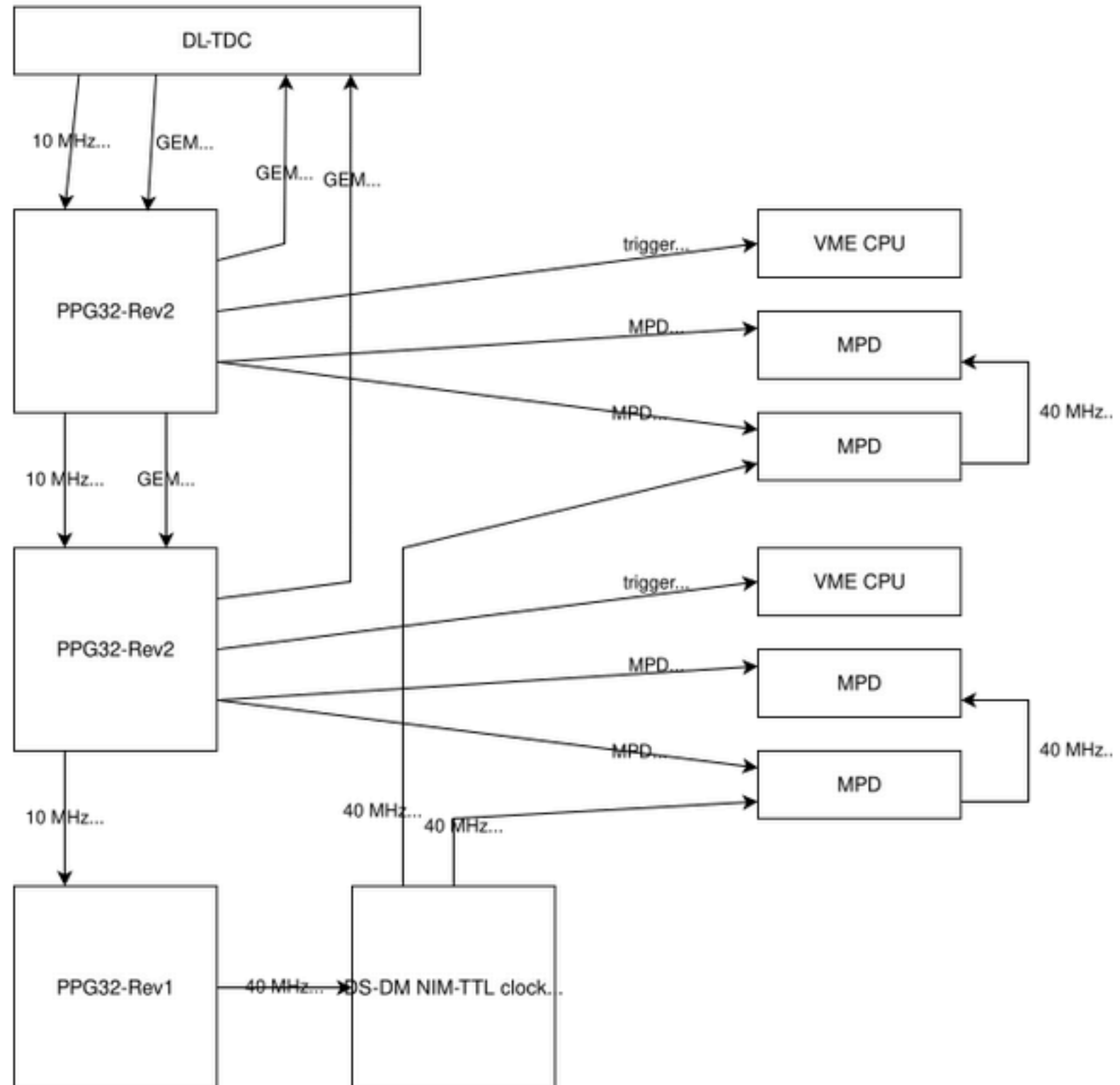


SVG format - trigger and clock distribution

DarkLight clock and trigger distribution, 6-Oct-2025...

Via Konstantin

Documented [here](#)



Note level
converter
handles clock
distribution in
reality