

PPG32 I/O v3 Oct 3/25

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I1: 10 MHz clock
input (TTL)

I2: trigger from DL-TDC
or other PPG32 (TTL)

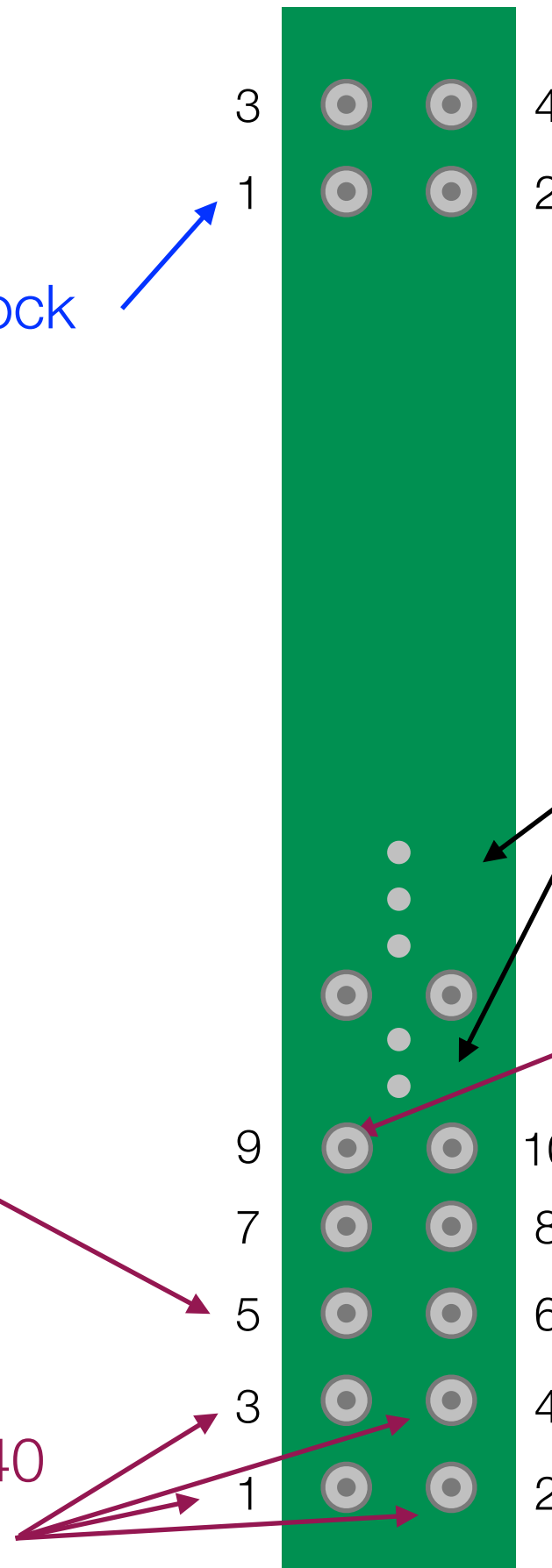
O5: 10 MHz clock
(firmware v0x01250722)
or trigger TTL (firmware v
0x01250603)

O1,2 (Busy),
3,4(Busy=100ns):
(NIM_IN_LATCH[1] or
nimout[1]) synched with 40
MHz clock to trigger

Any more above bottom
ten are unused

O9,10: 40 MHz clock pulse
NIM (100ns wide)

O6: trigger TTL for
distribution to next
PPG32 (both firmwares)



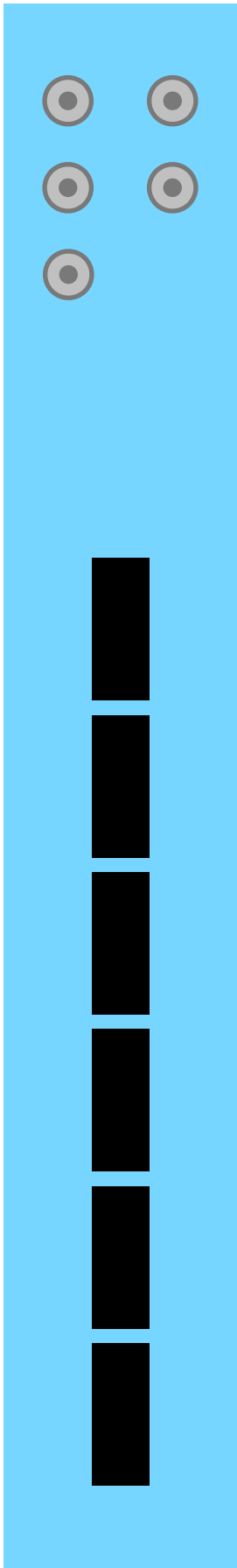
MPD I/O

Trigger in: latch or input
synched with 40 MHz
clock from PPG32

Busy signal?
Not used by us

Clock in: 40 MHz
clock. **MUST BE
LVTTTL SIGNAL** at
risk of breaking MPD

I0
O0
Clk



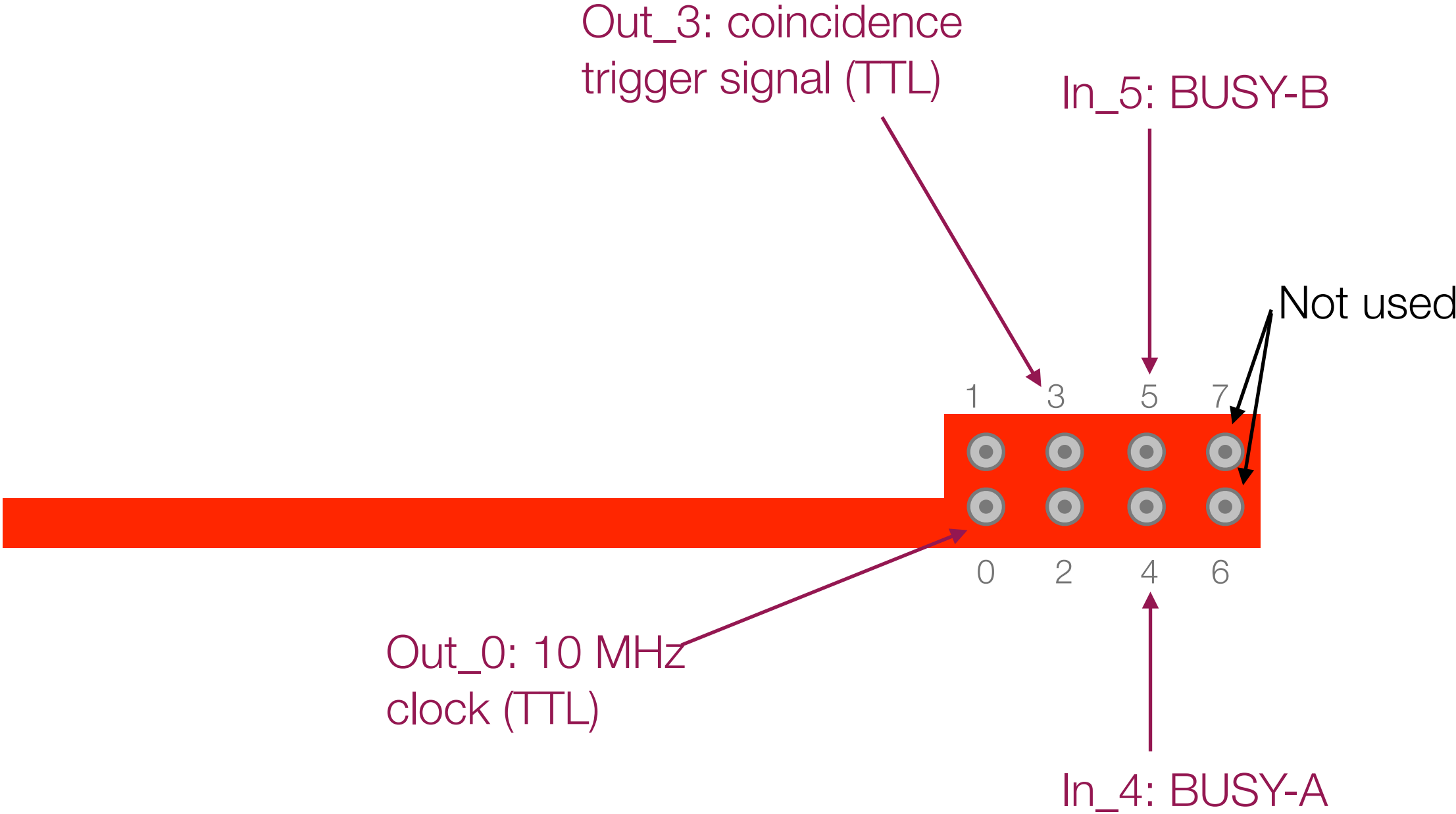
I1
O1

Sync? Not used by us
40 MHz clock out

D1
D0
A3
A2
A1
A0

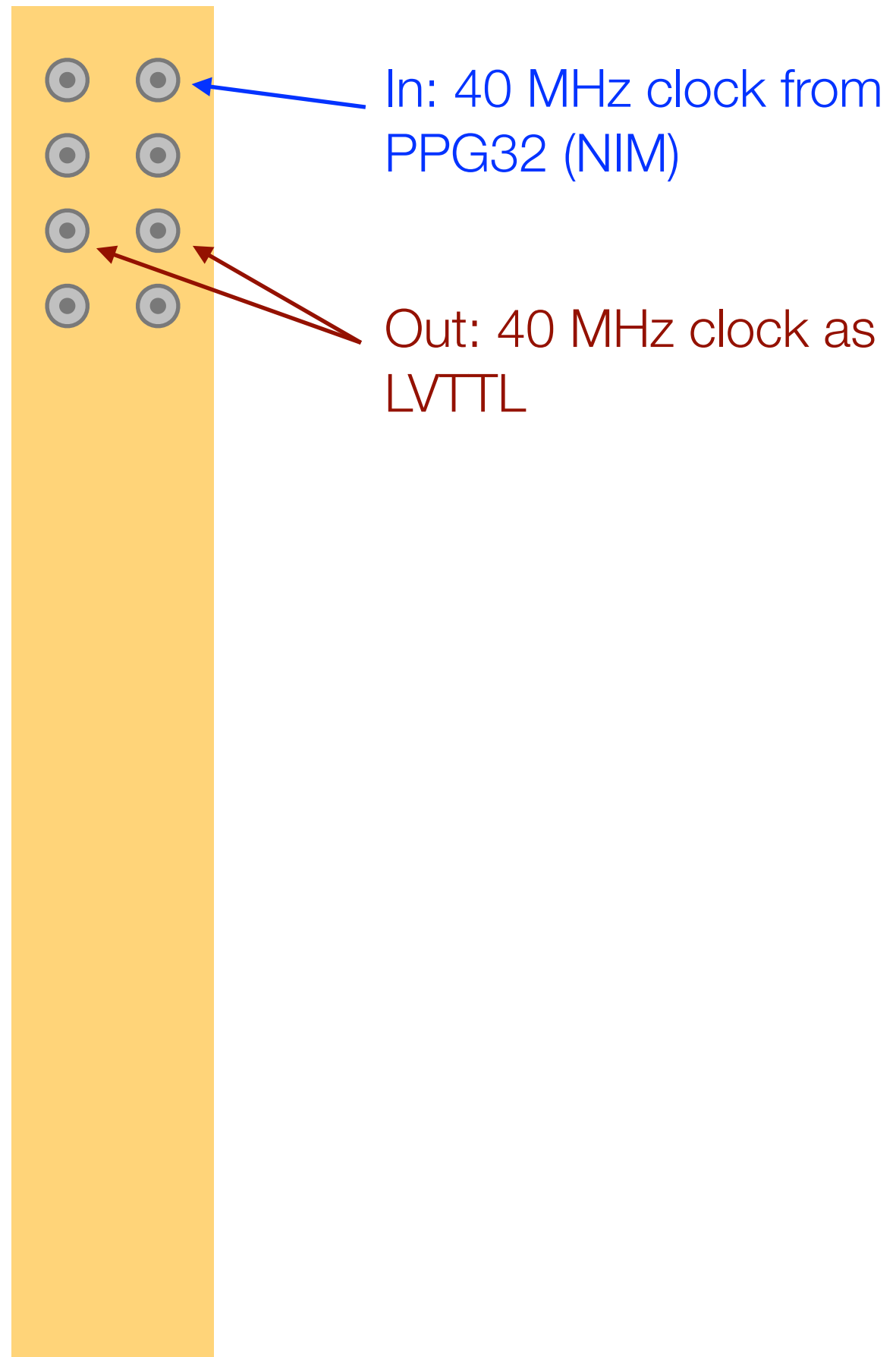
HDMI
cables

Chronobox I/O v3 Oct 3/25

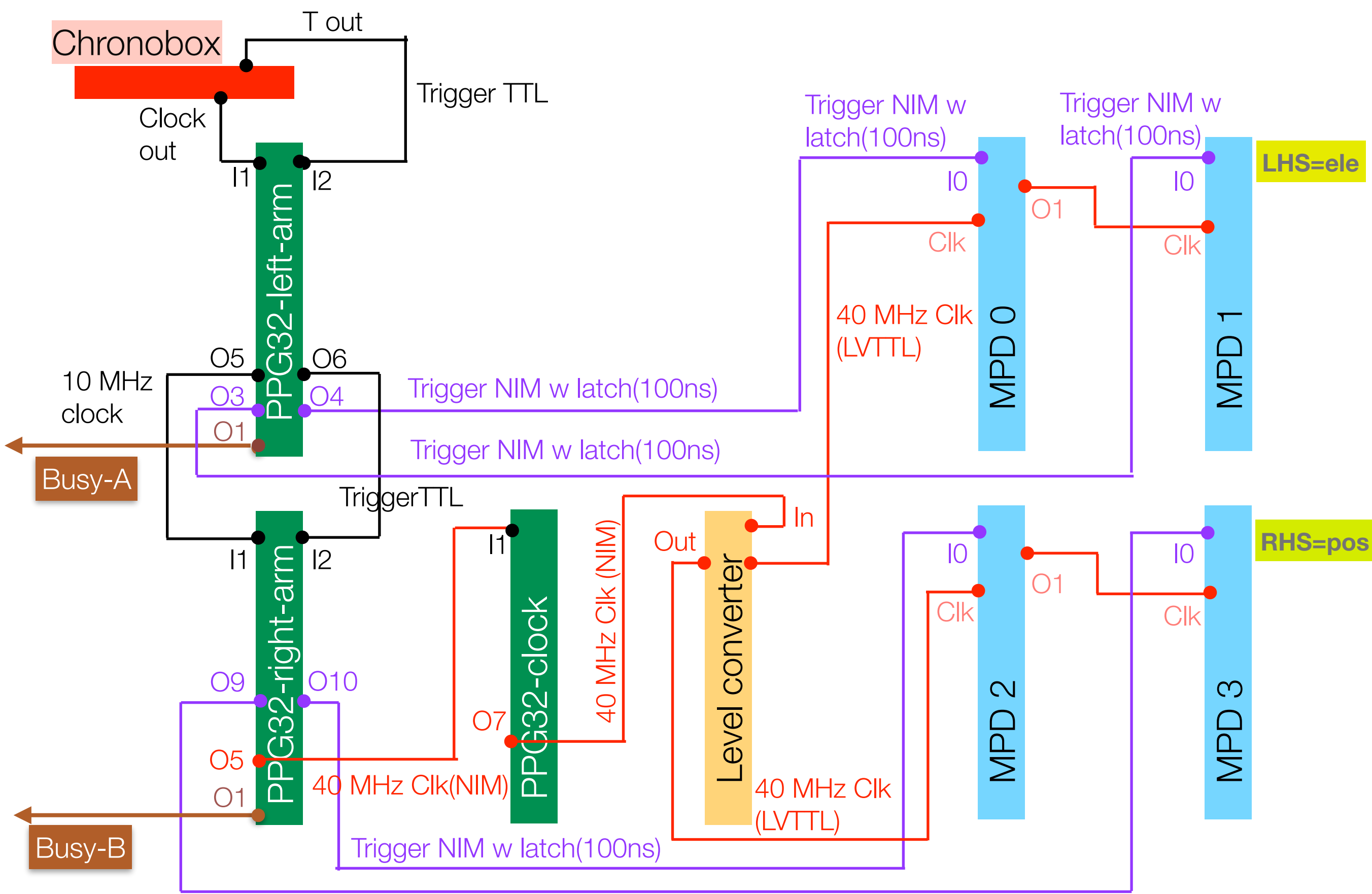


Level converter I/O

Necessary to ensure
PPG32s only ever receive
LVTTTL clock signals

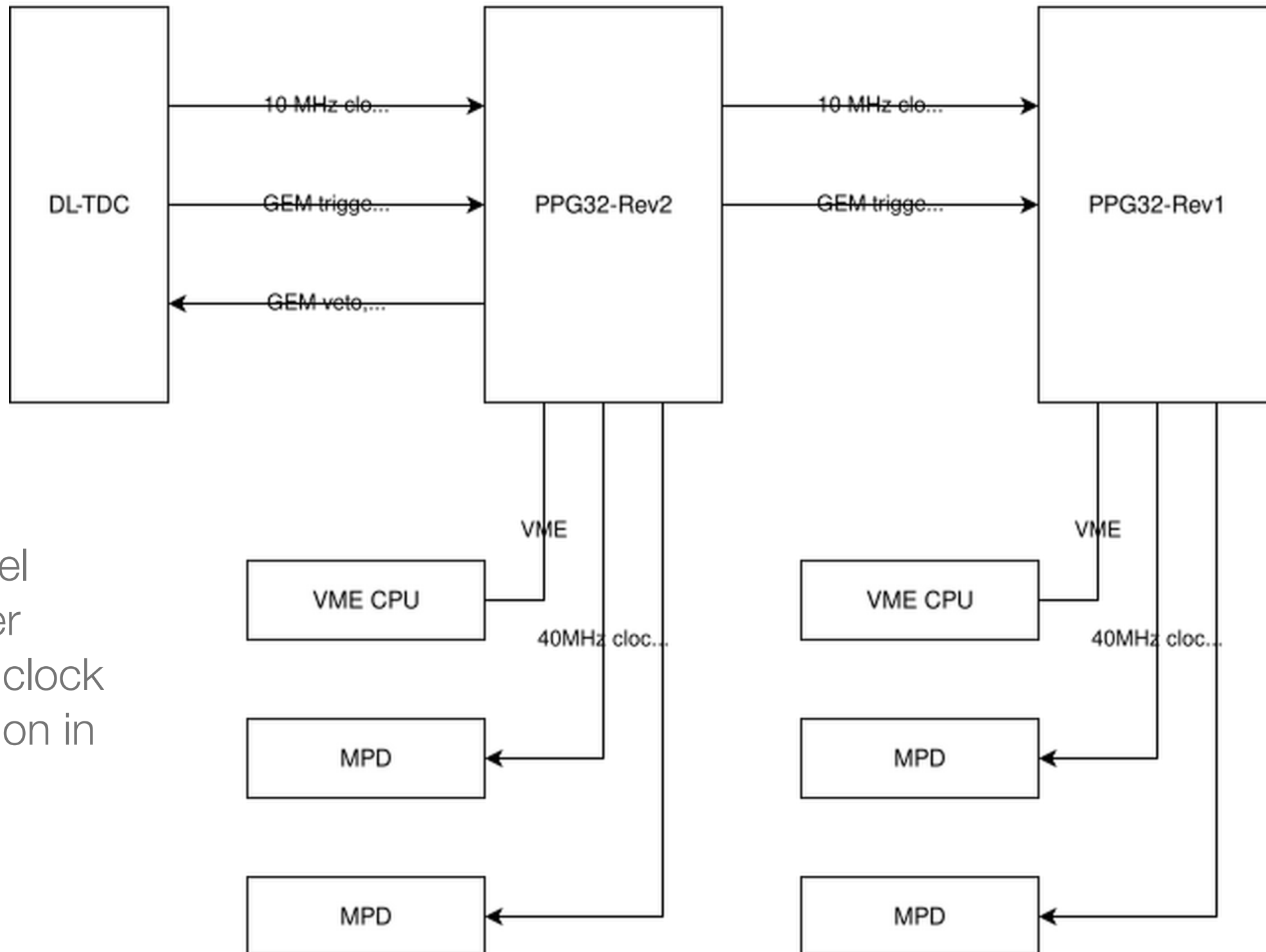


Cabling diagram v3 Oct 3/25



Via Konstantin

Documented [here](#)



Note level
converter
handles clock
distribution in
reality