PPG32 I/O v3 Oct 3/25

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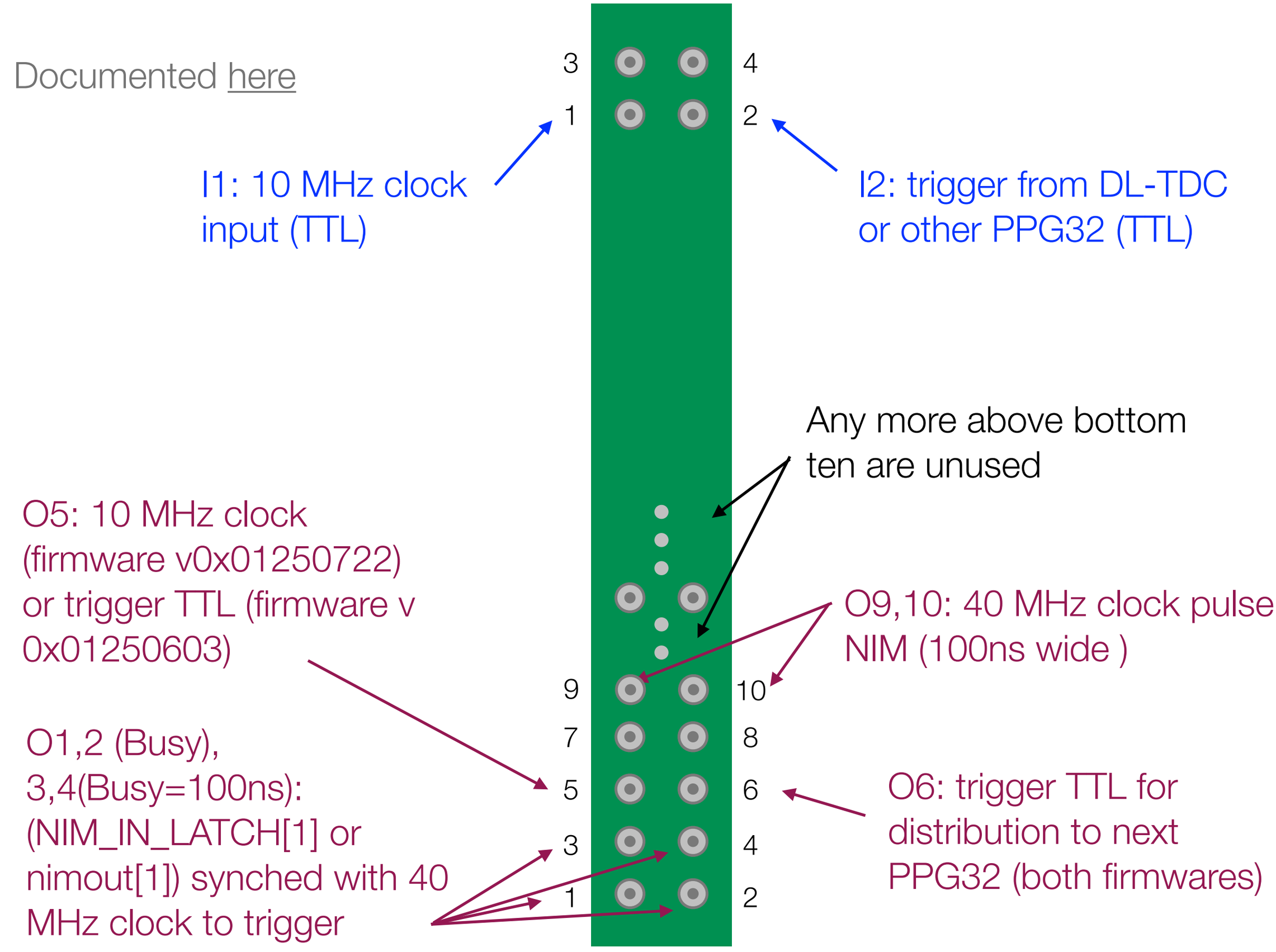
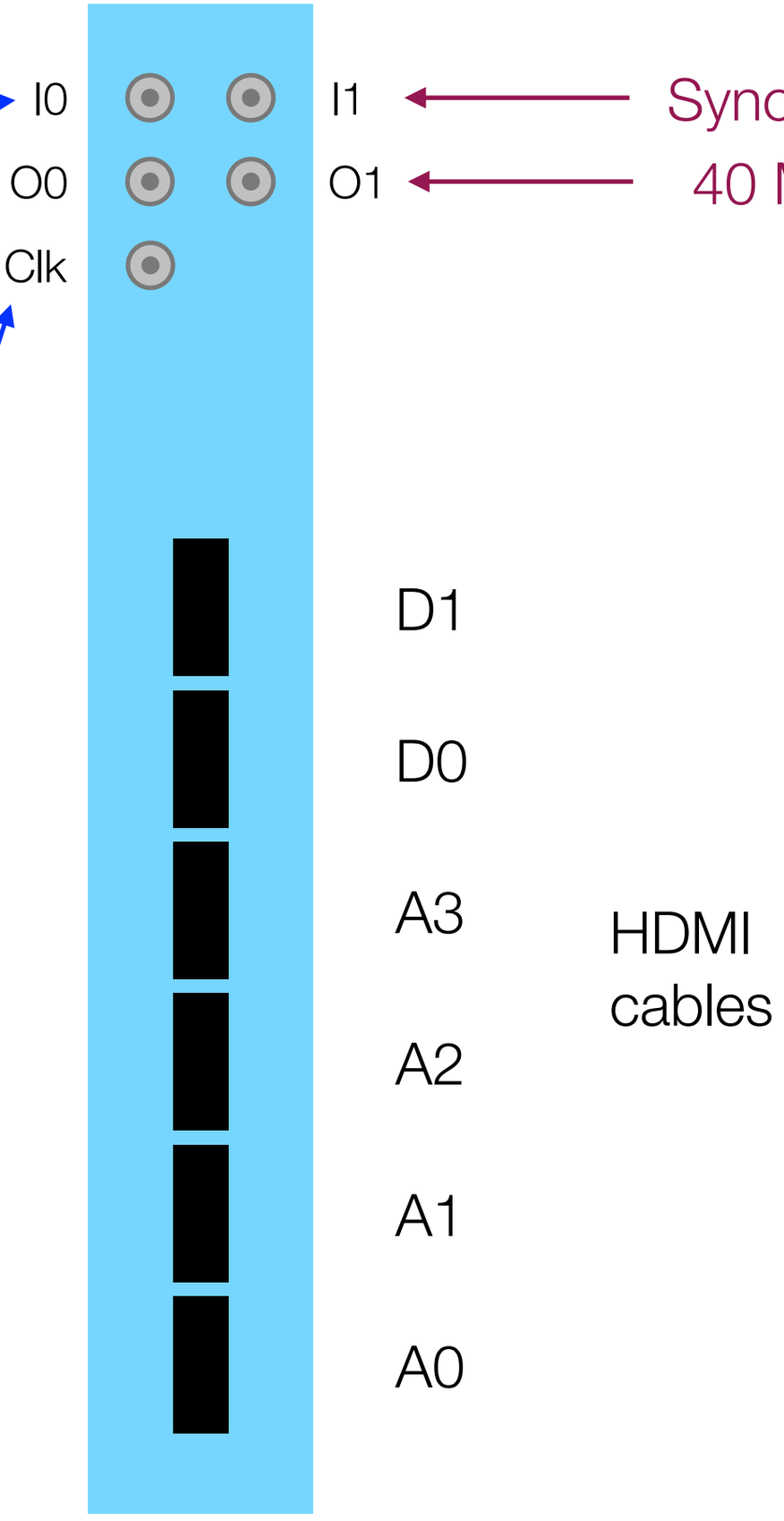


MPD I/O

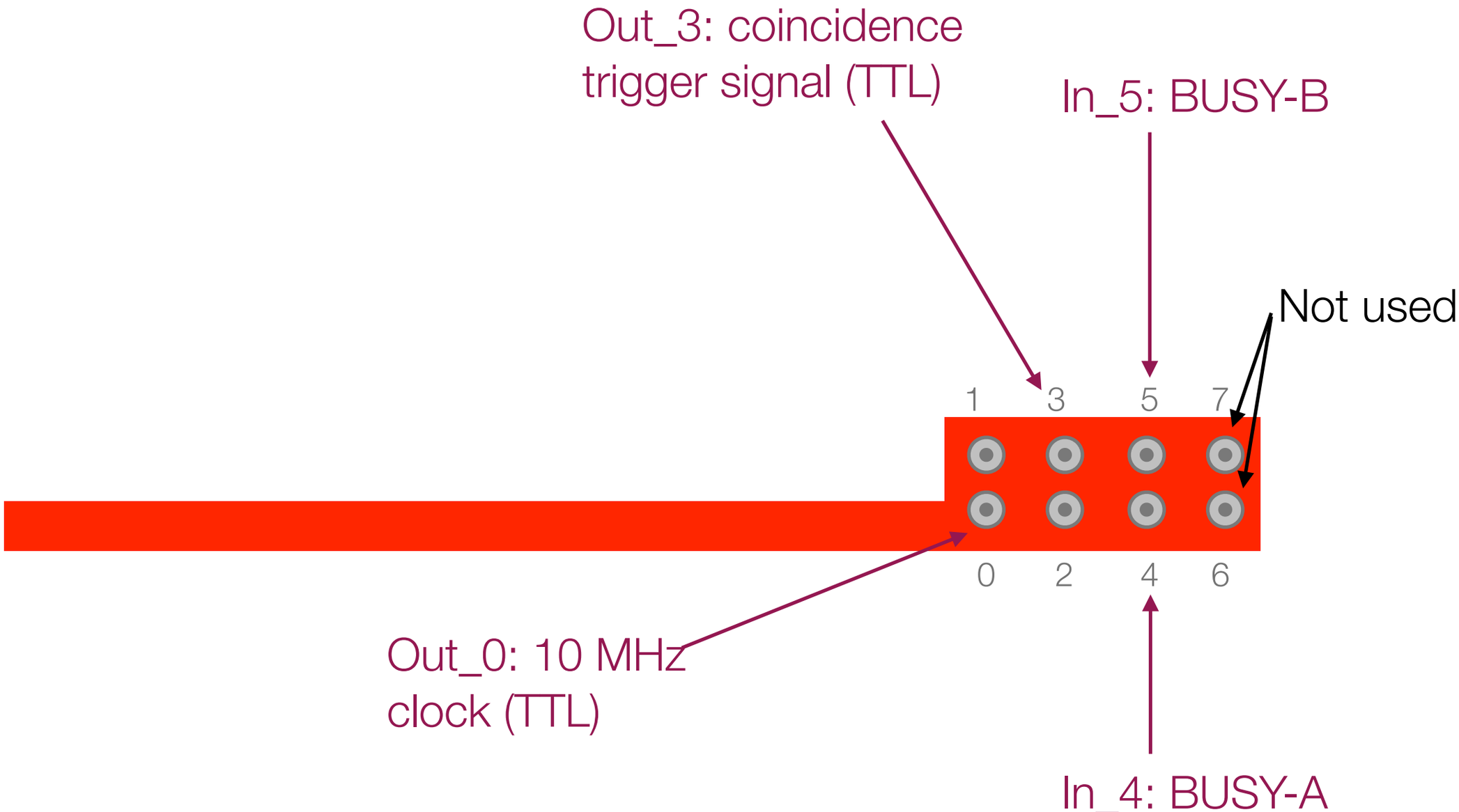
Trigger in: latch or input synched with 40 MHz clock from PPG32

Busy signal? Not used by us

Clock in: 40 MHz clock. **MUST BE LVTTL SIGNAL** at risk of breaking MPD

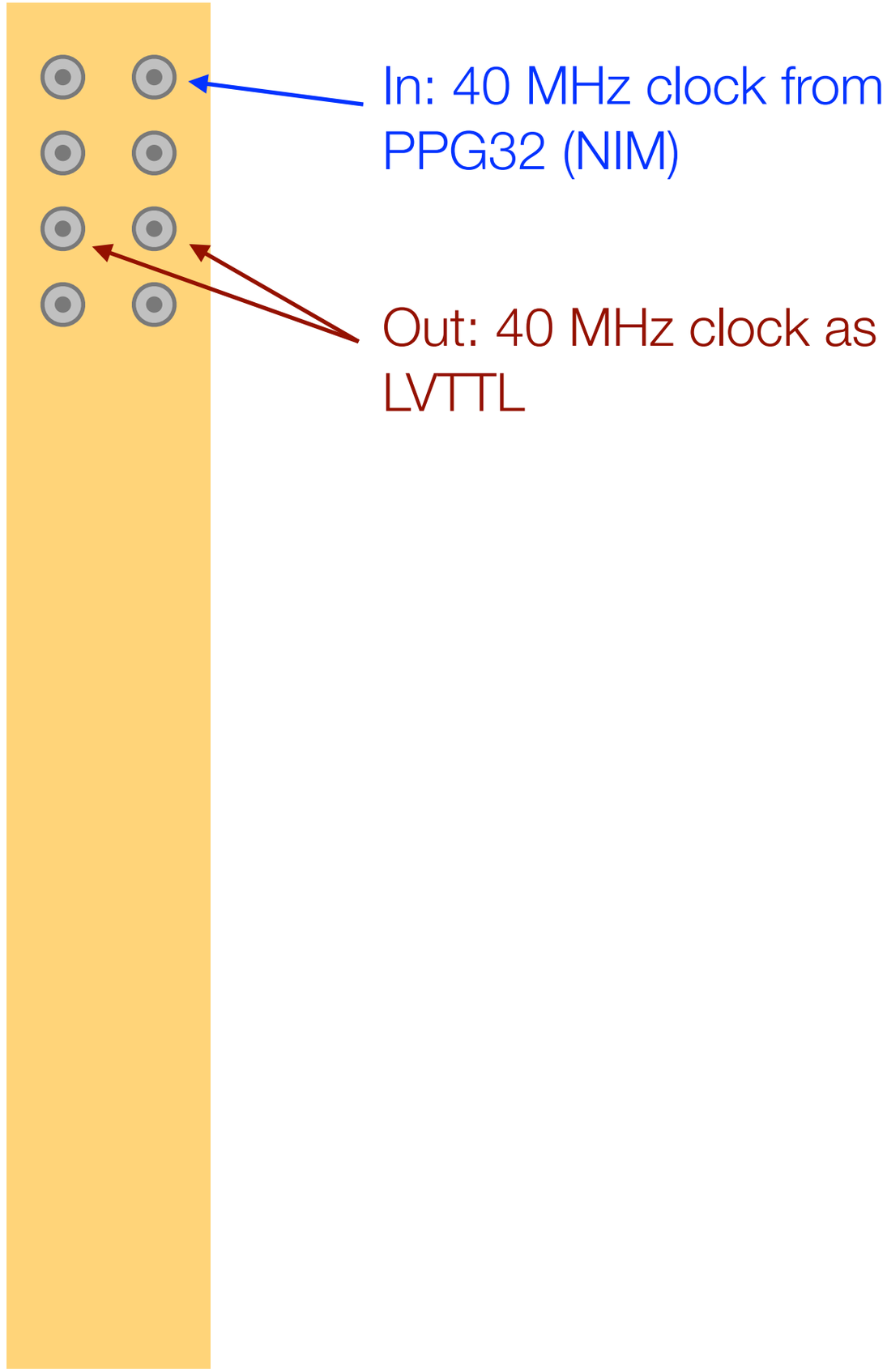


Chronobox I/O v3 Oct 3/25

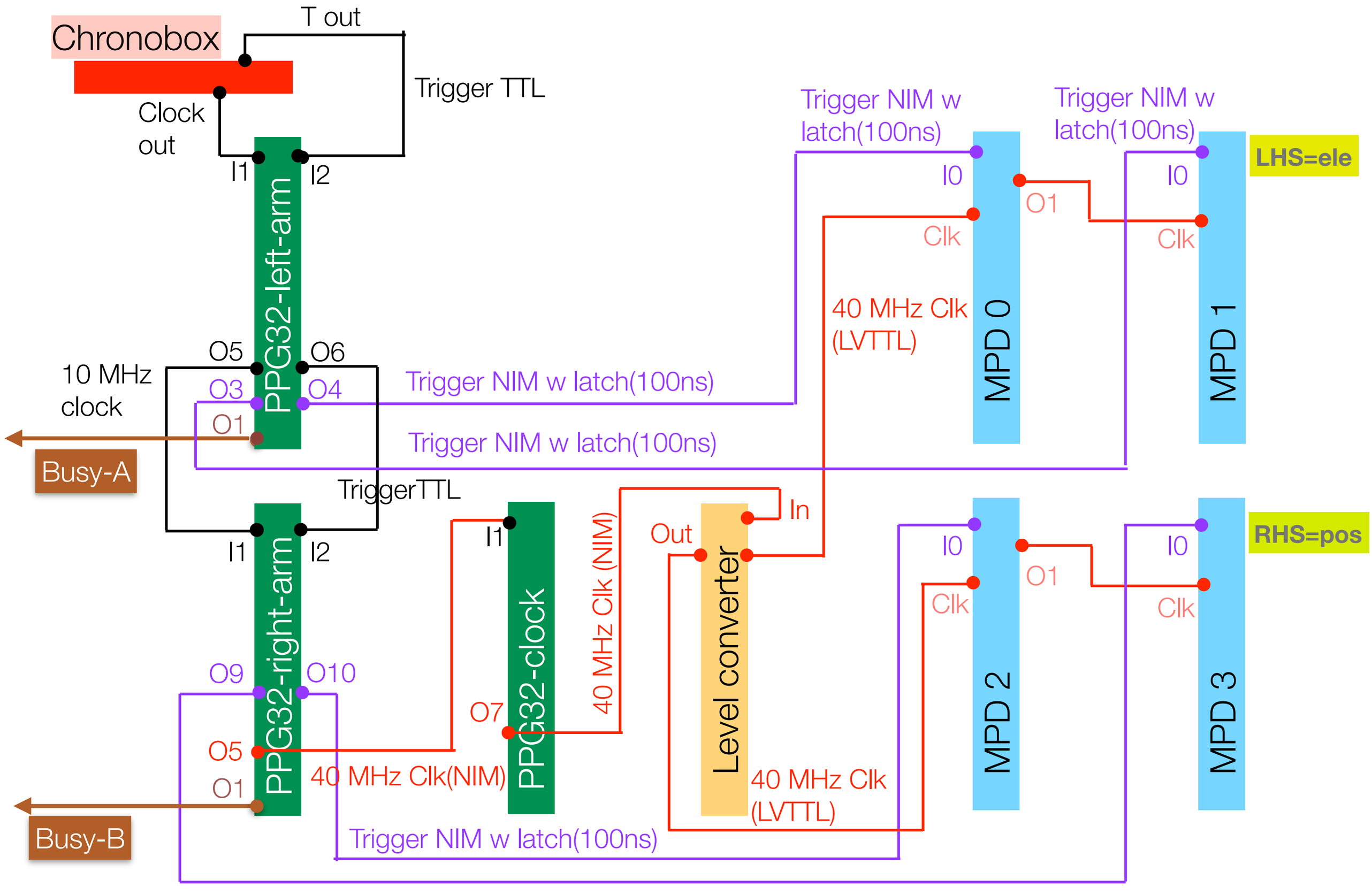


Level converter I/O

Necessary to ensure PPG32s only ever receive LVTTL clock signals



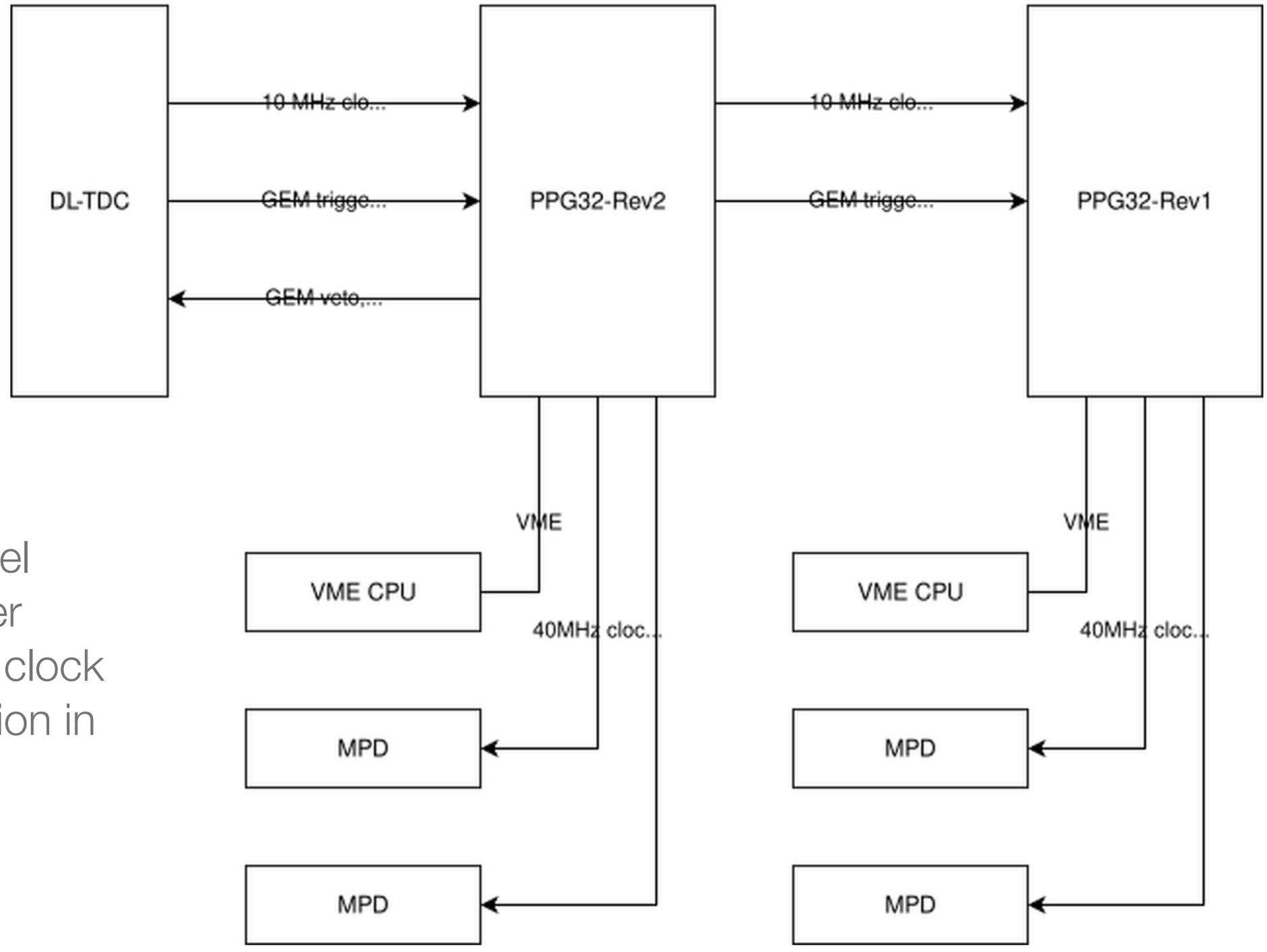
Cabling diagram v3 Oct 3/25



DarkLight clock and trigger distribution, 21-July-20...

Via Konstantin

Documented here



Note level converter handles clock distribution in reality