Week 2 Intellectual Property Protection

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Overview

As a hardware designer or a company, you want to protect your design intellectual property (IP) from being misused (by users, competitors, silicon foundry, etc). We will cover how you can build such protection during the design process which can be used as an evidence to support law enforcement protection. You are expected to understand the basic digital logic design knowledge covered in week 1. We will use several NP-hard problems as examples to illustrate the concepts of IP protection. These problems (graph vertex coloring problem and graph partitioning problem) will be introduced in the lecture and you do not need to know the concept of NP-complete.

Learning Objectives

After the completion of this week, you will be able to:
- learn self-protection techniques for design IPs: watermarking, fingerprinting, metering
- assess the trade-off among security, cost and performance

Video Lectures

- Introduction to IP Protection (11'26") PDF
- Watermarking Basics (8'23") PDF
- Watermarking Examples (12'31") PDF
- Good Watermarks (15'13") PDF
- Fingerprinting (17'24") PDF
- Hardware Metering (13'24") PDF

Readings

- G. Qu and M. Potkonjak, *Intellectual Property Protection in VLSI Designs: Theory and Practice*, Kluwer Academic Publishers, ISBN 1-4020-7320-8, January 2003.
- G. Qu and LYuan, "Secure Hardware IPs by Digital Watermark", in *Introduction to Hardware Security and Trust*, pp. 123-142, Springer, ISBN 978-1-4419-8079-3, 2012.
- Y. Alkabani and F. Koushanfar. *Active Hardware Metering for Intellectual Property Protection and Security.* USENIX Security, 2007
- F. Koushanfar, "Hardware Metering: A Survey", in *Introduction to Hardware Security and Trust*, pp. 103-122, Springer, ISBN 978-1-4419-8079-3, 2012.

Discussions

Click here to view the Week 2 Discussion Questions.

Quizzes

Click here to take the quiz.

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