An energy efficient multipliers using reversible gates

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Abstract.The known advantages of Reversible gates namely reduced power consumption and low latency found useful in Quantum computing. Its low power consumption and quicker operation makes them to be useful in applications Microprocessors, DSP processors and Quantum computers. Numerous reversible gates have been found in literature. This article focuses the implementation of 4 bit multiplier with the help of reversible logic gates. Array multiplier is chosen for our choice. Toffoli gate is chosen for partial product generation. The accumulation of partial products is carried using three topologies. The first topology uses reversible carry look ahead adder. The second topology uses parity preserving reversible carry look ahead adders. The third topology uses modified parity preserving reversible carry look ahead adders. The energy efficient multiplier's topology proposed in this article implementation are done using Cadence 180nm technology. Performance evaluation reveals that the proposed reversible gate based multiplier results lesser power consumption and also a quicker one. It results that the proposed topology consumes 52.03% lesser power, topology 2 consumes 63.02% lesser power and topology 3 consumes 63.79% lesser power when compared with an existing reversible multiplier design. As the power consumption is the dominating quantity in VLSI design, the proposed topologies of multiplier design results better performance. The achieved area occupation of the proposed topology 1, topology and topology 3 are also 58.44%, 61.90% and 69.26% lesser respectively when compared with that existing reversible multiplier. Its quicker operation is also achieved by the reduction in propagation delay. Hence the proposed multiplier topologies named as an energy efficient multipliers.

1. Introduction

Many of the Microprocessors, Digital Signal Processors and DSP applications need the multiplication operation. Many investigations in VLSI implementation were done for a lesser power dissipation and quicker operation without sacrificing its cell area. The frequently used arithmetic operations such as addition and multiplication plays major role in execution time of any Microprocessor or Digital Signal Processor. It is shown that 3/4th of the Instruction set in Microprocessor perform binary addition and multiplication [1]. Hence for this reason, designing a multiplier with increasing speed is required for signal processing applications. The second major criteria of multiplier is lesser power consumption. Employment of minimum of components in a multiplier design reduces its dynamic power consumption as this type of power consumption is more in total power consumption of any digital logic circuit. The major concern of an efficient multiplier design is its quicker operation and low power consumption. Researchers concentrated on this aspect and designed various architectures of multiplier. One such type of multiplier architecture is array multiplier. Due to its regular structure, they are used for many applications. Its operation done with partial product calculations and its accumulation by an array using binary adders. Its structure can directly mapped into hardware [2]. Its major drawback is its higher area consumption. The letter [3] proposes carry save array multiplier where the accumulation of partial products done using carry save

adder. A Wallace tree multiplier [4] introduces quicker operation compared to array multiplier for larger input. It is a tree like structure where tree multiplier is used for the reduction of number of cells and also critical path delay. But it suffers from larger area and irregular structure makes the design with higher computational complexity. Similar to the Wallace tree multiplier, Dadda multiplier has also a tree like structure. The difference between those two multipliers is that Dadda multiplier has fewer computations when compared with Wallace tree multiplier thereby making the multiplier design faster. But they also suffered from larger area consumption. Another structure of multiplier called Booth Wallace Tree Multipliers that generates the partial products using Booth algorithm and addition is similar to the Wallace tree operation [5]. This type of multiplier suffers from nonlinear delay when bit size increased though it consumes lesser area compared to other multipliers.

Reversible logic gates in VLSI design makes the design implementation lesser power consumption and quicker operation. Concept of reversible logic contains unique pattern of input and output. And each of its input derived from its output thus making back computation in reversible circuits. This substantially reduces the loss of information [6]. Another advantage of reversible gate is it has no fan out. Hence power consumption is further decreased. In future reversible logic gates will replace conventional logic gates due to these advantages mentioned above. Unlike regular logic gates, its number of input and output are equal. By this reversible computation, the latency and power dissipation has been reduced literally. This back computation highly needed for quantum computing and nanotechnology [7]. Parity preserving is a technique which finds a proper solution over improper occurrences. It would be useful in achieving error free circuits in quantum computing [8].

This letter contains the design of energy efficient 4 bit multiplier circuit using reversible gates. The toffoli gate is chosen for partial product calculations. The accumulation of partial products are done using carry look ahead adder. The formulation of this paper is as mentioned: section 2 discusses the related work on reversible gates based digital circuits. Section 3 gives the overview of reversible logic gate fundamentals and description about toffoli gate. The proposed optimized multiplier design is described in section 4 and section 5 discusses the simulation results of the proposed work. Finally, section 6 winds up the paper with conclusion and future scope.

2. Related Work

Numerous multiplier implementations have been done by means of reversible logic gates. Array multiplier and Wallace Tree multiplier implementations with the help of reversible logic gates have been identified in [3,4,10,11]. It is shown that array multiplier absorbs lesser power than tree multiplier. Also tree multiplier requires additional hardware. But array multiplier has lesser complexity because of its regular structure. Henceforth, array multiplier based reversible gates is the best choice for low power consumption, quicker speed, regular cell layout and relatively good performance [13-17].

The above mentioned works use more than two reversible logic gates for multiplier implementation. The letter [18] proposed only HNG gates based multiplier design. This article proposed an energy efficient multiplier circuit using toffoli reversible logic gates for partial product generation and its accumulation is done using reversible carry look ahead adder with three topologies. The proposed multiplier design results in reduced complexity and consumes lesser power when compared with existing reversible multiplier circuits.

3. Fundamentals Of Reversible Logic Gates

As mentioned earlier, reversible logic gates have equal number input and output. Any input combination can be derived from one of the output combination. Because of this character, there will be no information loss. This makes reversible logic gates more advantageous than conventional logic gates. Any basic gate operation can be done by the inclusion of extra wires at the input and output side [9]. But it has the following two conditions such as unavailability of feedback and unavailability of Fan-out (Fan-out is ‘1’).

A reversible gate of structure n*n has n number of input and n number of output. Many reversible logic gates were found over past years. Figure 1 shows the toffoli reversible gate. It has three input and three output. The output expression are mentioned in Figure.1. Many multiplier

designs were found using more than one reversible logic gates. This may increase the quantum cost of the system. To eradicate this problem, we focused Toffoli gate alone for the partial product generation. For the design of carry look ahead adder of this proposed work includes the following reversible logic gates such as Feynman gate, Fredkin gate, TSG gate, PGA gate, F2G gate, NFT gate and R2 gate. The logic expressions of those gates are explained in this brief.

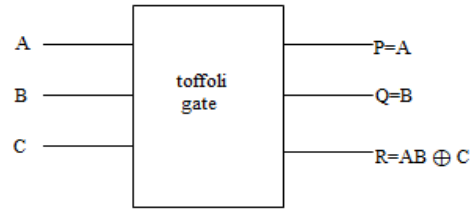

Figure 1: Toffoli gate

Another reversible gate called Feynman gate is shown in Figure.2. It is an 2*2 reversible gate and its expressions are shown in the Figure.2. This reversible gate can be used as a copying gate.

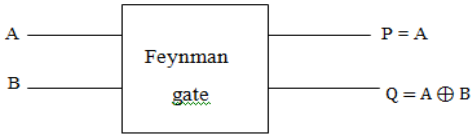

Figure 2: Feynman gate

The Fredkin gate shown in Figure.3 is also a reversible logic gate which is a 3*3 gate. Its output expressions are given in the Figure.3

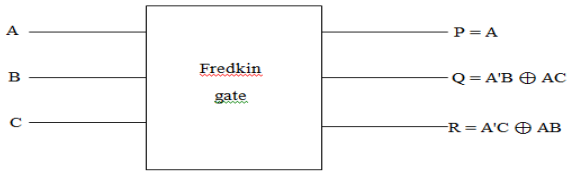

Figure 3: Fredkin gate

A 4*4 reversible logic gate is TSG gate which is shown in Figure.4. It alone works as a full adder which clear from the output expressions given in Figure.4.

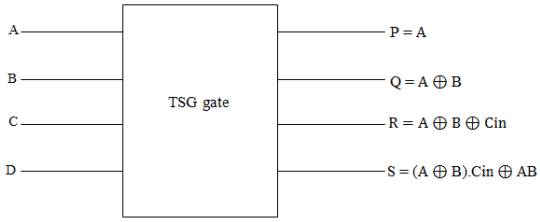

Figure 4: TSG gate

The Propagate Generate Architecture gate which is abbreviated as PGA gate is capable of generating sum (S_i), Carry propagate (P_i), Carry generate (G_i) expressions of a carry look ahead adder and its diagram is shown in Figure.5

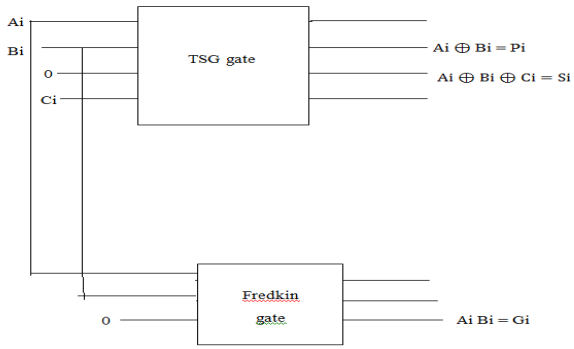

Figure 5: PGA Gate

The Feynman Double Gate (F2G) is also a reversible logic gate which is shown in Figure.6. If any of its three input is made '0', then the copy of its one input would be the output.

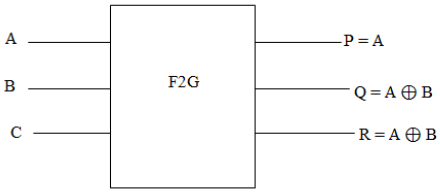

Figure 6: F2G Gate

New Fault Tolerant Gate is shown in Figure.7. This reversible logic gate is capable of doing all logic gate functionalities such as AND, OR, NAND, NOR, EXOR and EXNOR.

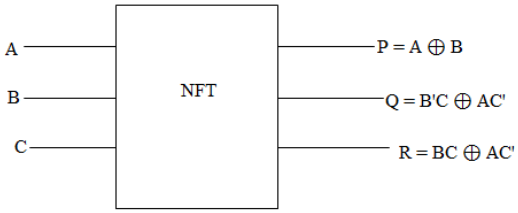

Figure 7: NFT Gate

A new type of 4*4 reversible logic gate (R2 gate) and its output expressions are shown in Figure.8. This gate is very much useful in parity calculations as it does only EXOR operation of any four input bits.

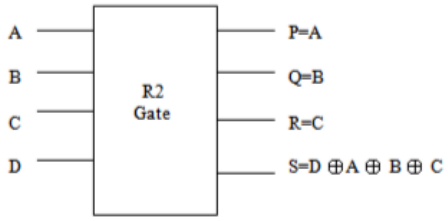

Figure 8: R2 Gate

4. Proposed Multiplier Design

The array multiplier proposed in this work designed using Toffoli reversible gate. The partial products calculated using Toffoli gate and the accumulation of partial products done with the help of carry look ahead adder. The partial product accumulation using carry look ahead adder is actually done using three topologies in this work. They are as follows:

Topology – 1: 4-bit multiplier in reversible carry-look ahead adder circuit.
Topology – 2: 4-bit multiplier in parity preserving reversible carry-look ahead adder
Topology – 3: 4-bit multiplier in modified parity preserving reversible carry-look ahead adder

4.1. Topology – 1: 4-bit multiplier in reversible carry-look ahead adder circuit

The operation of array multiplier starts with the calculation of partial products of the individual bits of two operands. For 4 bit multiplication, totally 16 partial product terms were obtained. The partial products in each stage is shifted and added to the next stage partial products. Thus the final product of multiplication process is obtained. The accumulation of each partial product stage can be done using any of the traditional adder topology. In our work, we used Toffoli reversible gate for the calculation of partial products and we used reversible carry look ahead adder for the accumulation of partial products. Figure.9 shows the proposed 4 bit multiplier design where the partial products are developed using toffoli reversible gate and the accumulation is done using reversible carry look ahead adder. Then the design of 4-bit carry-look ahead adder includes the reversible logic gates such as fredkin gate, feynman gate, PGA gate, TSG gate, R2 gate. The detailed description of these reversible gates are explained in section 3. Figure.9 depicts the circuit diagram of the 4 bit reversible multiplier using toffoli gate and carry look ahead adder. The proposed topologies proposed in this work differs only by carry look adder block. In topology 1, the carry look ahead adder is designed using reversible gates as shown Figure.10. The carry propagate, carry generate and sum expressions of carry look ahead adder will be as follows:

Carry propagate $P_j = A_j$ XOR B_j, where A_j, B_j are input of each stage &C_j is input carry
Carry generate $G_j = A_j$ AND B_j
Sum at each stage $S_j = P_j$ XOR C_j
Carry expression $C_{j+1} = G_j + P_jC_j$

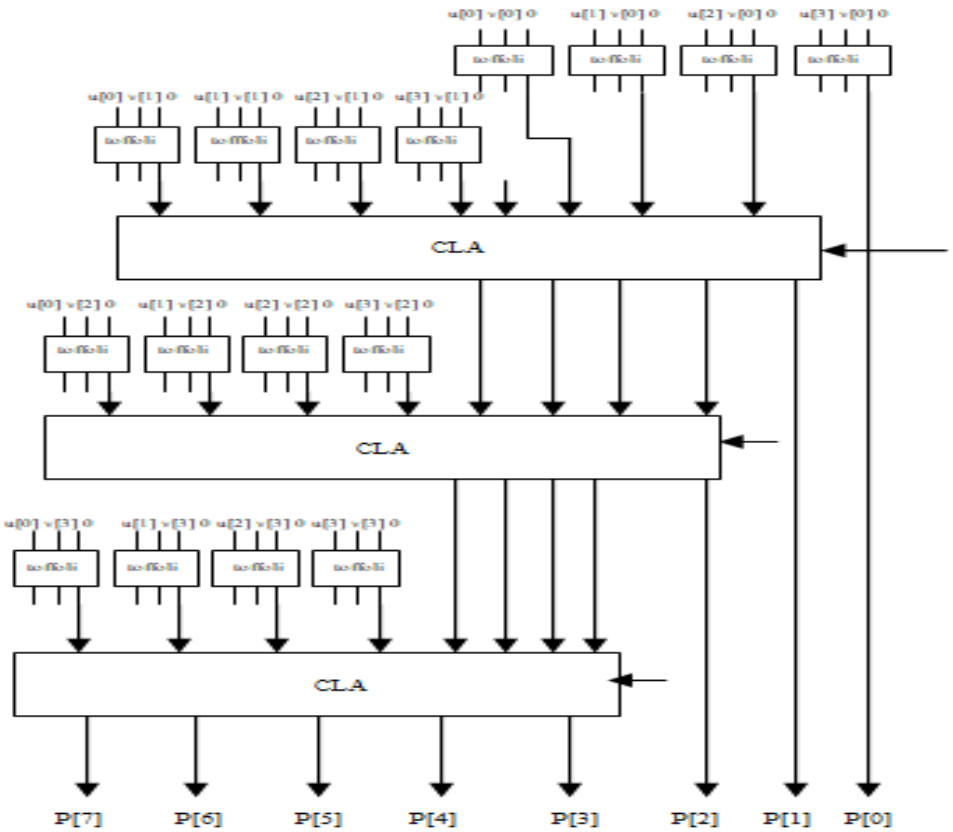

Figure 9. Circuit Diagram of the proposed 4 Bit Multiplier

4.2. Topology – 2: 4-bit multiplier in parity preserving reversible carry-look ahead adder

This topology uses the technique called parity preserving. A reversible logic gate is called is said to be parity preserved if its EXOR of inputs equals the EXOR of outputs. Not all the reversible gates are parity preserving gates. Fredkin gate, F2G gate and NFT gates are some examples of parity preserved reversible gates. The proposed topology 2 does partial product calculation using toffoli gate like topology 1. The accumulation of partial product is done using parity preserving reversible gates based look ahead carry adder. This topology 2 contains 24 number of parity preserving reversible gates. The parity preserving reversible gates utilized in this topology are F2G gate and NFT gate. Figure.11 shows the carry look adder circuit by means of the mentioned parity preserving reversible logic gates.

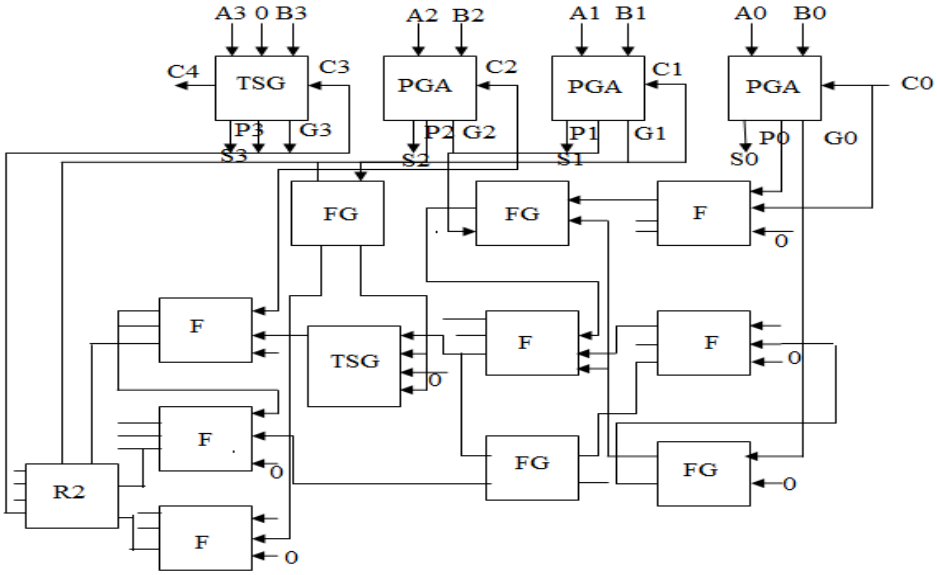

Figure 10: Topology 1 Reversible 4-bit Carry Look Ahead Adder

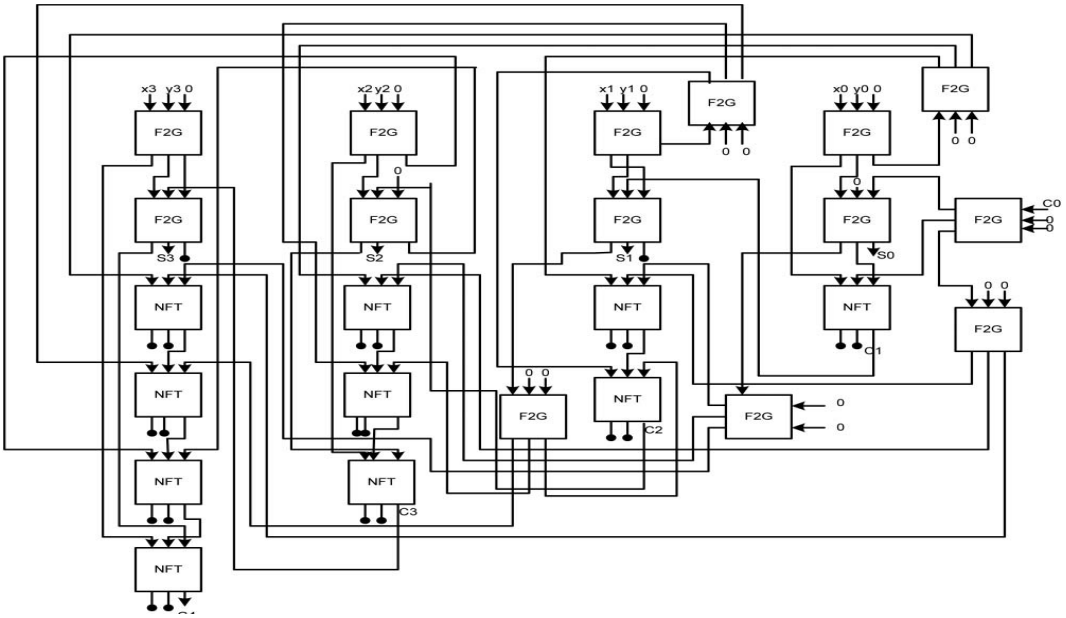

Figure 11: Topology 2 Reversible 4-bit Carry Look Ahead Adder

4.3. Topology – 3: 4-bit multiplier in modified parity preserving reversible carry-look ahead adder

This topology is similar to the previous one, but a few modifications were in the circuit diagram. As shown in Figure.12, this proposed topology 3 uses reduced number of parity preserved reversible logic gates. The difference between the proposed topology2 and topology3 is that the previous topology uses 24 reversible gates and topology 3 uses 22 reversible logic gates. This topology 3 also uses same F2G and NFT gate which are parity preserving.

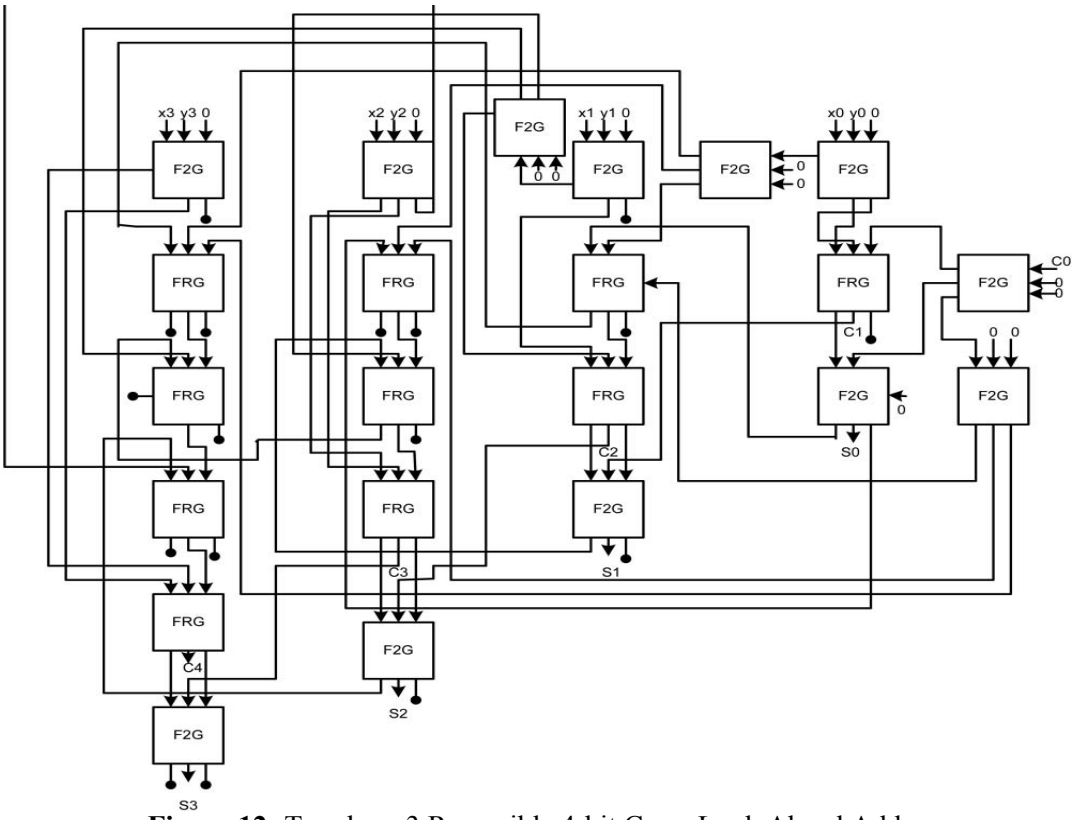

Figure 12: Topology 3 Reversible 4-bit Carry Look Ahead Adder

5. Results And Discussion

The simulation for the 4 bit reversible multiplier with all three topologies is realized using Cadence 180nm technology. The simulation waveform for the proposed multiplier using Topology 1, Topology 2 and Topology 3 is exhibited in Figure.13, Figure.14 and Figure.15 respectively. The quality evaluation matrices such as power consumption, area consumption and propagation delay for the proposed topologies are depicted in Table. I. Simulation results reveal that the proposed topology consumes 52.03 % lesser power, topology 2 consumes 63.02 % lesser power and topology 3 consumes 63.79 % lesser power when compared with an existing reversible multiplier design [18]. As the power consumption is the dominating quantity in VLSI design, the proposed topologies of multiplier design results better performance. The achieved area occupation of the proposed topology 1, topology and topology 3 are also 58.44%, 61.90% and 69.26% lesser respectively when compared with that existing reversible multiplier [18]. Also the proposed multiplier topology1 operates with 47.50% lesser propagation delay, topology 2 operates with 59.14% lesser propagation delay and topology 3 operates with 60.82% lesser propagation delay when compared with the same existing multiplier proposed in [18]. Hence the proposed multiplier topologies named as an energy efficient multipliers. Its graphical representation in regards with power, area and delay is depicted in Figure.16, Figure.17 and Figure.18 respectively.

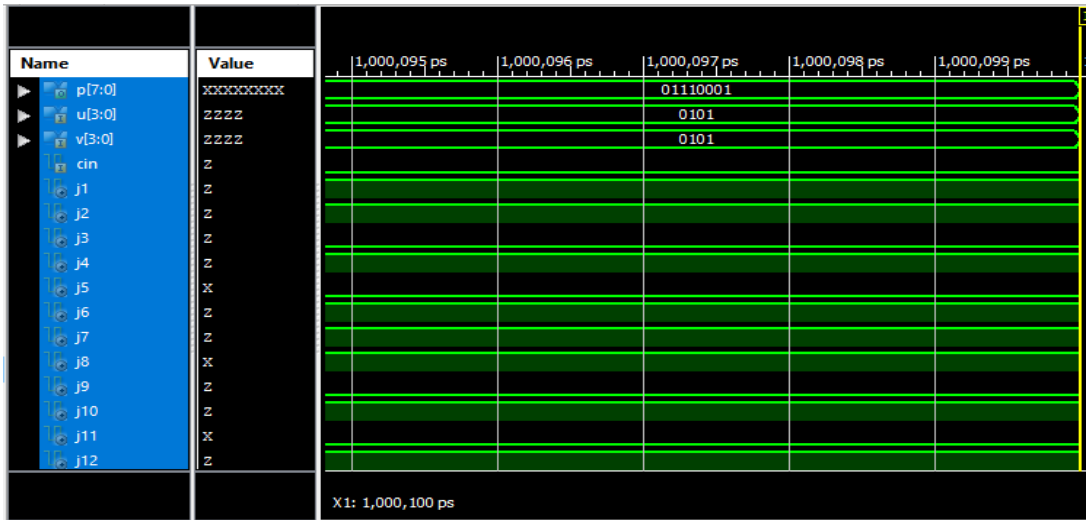

Figure 13: Simulation result of 4 Bit Reversible Multiplier using proposed Topology 1

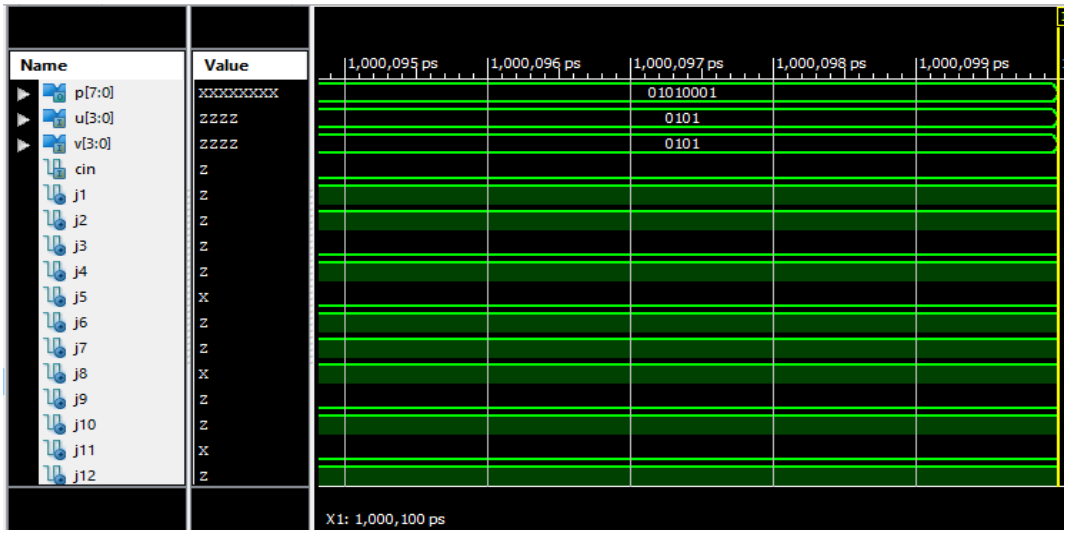

Figure 14: Simulation result of 4 Bit Reversible Multiplier using proposed Topology 2

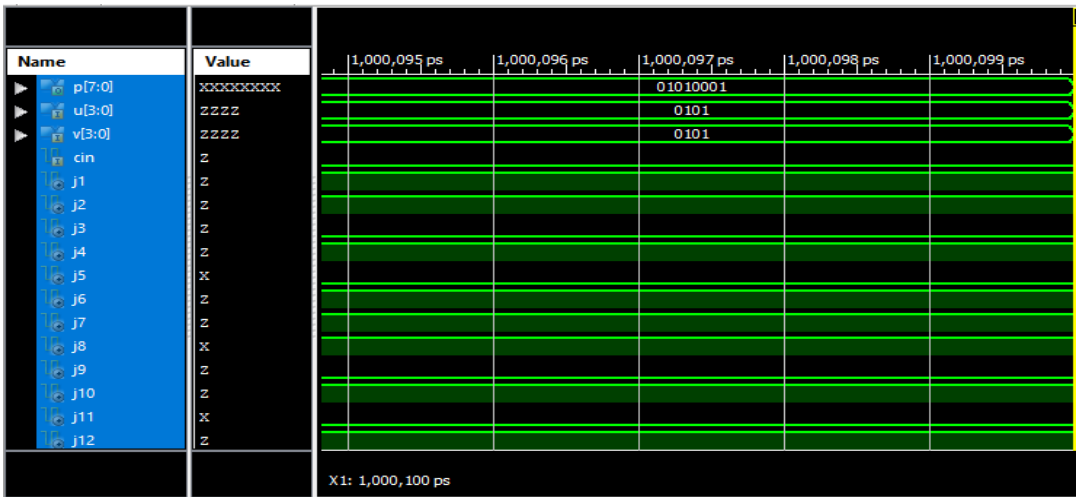

Figure 15: Simulation result of 4 Bit Reversible Multiplier using proposed Topology 3

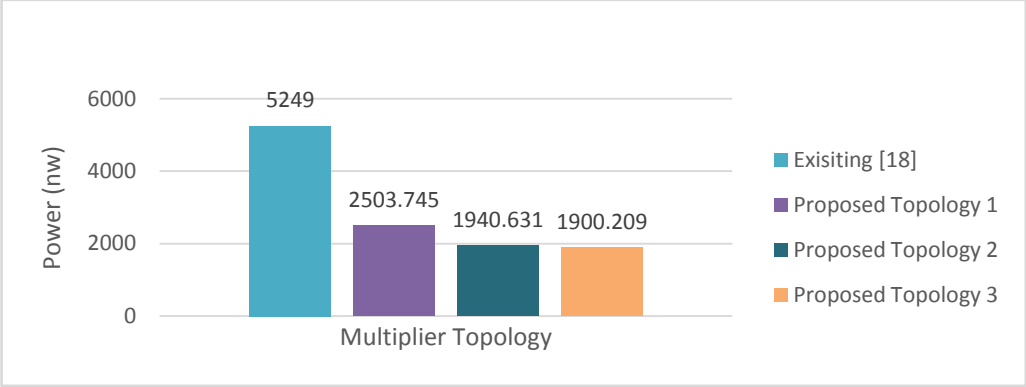

Figure 16: Graphical representation on power comparison of different multiplier topologies

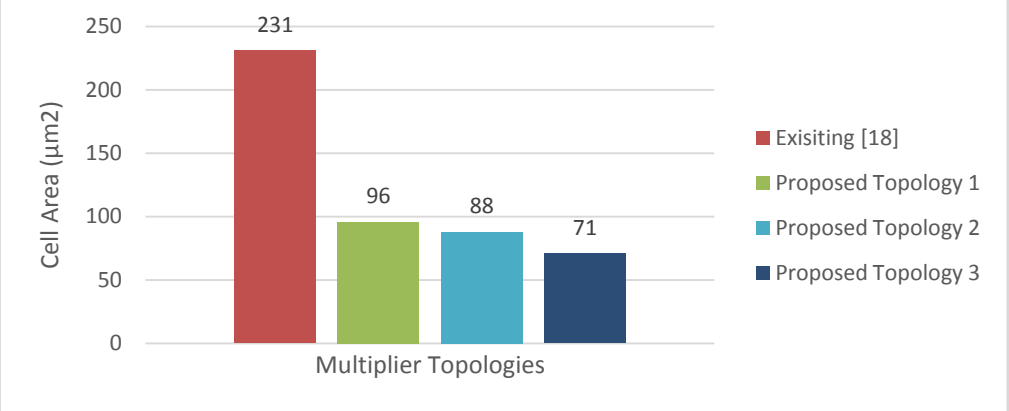

Figure 17: Graphical representation on Cell Area of different multiplier topologies

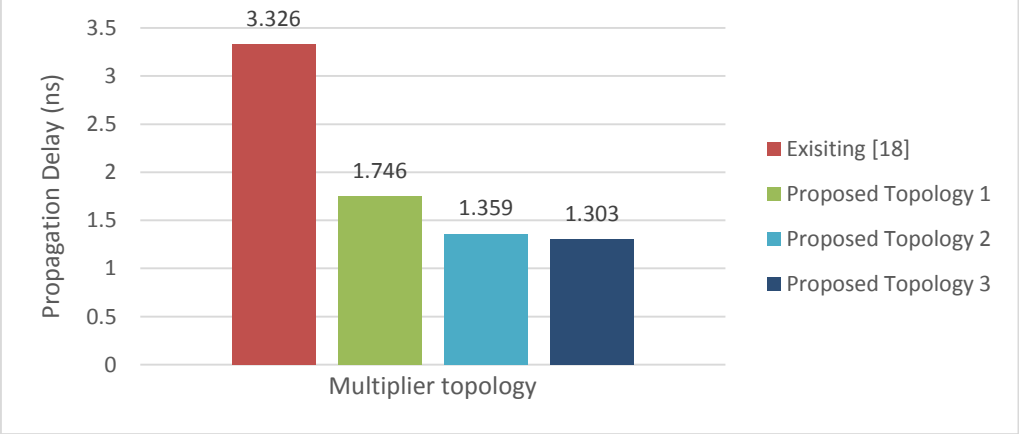

Figure.18: Graphical representation on Propagation Delay of different multiplier topologies

Table 1 Comparative Analysis

Multiplier topology	Power (nw)	Cell area (μm^2)	No of Gates	Propagation Delay (ns)
Existing multiplier [18]	5249	231	28	3.326
Proposed Topology 1	2503.745	96	28	1.746
Proposed Topology 2	1940.631	88	28	1.359
Proposed Topology 3	1900.209	71	28	1.303

6. Conclusion

The implementation of 4 bit reversible multiplier is done in this letter. The proposed implementation separated into three topologies such as reversible multiplier based on toffoli gate and carry look ahead adder, reversible multiplier with the help of toffoli gate and carry look ahead adder using parity preserving reversible gates and reversible multiplier based on toffoli gate and modified carry look ahead adder with the help of parity preserving reversible gates. Simulation was done using Cadence 180 nm technology. As given in section 5, the proposed reversible multiplier achieves lesser power consumption, occupies lesser area and operates with higher speed when compared with [18]. This energy efficient reversible multiplier is useful in the basic arithmetic unit in Microprocessors, DSP processors and quantum computers.

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