Technical Overview

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Processor Type

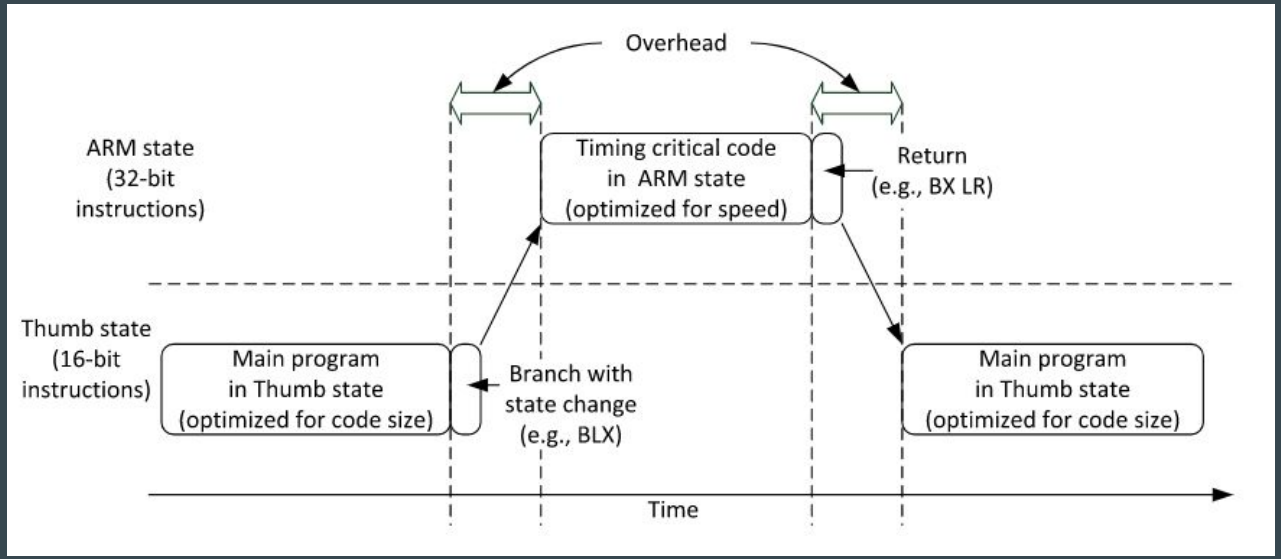
- All Cortex-M processors are 32bit RISC processors
  - 32 bit registers
  - 32 bit internal data path
  - 32 bit bus interface
- Can handle 8bit, 16bit and 64bit data efficiently
- Have three state pipeline (instruction patch, decode, execution)
- There is only one 4GB unified memory space
- Based on load-store architecture.
  - load a data from SRAM into a register
  - process
  - written back into SRAM

Processor Architecture

- Architecture :
  - Instruction Set Architecture(ISA),
  - programmer model (what the software sees)
  - debug methodology (what the debugger sees)
- Micro architecture
  - Implementation specific detail (interface signals, instruction execution time, etc)
- An instruction architecture can be implemented with various micro architecture
- For programmer, we just need to read “Generic User guide”
- http://infocenter.arm.com
  - Cortex-M series processors
    - Cortex-M0/M0þ/M3/M4
      - Revision number
        - Cortex-M4/M3/M0/M0þ Devices Generic User Guide

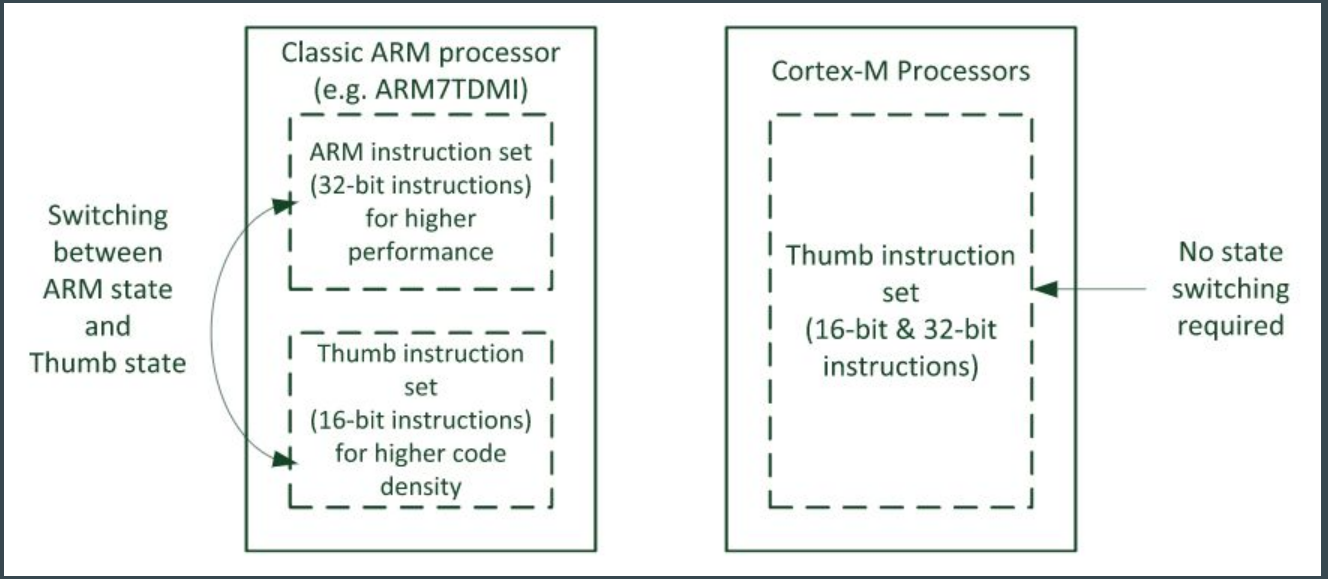
Instruction Set

- Switching between ARM code and Thumb code in class ARM processors such as the ARM7TDM

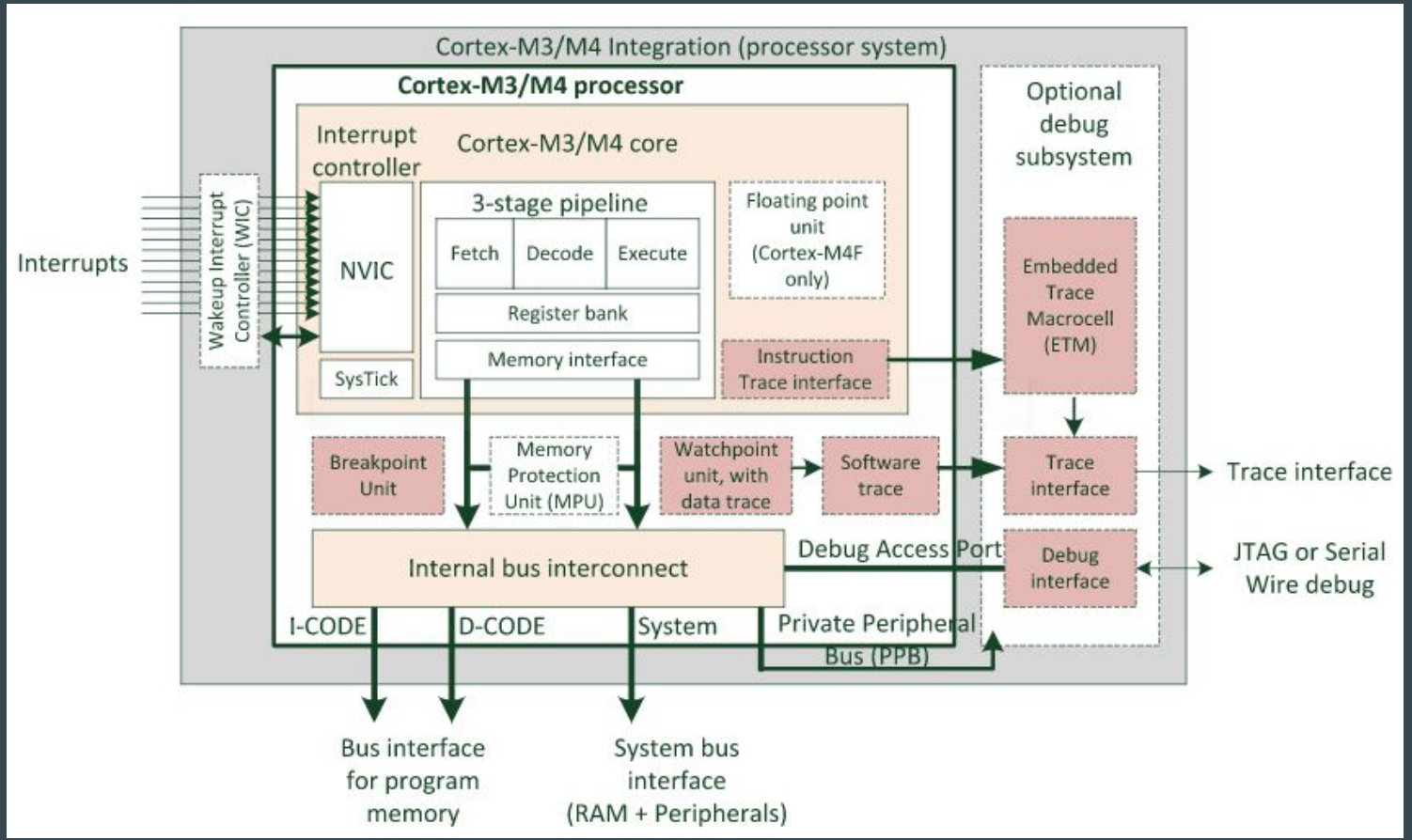


Instruction Set

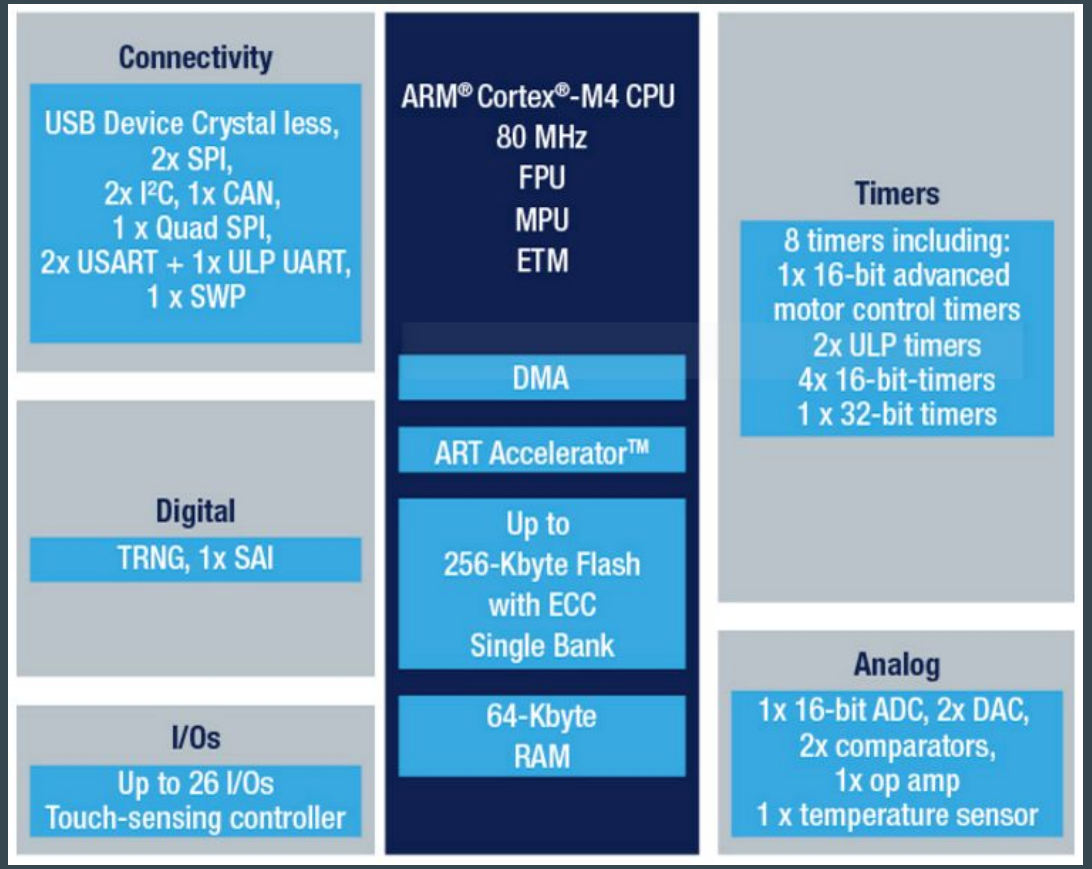
- Thumb2 allows mixture of 16-bit and 32-bit instructions for high code density and high efficiency



Block Diagram



STM32L432


Connectivity
USB Device Crystal less,
2x SPI,
2x I²C, 1x CAN,
1 x Quad SPI,
2x USART + 1x ULP UART,
1 x SWP
Digital
TRNG, 1x SAI
I/Os
Up to 26 I/Os
Touch-sensing controller
ARM® Cortex®-M4 CPU
80 MHz
FPU
MPU
ETM
DMA
ART Accelerator™
Up to
256-Kbyte Flash
with ECC
Single Bank
64-Kbyte
RAM
Timers
8 timers including:
1x 16-bit advanced
motor control timers
2x ULP timers
4x 16-bit-timers
1 x 32-bit timers
Analog
1x 16-bit ADC, 2x DAC,
2x comparators,
1x op amp
1 x temperature sensor

Memory System

- Cortex-M processor does not include memories but generic on-chip bus interface.
- Microcontroller vendors add their own memory system
  - Program memory (Flash)
  - Data memory (SRAM)
  - Pheripherals
- The bus interface is based on AMBA (Advanced Microcontroller Bus Architecture). This is becoming de facto in industry.
  - Main bus protocol : AHB Lite (Advanced High-performance Bus)
  - Peripheral bus protocol : APB (Advanced Peripheral Bus)
- No need to initialize at boot time

Interrupt and exception support

- Interrupt controller : NVIC (Nested Vectored Interrupt Controller)
- It is programmable and registered are memory mapped
- The address location is fixed and the programming model on NVIC is same across all Cortex-M processors
- NVIC supports several exceptions (NMI, exception sources in processor)

Performance, Code density and Low Power

- Each instruction fetch is 32-bit, and most instructions are 16-bit. Therefore up to two instructions can be fetched at a time.
- It is now possible to add low-cost graphical interfaces to embedded devices
- Single Instruction, multiple data (SIMD) instruction support exists in **Cortex-M4**
- Single precision floating point instructions are available in **Cortex-M4**
- STM32L4 MCU series
    - Excellence in ultra-low-power with performance

http://www.st.com/resource/en/product_presentation/stm32l4_marketing-pres.pdf

http://www.eembc.org/ulpbench/

Memory System, Memory Protection Unit and Interrupt

- Harvard bus architecture (Instruction bus and Data bus) cf) Von Neumann
- Support big endian and little endian memory system
- MPU (Memory Protection Unit) : Optional
  - If an MPU is included, applications can divide the memory space into a number of regions and define the access permissions for each of them
  - For example, separate kernel process and user process. Make read only memory region
- Microcontroller vendors decide how many interrupts and exceptions are used.
  - Up to 240 interrupts
  - Priority level can changed dynamically
  - Vector table can be located at any address (default 0x0 address)

OS support and system level features

- Have a built in system tick timer called SysTick
- Banked stack pointer :
  - MSP : Main Stack Pointer for OS and interrupt (Default, this is used on without OS)
  - PSP : Process Stack Pointer for user process
- Support privileged and non-privileged mode
  - Processes start in privileged mode by default
  - can be used with MPU
- Cortex-M4 specific
  - include DSP extentions and single precision floating point unit (FPU)
  - SIMD (for example, can be used right and left channel audio processing)
  - Single-cycle 16-bit, dual 16-bit, and 32-bit Multiply and Accumulate (MAC).
  - ARM Support DSP library

Debug Support, Scalability and Compatibility

- Support up to 8 hardware comparators for breakpoint in FPB (Flash Patch and Breakpoint Uint)
- Have 4 hardware watchpoint comparators in DWT (Data Watch point Trace)
- JTAG or Single-wire debug (SWD) can be used