期末考講解

第一題（8 分）

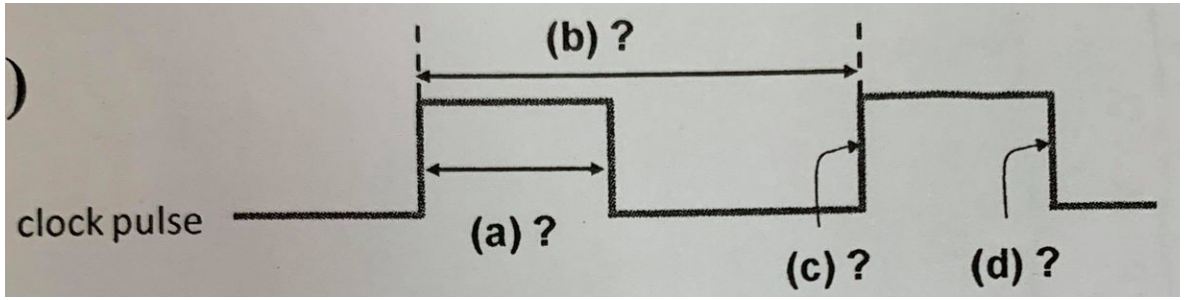
1. Define the four items in the right fugure.

a. clock width

b. clock period

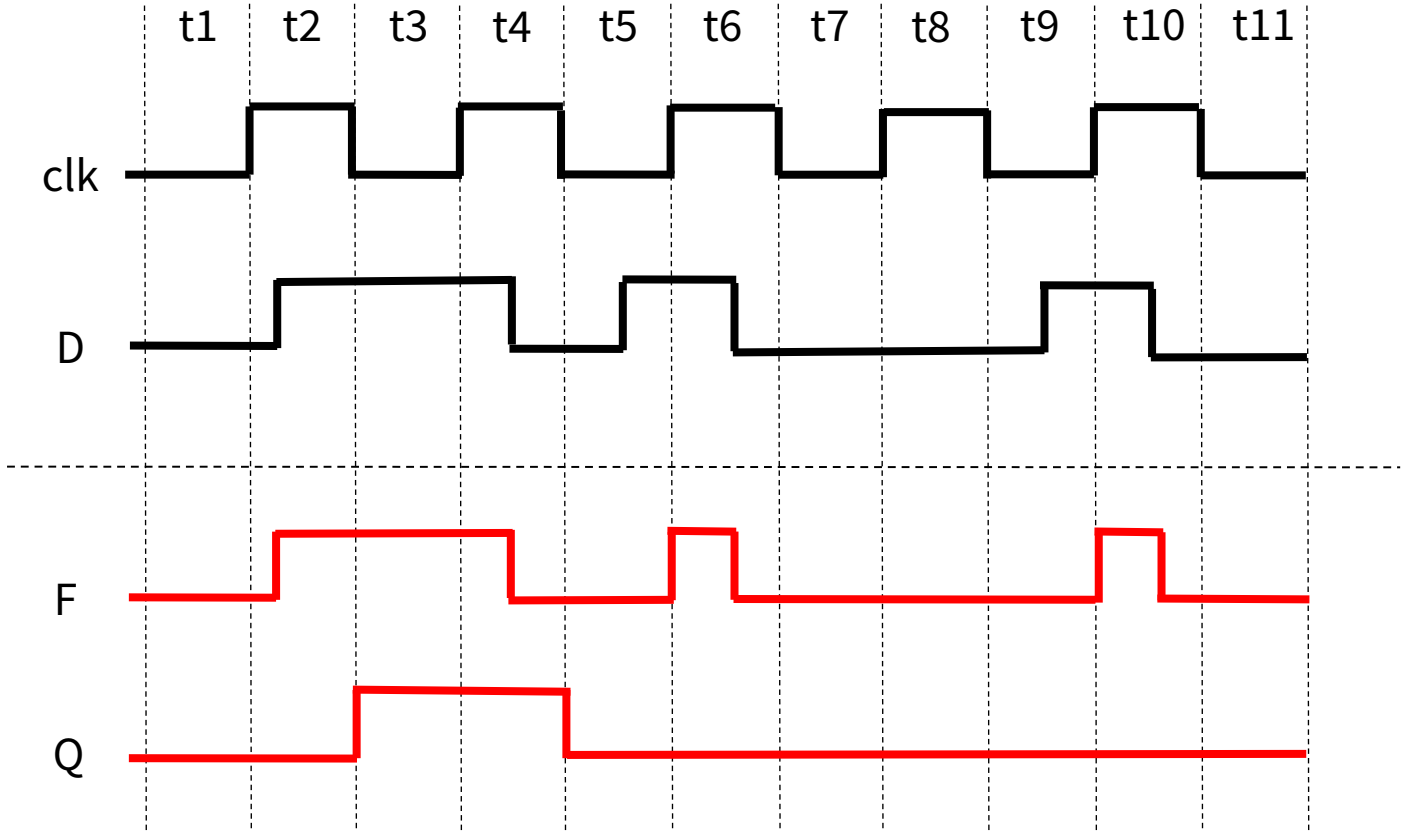
c. rising edge (positive edge)

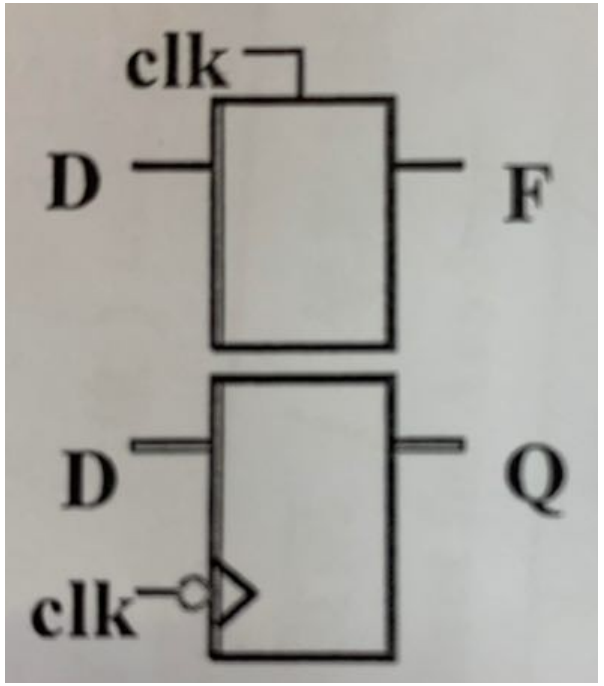
d. falling edge (negative edge)



第二題（10 分）

2. Define the timing output of latch and flip-flop.

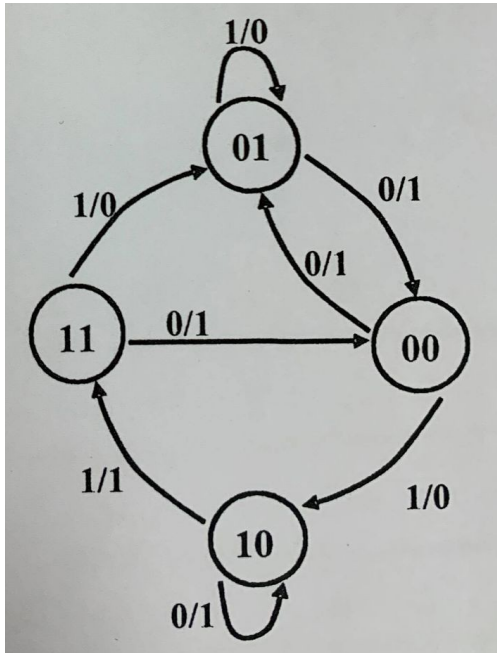




第三題（10 分）

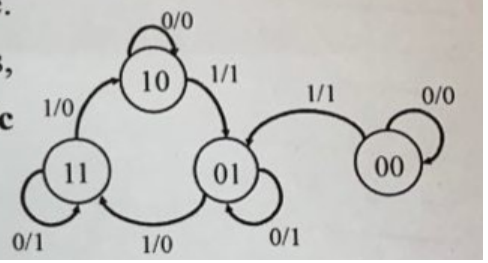
3. Draw the state table by using the stage diagram shown in the figure.

Present State	Input	Next State	Output
00	0	01	1
00	1	10	0
01	0	00	1
01	1	01	0
10	0	10	1
10	1	11	1
11	0	00	1
11	1	01	0



第四題（20 分）

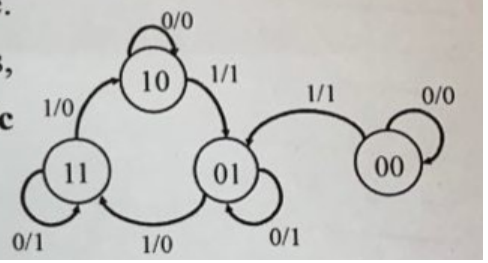
4. The state diagram of a circuit is shown in the right figure. Implement it by using (a) JK flip-flops and (b) D flip-flops, respectively. Please draw (a)**state table** and (b)**circuit logic diagram** of the two implementations, respectively. **(20%)**

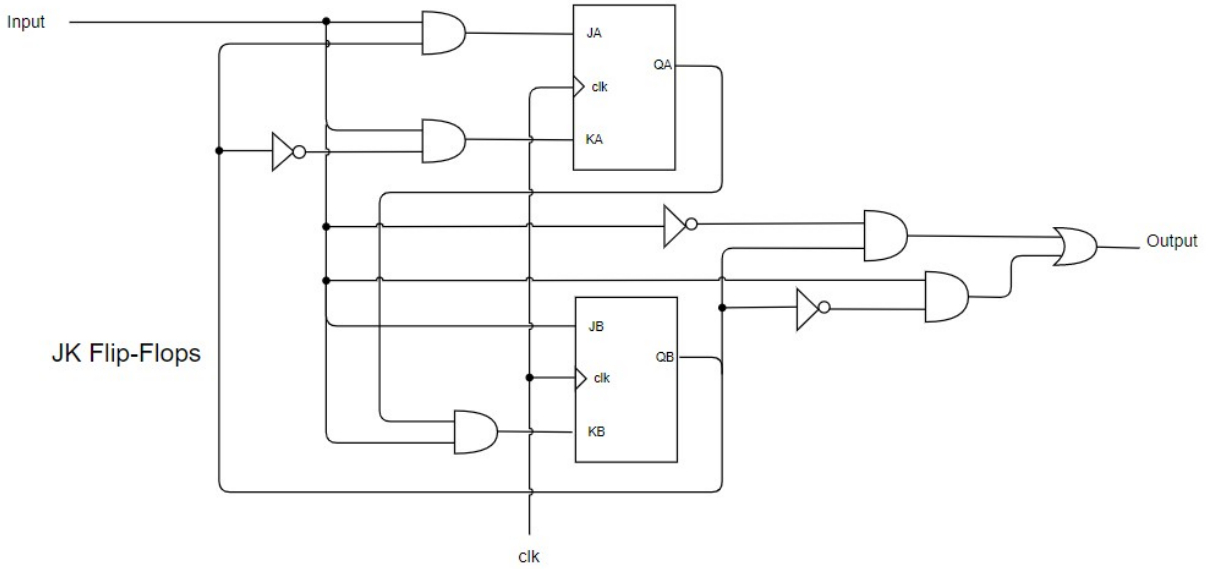


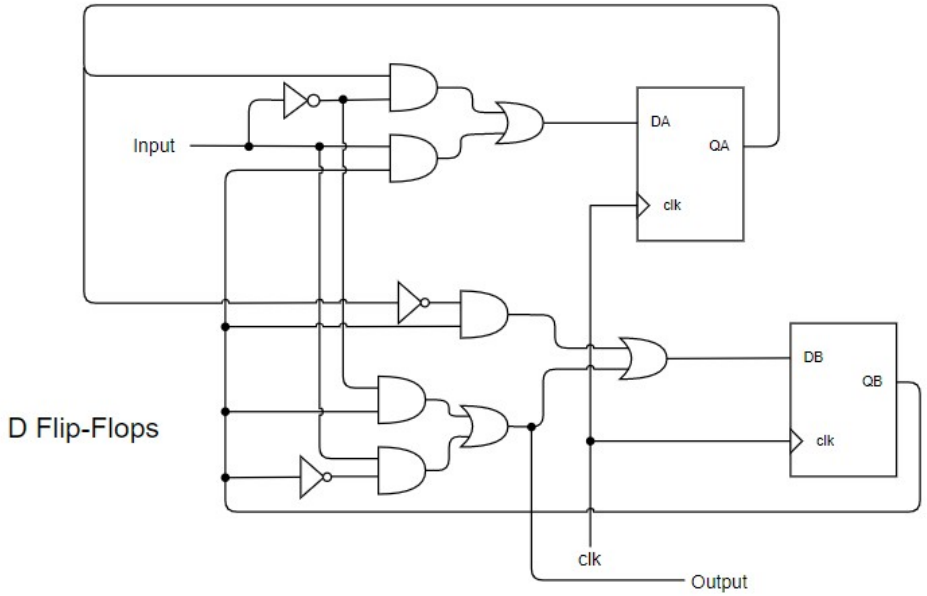
Current state	Input	Next state	output						
00	0	00	0	0	0	0	X	0	X
00	1	01	1	0	1	0	X	1	X
01	0	01	1	0	1	0	X	X	0
01	1	11	0	1	1	1	X	X	0
10	0	10	0	1	0	X	0	0	X
10	1	01	1	0	1	X	1	1	X
11	0	11	1	1	1	X	0	X	0

第四題（20 分）

4. The state diagram of a circuit is shown in the right figure. Implement it by using (a) JK flip-flops and (b) D flip-flops, respectively. Please draw (a)**state table** and (b)**circuit logic diagram** of the two implementations, respectively. **(20%)**







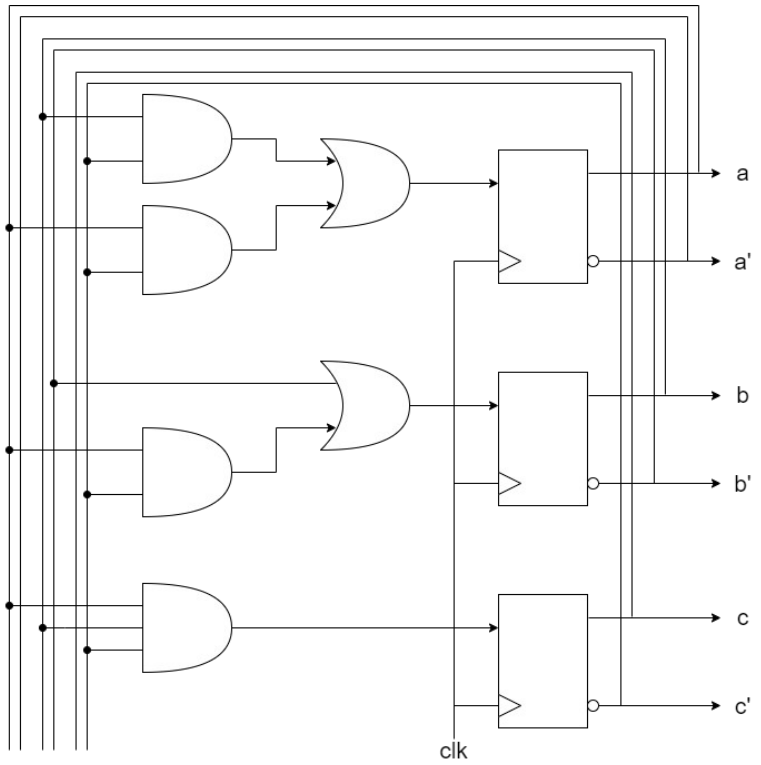
第五題（20 分）

5. Please use the positive-edge-triggered D flip-flops and JK flip-flops to design a 3-bit synchronous counter with the following repeated binary sequence: 000→010→100→110→111→000→010→100→110→111→000... . Please draw its (a) **state table** and (b) **circuit logic diagram (20%)**.

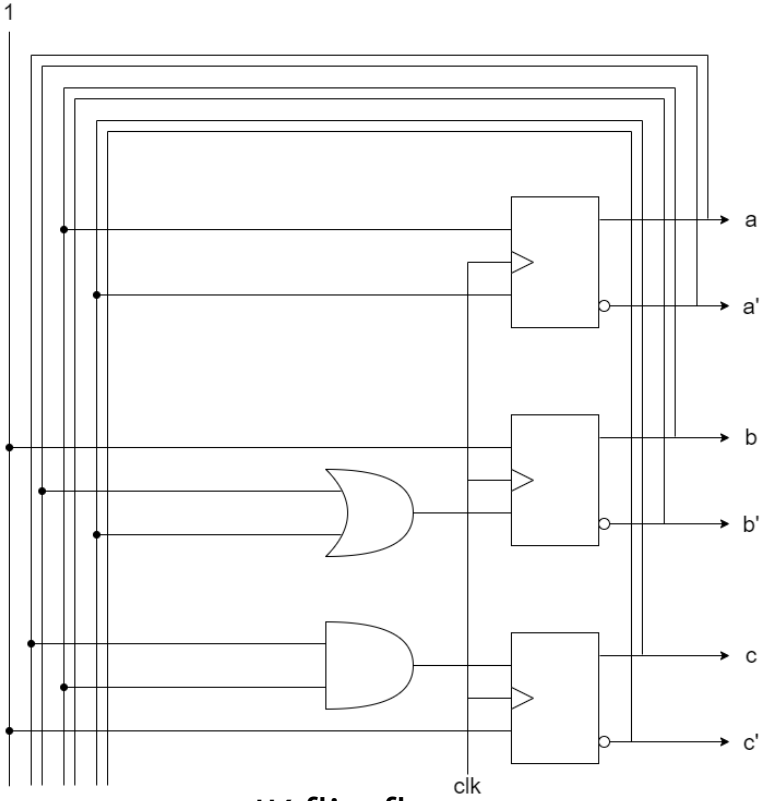
Current state			Next state			JK flip-flop set up					
A	B	C	a	b	c	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	1	0	0	X	1	X	0	X
0	0	1	X	X	X	X	X	X	X	X	X
0	1	0	1	0	0	1	X	X	1	0	X
0	1	1	X	X	X	X	X	X	X	X	X
1	0	0	1	1	0	X	0	1	X	0	X
1	0	1	X	X	X	X	X	X	X	X	X
1	1	0	1	1	1	X	0	X	0	1	X

第五題（20 分）

5. Please use the positive-edge-triggered D flip-flops and JK flip-flops to design a 3-bit synchronous counter with the following repeated binary sequence: 000→010→100→110→111→000→010→100→110→111→000... . Please draw its (a) **state table** and (b) **circuit logic diagram (20%)**.



D flip-flop



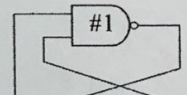
JK flip-flop

第七題（12 分）

Describe the differences of the following terms in detail. **(12%)**

a. **combinational circuit vs. sequential circuit**

b. **latch vs. flip-flop**



(a) Combinational circuits: 沒有記憶單元，輸出僅與現在輸入有關。
Sequential circuits: 有 feedback path ，輸出與當前輸入及當前狀態有關。

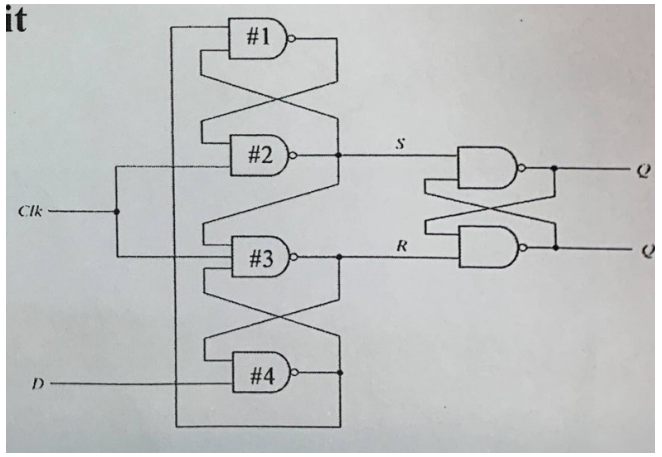
(b) Latch :
1. level triggered.
2. multiple transitions might happen during logic-1 level.

Flip flop :
1. edge triggered.
2. eliminate the multiple-transition problem

第八題（14 分）

Explain the following terms happened in the D flip-flop shown in the right figure: **(14%)**

(a) hold time **(b) setup time**



(a) D input must not changes after the application of the positive Clk pulse.
= the propagation delay of gate 3.
clock to the internal latch.

(b) D input must be maintained at a constant value prior to the application
of the positive Clk pulse
= the propagation delay through gates 4 and 1
data to the internal latches