

第二次期中考解答

第一題

- Discuss the advantages of the two different 4-bit adders mentioned in the class

	Advantage	Disadvantage
Ripple adder	成本低	速度慢
Carry look ahead adder	速度快	成本高

第二題

- A. combinational circuit vs. sequential circuit
 - 沒有記憶單元，輸出與目前輸入有關
- B. synchronous sequential circuit vs. asynchronous sequential circuit
 - 有記憶單元，輸出與現在的 input 與現在的 state(或是先前輸出) 有關

第三題

- A. even parity
 - 加入一個額外的 bit ，讓所有位元 1 的個數為偶數個
- B. priority encoder
 - 優先權編碼器，較高位的位元優先權高於較低的位元

第四題

A. 此 circuit 為 4-bit 的加減法器
當 $M = 0$ 時，為 $A+B$
當 $M = 1$ 時，為 $A-B$
(需舉例說明)

B. 此 XOR 用來檢查是否 overflow
(需舉例說明)

$V=0$ 無 overflow

$V=1$ 有 overflow

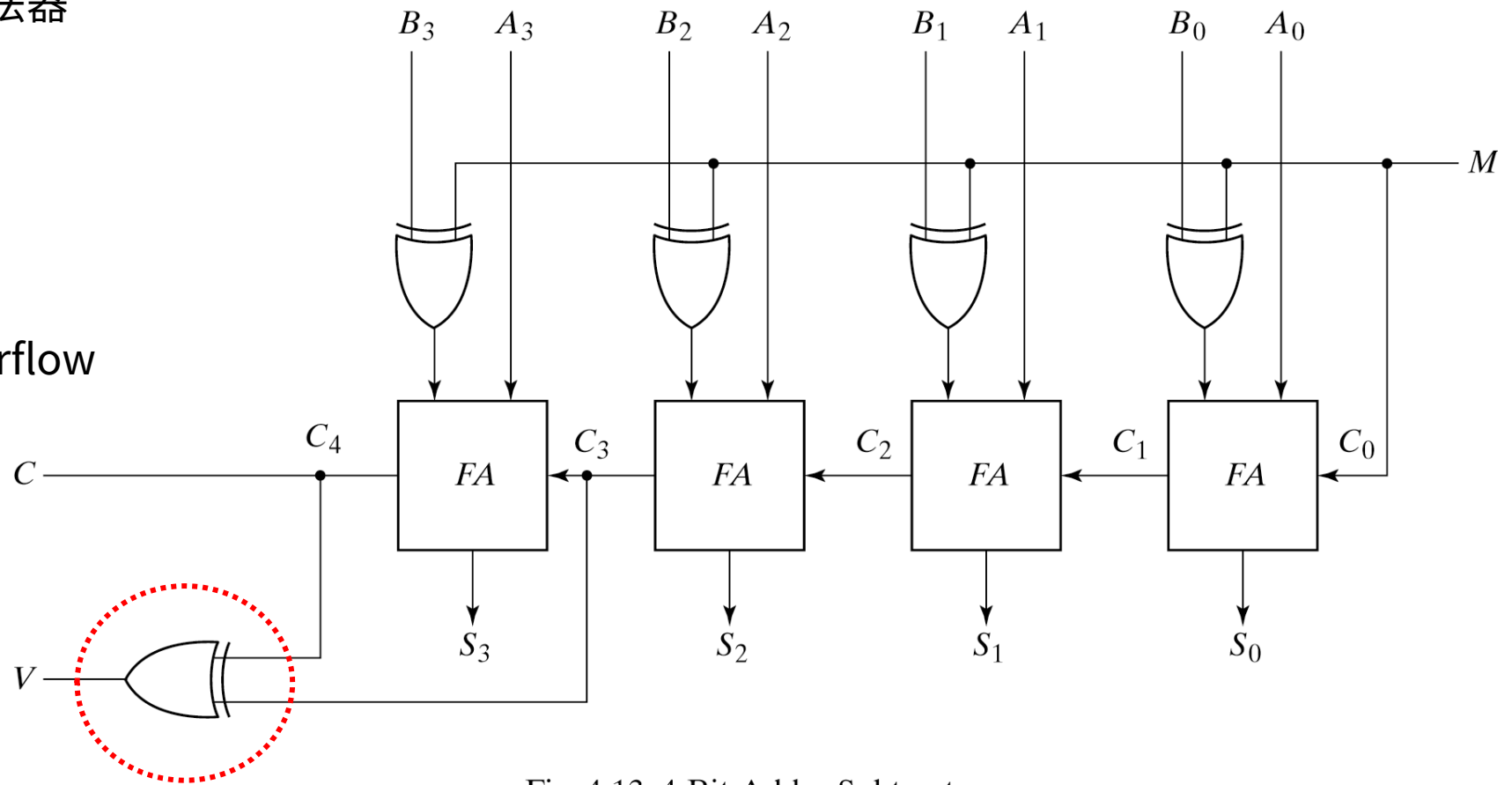
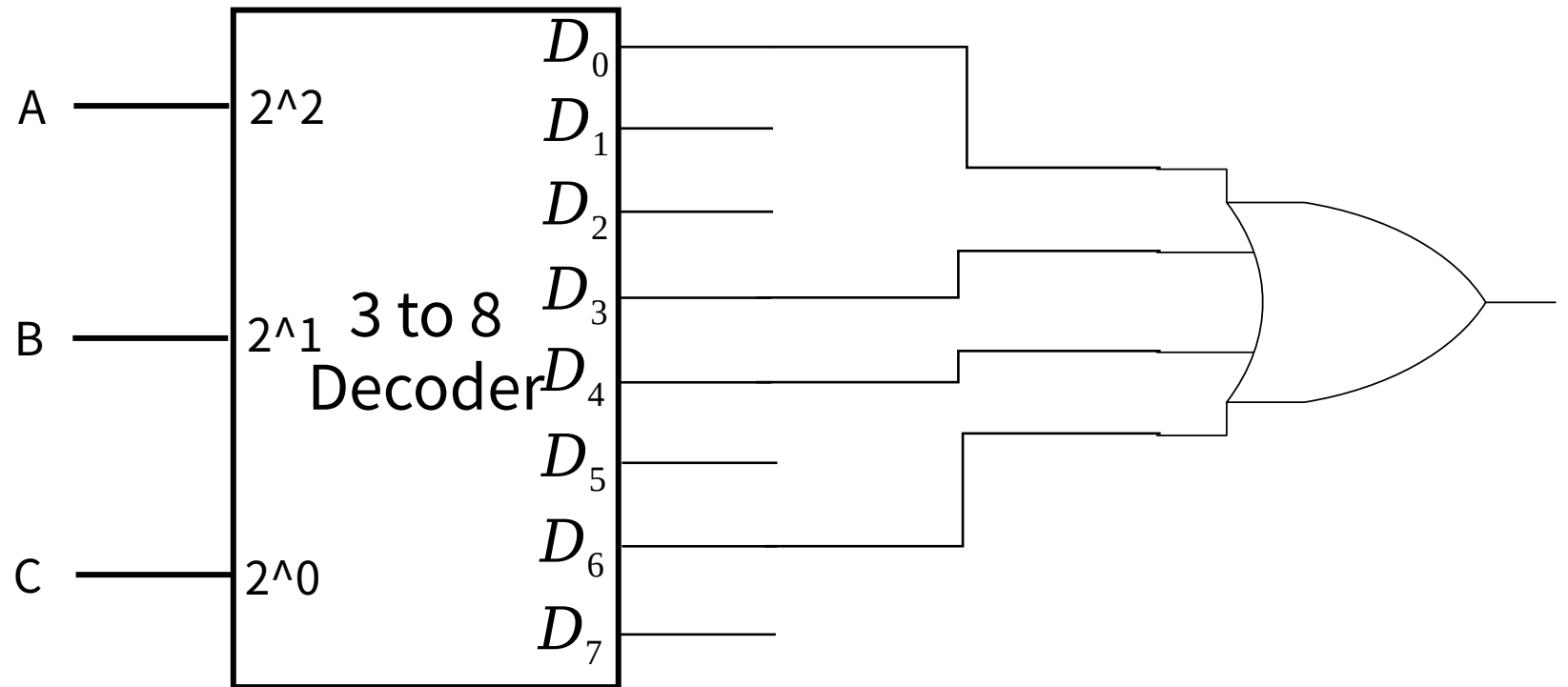


Fig. 4-13 4-Bit Adder Subtractor

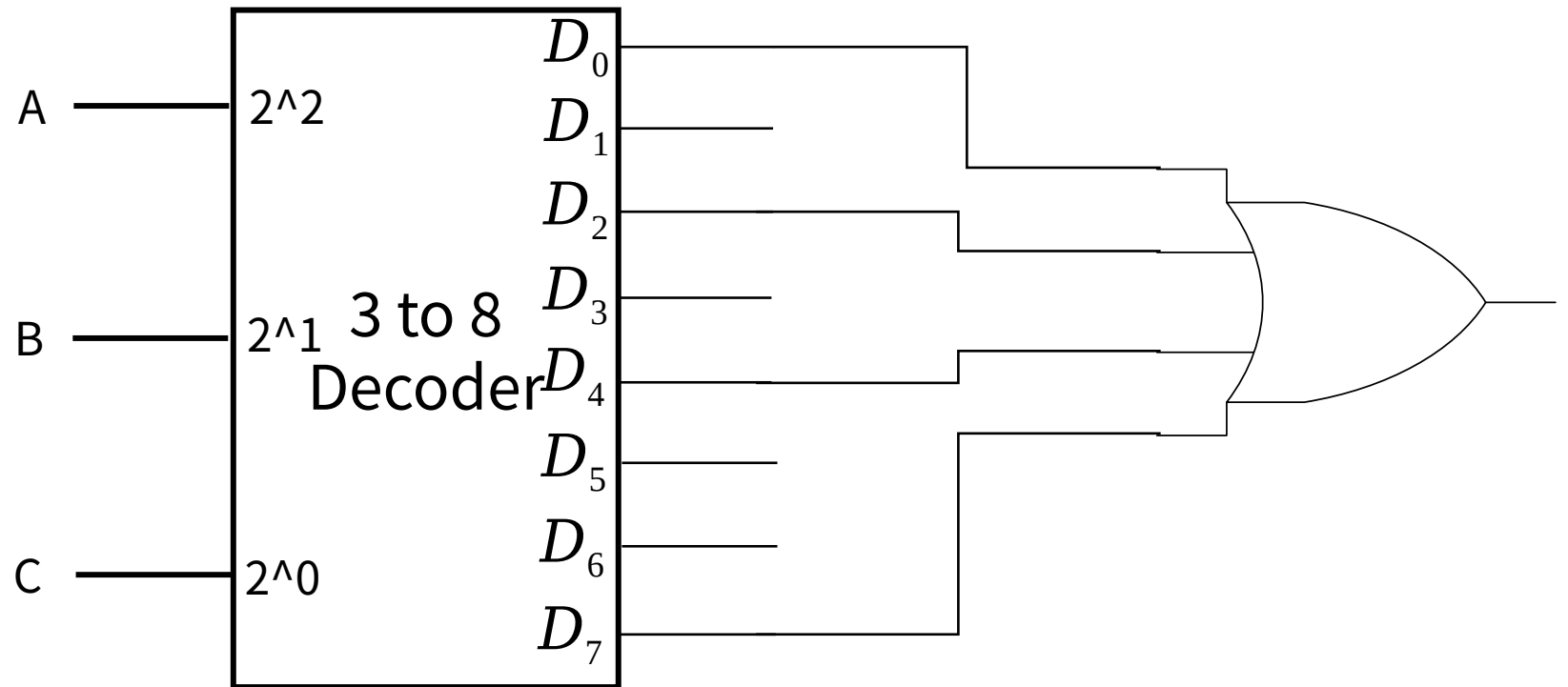
第五題

- A. $F(A,B,C) = A' B' C' + AB' C' + A' BC + ABC'$



第五題

- B. $F(A,B,C) = ABC + A' B' C' + A' BC' + AB' C'$

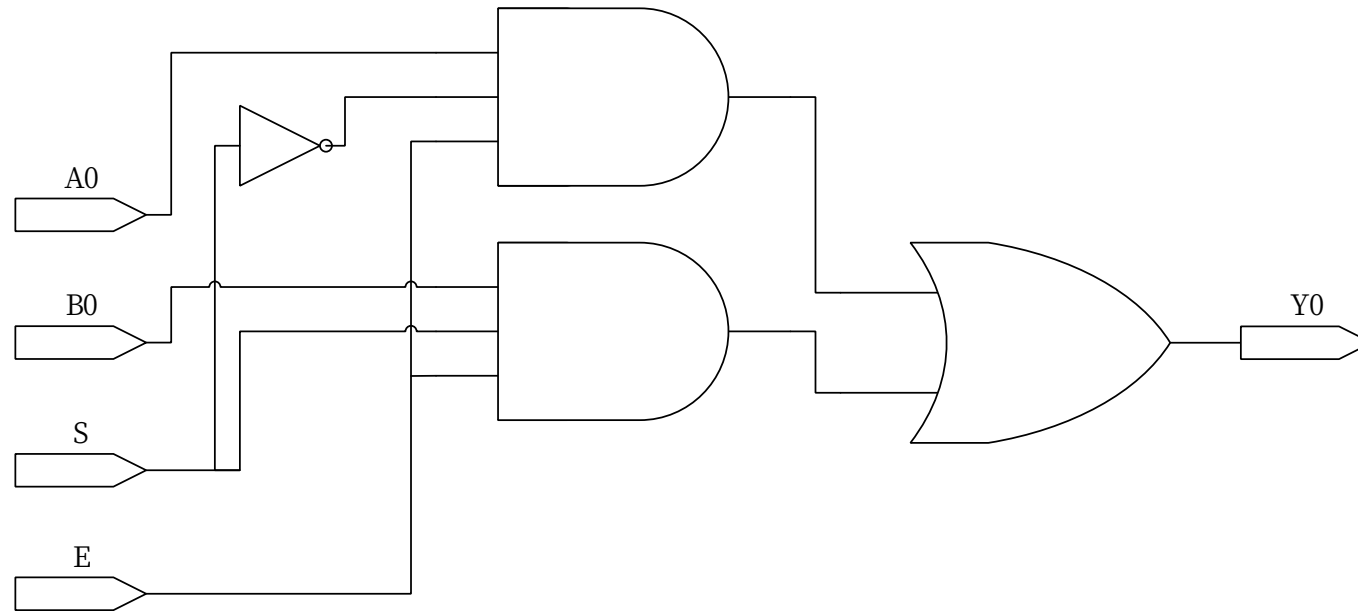


第六題

- Design an **active-high** one bit 2-1multiplexer with an **active-high** enable signal. Please draw its **Function Table** and **Logic Diagram**

E	S	Output Y0
0	X	All 0' s
1	0	Select A0
1	1	Select B0

第六題

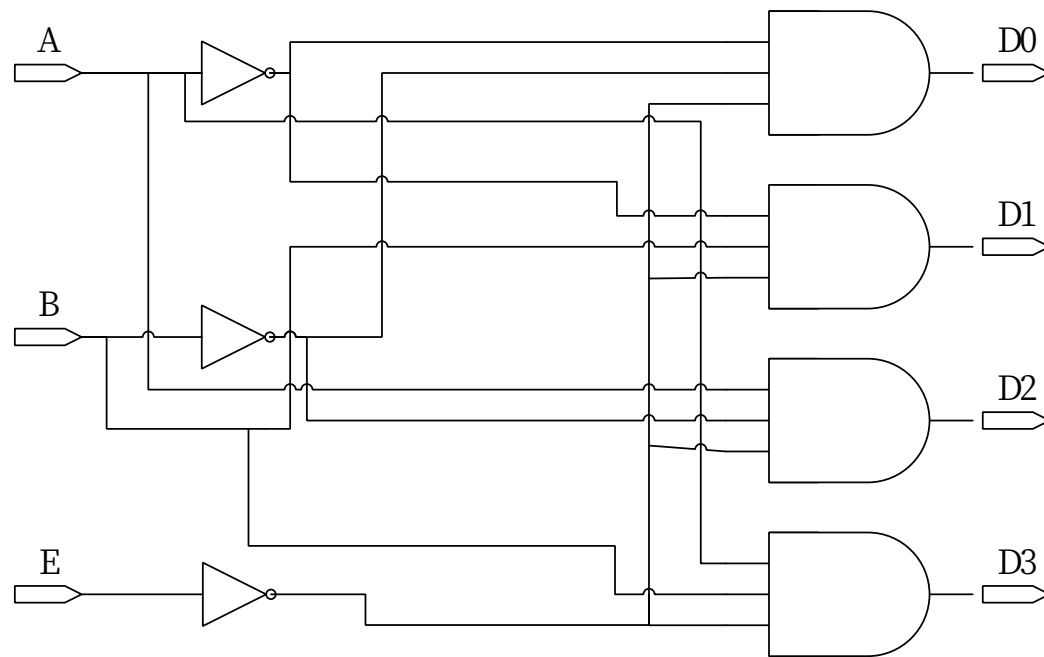


第七題

- Design an **active-high** 2-to-4 decoder with an **active-low** enable signal. Please draw its **Function Table** and **Logic Diagram**

E	A	B	D0	D1	D2	D3
1	X	X	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	1	0	0	0	1

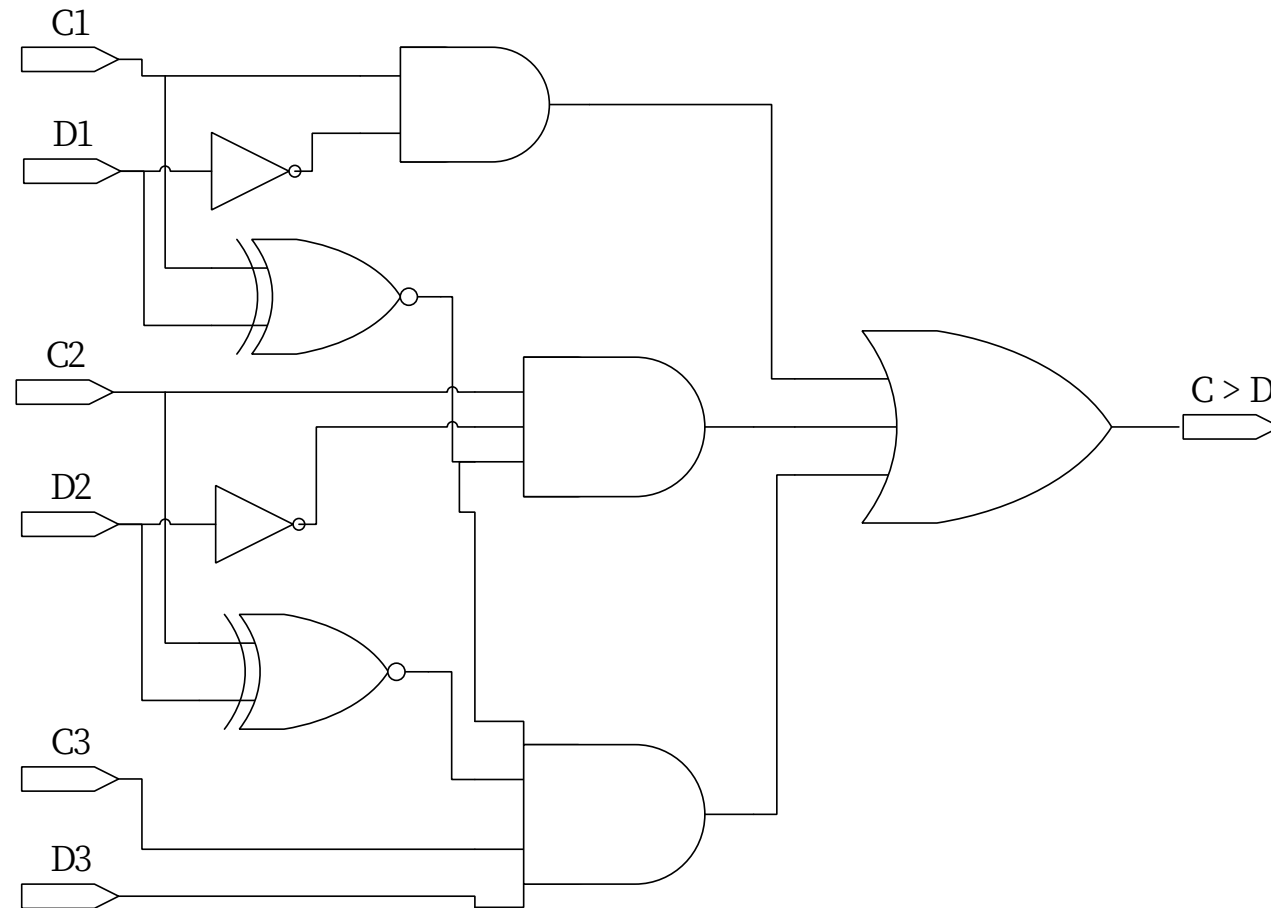
第七題



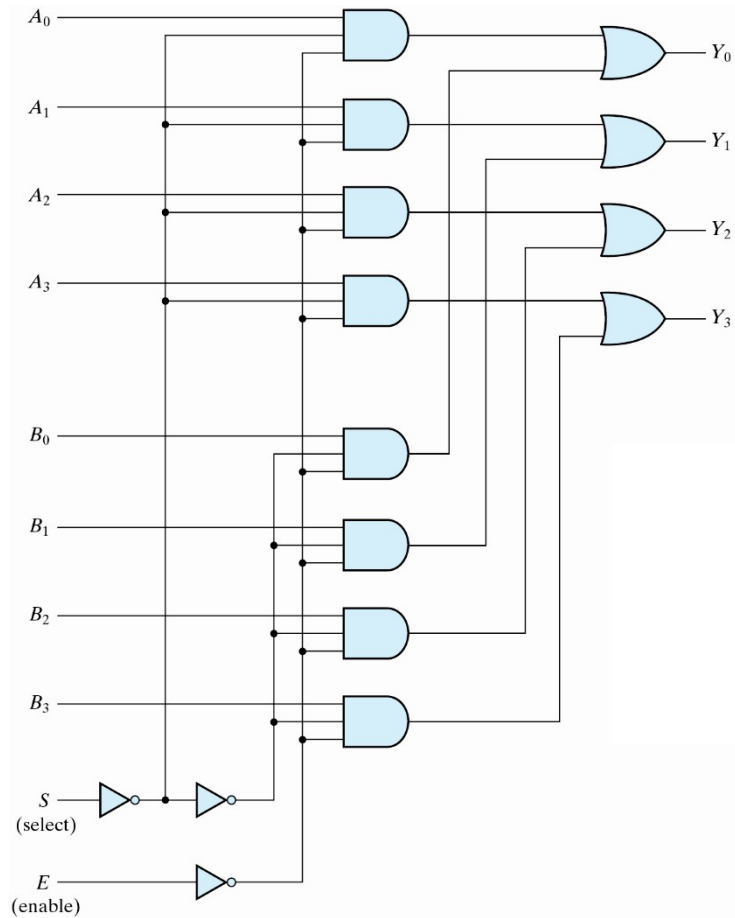
第八題

- Design a 3-bit comparator which can output 1 if $C > D$. Please write its **Boolean function** and draw its **Logic Diagram**
 - (exclusive-nor)
 - ,
 - $C > D = C_1 D_1' + x_1 C_2 D_2' + x_1 x_2 C_3 D_3'$

第八題



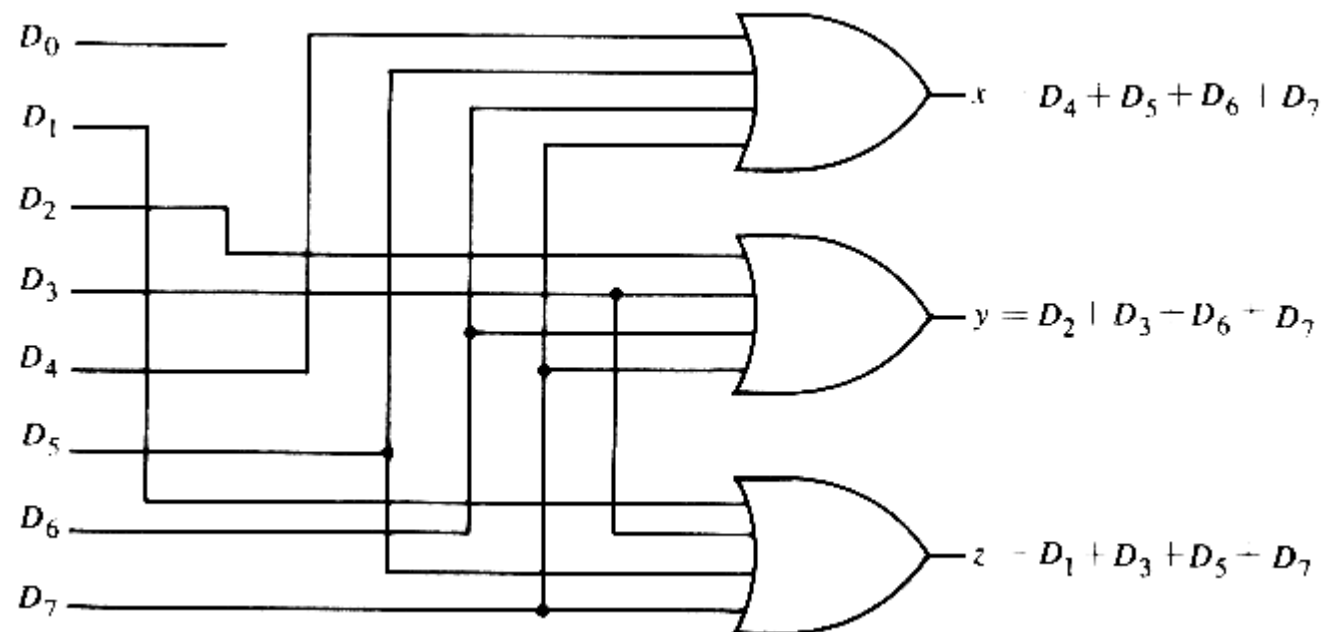
第九題



此電路為 two-to-one multiplexer (4bits)

<u>E</u>	<u>S</u>	<u>output Y</u>
1	X	all 0' s
0	0	select A
0	1	select B

第九題



此為 8-to-3 Encoder

Table 4.7
Truth Table of an Octal-to-Binary Encoder

Inputs								Outputs		
D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	x	y	z
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

第十題

- Design a **nor circuit** to convert the 4-bit binary code to the 4-bit gray code

$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

$G_3 = B_3$

$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

$G_2 = ((B_3 + B_2)' + (B_3 + B_2))'$

第十題

$B_1B_0 \backslash B_3B_2$	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	0	0	1	1

$B_1B_0 \backslash B_3B_2$	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	0	1	0	1
10	0	1	0	1

$$G_1 = ((B_2 + B_1)' + (B_2 + B_1))' + ((B_2 + B_1)' + (B_2 + B_1))'$$

$$G_0 = ((B_1 + B_0)' + (B_1 + B_0))' + ((B_1 + B_0)' + (B_1 + B_0))'$$

第十題

