# Stick diagram representation for nanomagnetic logic based combinational circuits

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***Abstract*—Nanomagnetic logic (NML) is considered as the most promising post CMOS technology to realize system on chip (SoC) applications. In NML, the magnetostatic interactions evolve to a domain orientation, which is viewed as a logical level. The NML is based on the single domain behavior of the dots, and combinational circuits are realized by arranging the dots in ferromagnetic and antiferromagnetic order in a plane. Stick diagram in CMOS technology not only provides topographical and mask layer information, but also presents a quick footprint estimation of the designed subsystem. In this paper, ML based full adder circuit is designed in OOMMF, a micromagnetic simulation tool, and stick diagram representation for NML technology is proposed to design higher order digital subsystem.**

***Keywords— adder, stick diagram, layout, magnetic logic device, nanomagnets.***

## INTRODUCTION

Following Moore's law, the shrinking size of CMOS transistor presents short channel problems, leakage current issues, contention current and high static and dynamic power dissipation challenges [1]. Nanomagnetic logic (NML) device is considered as a feasible alternative to CMOS technology to realize digital circuits [2]. The NML device inherits magnetostatic interaction between the dots and generates a desired domain orientation [3]. Shape anisotropy driven single domain nanomagnets renders two distinct magnetic states based on the domain orientation [4], which is viewed as bistable logic output levels. The combinational circuit presented in this paper utilizes the single domain behavior of the ferromagnetic nanodots, which are closely coupled to each other. The proposed stick diagram developed for NML based combinational subsystem offers quick approximation of the footprint, required to design higher order subsystems on a chip.

The minimum energy to switch domains in a nanomagnetic dot is observed in permalloy patterned dots [5], [6]. The ferromagnetic ordering (FO) and anti-ferromagnetic ordering (AFO) is exhibited along the easy and hard axis respectively in the closely packed network of dots [3]. The FO and AFO yields magnetostatic interaction between the dots leading to a minimum global energy state that defines a logical level. Previously an ML based majority gate was designed and computing energy and delay was studied [7]. In this paper, an ML based one bit and two bit full adder (FA) circuit is simulated and a stick diagram representation to offer quick footprint estimation is proposed. Stick diagram representation for an NML circuit is presented in a view to assist designers optimize circuit layout on a chip.

## DESIGN OF ML BASED FULL ADDER CIRCUIT

Full adder is the most utilized building block, often seen in multipliers, subtractors, and other datapath subsystems [8]. The ML based one bit full adder circuit is designed in an open source micromagnetic framework simulator *OOMMF* [9], developed by NIST, USA. Given a magnetic pattern, *OOMMF* determines the magnetization and spin direction in the structure by solving Landau-Lifshitz equation [10] stated in the equation 1, where M is pointwise magnetization (A/m), $\gamma$ is gyromagnetic ratio (m/(A.s)), $\alpha$ is the damping coefficient (dimensionless), and $H_{eff}$ is the pointwise effective field (A/m), defined as:

$$H_{eff} = -\mu_0^{-1}\frac{\partial(M)}{\partial M}$$

where $\mu_0$ is magnetic permeability in vacuum and E(M) is Landau-Lifshitz energy, which is given by
$E(M) = Eexchange(M) + Eanisotropy(M) + Eapplied(M) + Estray(M)$

$$\frac{dM}{dt} = -\gamma M \times H_{eff} - \frac{\gamma\alpha}{M_s} M \times \left(M \times H_{eff}\right) \qquad (1)$$

A default value of $2.21 \times 10^5$ was set for $\gamma$ in the simulator, with damping coefficient ($\alpha$) of 0.5 was configured. Permalloy ferromagnetic material was chosen to design the adder circuit due to its faster switching response and low demagnetizing energy property among the other materials [11]. The saturation magnetization, crystalline anisotropic constant, and exchange stiffness were set to $860 \times 10^3$ *A/m*, $13 \times 10^{-12}$ *J/m* and 0 $J/m^3$ respectively [11]. The solver uses exchange stiffness, and crystalline anisotropic constant to calculate exchange energy, and anisotropy energy for providing Landau-Lifshitz energy *E*(*M*) component. A steady state spin moments were evolved by the solver on reaching minimum energy induced individual pointwise magnetization in time domain. One bit and two bit full adder (FA) circuits were designed in *OOMMF* with dot spacing of 22 nm. One bit FA circuit comprised of two inputs ($A_0$, $B_0$), and a *carry-in* ($C_0$), to generate a sum ($S_0$) bit, and a carry out ($C_1$) bit. The rectangular cornered permalloy dots were designed for a size of 50 nm in width, 100 nm in length, and spacing of 22 nm. The aspect ratios of individual dots were chosen to aid in

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easy switching of the magnetic domains along easy axis [12]. The input dots were assymetrically designed with a slant magnets to reduce the footprint of the input dots, and effectively switch the domains of the nearby dots [13]. The slanted edge magnets have tilted energy landscape, as shown in Figure 1, influencing a shift in the energy barrier. In slant magnets, the energy barrier is not at maximum when the dot is magnetized along the horizontal direction, as in the case of the symmetric magnets [13], hence the domains settle to a minimum energy position after switching off the applied magnetic field, thereby achieving the same input logical state, when symmetric dots were designed.

Conventionally for one bit FA circuit, $S_0$ and $C_1$ bits are defined by EXOR and majority gate operations respectively [1]. Alternately, sum ( $S_0$ ) bit is recursively expressed as $S_0 = MAJ(MAJ(A_0, B_0, \bar{C}_0), \bar{C}_1, C_0)$, where majority gate operation is represented by the *MAJ* symbol. The carryout ($C_1$) bit is expressed as $C_1 = MAJ(A_0, B_0, C_0)$. The recursive representation of *Sum* bit allows to visualize higher order *n* bit adder subsystem in the form of majority (*MAJ*) blocks. One bit adder circuit generating $C_1$ and $S_0$ bits using magnetic logic based majority gate is shown in Figure 2. One bit adder circuit was designed in the *OOMMF* simulator and a transient analysis was completed till the domains in the individual magnetic dots were aligned to reach a global minimum energy state. The total energy dissipation and delay to evaluate a logical $S_0$ bit is 0.51 $\times 10^{-16}$ J and 6.50 ns respectively. Similarly, a two bit adder circuit was designed and simulated in *OOMMF* as shown in Figure 3. The energy dissipated and the computational delay to obtain a logical $S_1$ bit is 1.82 $\times 10^{-16}$ J and 16.68 ns respectively.

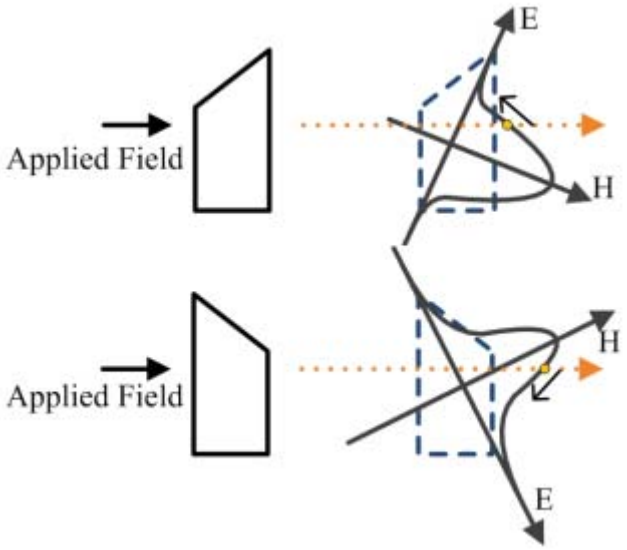


Fig. 1: Design of asymmetric slant nanomagnets, with energy landscape overlaid on the schematic.

## DEVELOPMENT OF STICK DIAGRAM MODELS

As shown in Figure 2, one bit FA circuit is realized with two primitive *MAJ* blocks to generate $C_1$ and output of $MAJ(A_0, B_0, \bar{C}_0)$ separately. The blocks are colored

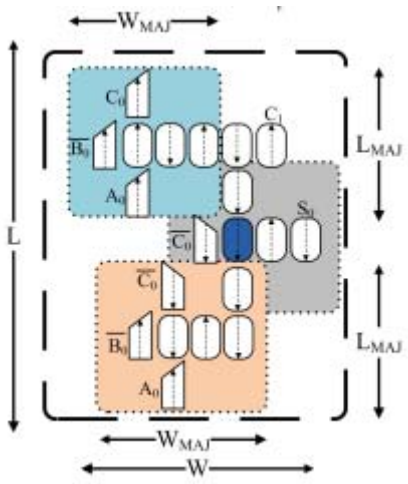


Fig. 2: Schematic representation of magnetic logic based one bit full adder circuit.

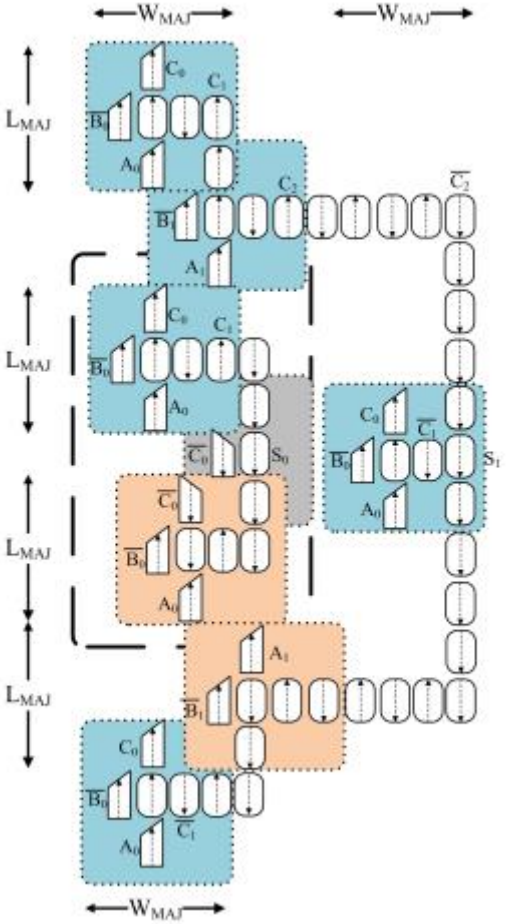


Fig. 3: Schematic representation of magnetic logic based two bit full adder circuit.

differently to indicate the logical change in inputs and thereby generating dissimilar outputs. The outputs of these two blocks are magnetically navigated to final *MAJ* block to generate $S_0$ bit. A two bit FA circuit generating $C_2$ and $S_1$ bits are shown in Figure 3. In addition, the two bit adder design included

three regenerate *MAJ* blocks producing $\bar{C}_1$, and $C_1$ bits separately, and three generate *MAJ* blocks for the 2nd bit operations with similar or compliment of $A_1$, $B_1$, and $C_1$ inputs. The regenerate *MAJ* blocks yields lower significant bits (LSB), which already existed elsewhere in the schematic. The three new regenerate *MAJ* blocks were designed to avoid the magnetic disturbances, observed in an otherwise long chain of coupled and highly branched network of ferromagnetic dots [3]. The number of *MAJ* blocks to design higher order *n* bit FA circuit is generalized to 3*n*+*Blocks*(*n*-1), where *n* is the number of adder bits, and *Blocks*(*n*-1) function is the number of *MAJ* blocks to realize *n* - 1 FA. The number of *MAJ* blocks in the dot level schematic which is summarized in Table I, is useful information to realize higher order FA subsystem.

A model to approximate the footprint of fast adder circuit is considered useful in planning and routing stage of a system design flow. The footprint of *n* bit FA circuit summarized in Table II, is given in terms of length ($L_{MAJ}$) and Width ($W_{MAJ}$) of primitive *MAJ* logic gate where $W_d$ represents width of a dot and spacing between the horizontally placed dots, and $L_d$ refers to the length of a dot and spacing between the vertically placed dots. $W_d$ is 72 nm and $L_d$ is 122 nm in our design. The overall footprint for higher order *n* bit adder block is modeled as ((2*n*-1) $W_{MAJ}$ - $W_d$)× ((2$^n$+2) $L_{MAJ}$ - $L_d$). Note that the primitive *MAJ* block occupies a footprint of $W_{MAJ} = 4W_d$, and $L_{MAJ} = 3L_d$. The footprint of ML based one bit adder circuit as shown in Figure 2, is expressed approximately as $(W_{MAJ} + W_d) \times (2L_{MAJ} + L_d)$, which is 0.30 $\mu m^2$. A 22 nm CMOS based one bit adder circuit occupies a footprint of approximately 17 $\mu m^2$ [8]. Although the readout circuitry is not involved in the proposed ML design, yet the overall footprint of ML based adder circuit will be significantly low. The proposed stick diagram in NML simplifies the dot level schematic and provides additional mask layer information to pattern the dots for subsystem. For NML, the stick diagram is represented by horizontal and vertical lines, where the horizontal line indicates AFO nature, and vertical line exhibits FO behavior among the placed dots. The electrically isolated dots, are magnetically coupled, hence a line in a stick diagram indicates coupling between the dots placed either horizontally or vertically. Lines of same color suggest that the designed AFO or FO behavior among the series of dots is confined to a plane. The stick diagram representation for two bit adder circuit, which primarily includes the *MAJ* block, is represented by two orthogonal intersecting lines indicating the placement of dots along hard and easy axis. The output logic is generated in the nonmagnetic dot denoted by the center of the intersecting orthogonal stick lines. In a conservative approach to design circuit layout, the spacing between two horizontal lines of same color is designed to be at least $5L_d$ for collinear vertical inputs, otherwise the spacing is suggested to be at least $3L_d$. Similarly the desired spacing between two vertical lines of same color is designed to be at least $5W_d$ for collinear inputs, and $3Wd$ for non-collinear inputs. A stick diagram representation of two bit FA circuit

**TABLE I:** Number of generate and regenerate majority blocks to represent *n* bit adder.

| *n* bit Adder | Generate | Regenerate | Total blocks |
|---|---|---|---|
| 1 bit | 3 | 0 | 3 |
| 2 bit | 3 | 3 | 6+Blocks(1 bit) = 9 |
| 3 bit | 3 | 6 | 9+Blocks(2 bit) = 18 |
| *n* bit | 3 | 3(*n*-1) | 3 + Blocks (*n*-1) |

**TABLE II:** Footprint of the *n* bit fast adder circuit.

| n bit Adder | Width | Length |
|---|---|---|
| 1 bit | $W_{MAJ} + W_d$ | $2L_{MAJ} + L_d$ |
| 2 bit | $3W_{MAJ} - W_d$ | $6L_{MAJ} - L_d$ |
| 3 bit | $5W_{MAJ} - W_d$ | $10L_{MAJ} - L_d$ |
| *n* > 1 | $(2n-1)W_{MAJ} - W_d$ | $(2^n + 2)L_{MAJ} - L_d$ |

derived from the dot level schematic is presented in Figure 4. The *MAJ* blocks shown in the dot level schematic is substituted by intersecting orthogonal lines in the stick diagram representation. A quick footprint estimation model following one bit, and two bit FA circuit is expressed as $(2+N_H + 2\sum_{i=1}^{n} i) \times W_d \times (9+N_V + 5\sum_{j=1}^{n} j - 1)$, where $N_V$, and $N_H$ are the number of intersections in the vertical and horizontal collinear input lines that has the highest number of intersections respectively and *n* is the number of bits in FA circuit. Based on the stick diagram representation for 1 bit and 2 bit FA subsystem, a peripheral outline with signal generation and propagation sketch for *n* bit FA subsystem is shown in the Figure 5. The box shown in black dotted lines signifies the designed footprint occupied by the higher order *n* bit subsystem.

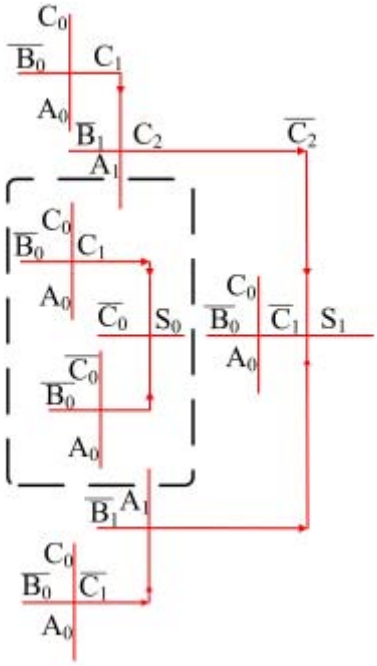


Fig. 4: Stick diagram representation of 1 bit and 2 bit full adder circuits.

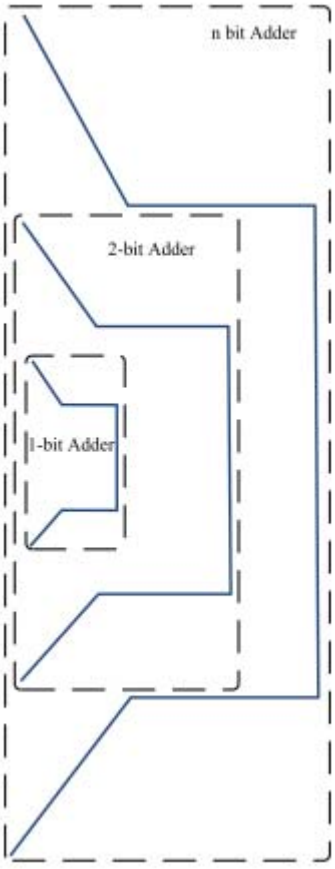


Fig. 5: Schematic representation of logic generation for n bit full adder subsystem.

## CONCLUSIONS

An NML based one bit and two bit FA subsystem was designed and simulated in micromagnetic simulator. The number of majority blocks designed in the higher order *n* bit adder subsystem was extended to approximate footprint of the circuit in terms of length and width of a majority gate. A stick diagram model was derived from the majority gate model and quick footprint approximation was estimated to design combinatorial subsystem. A footprint model to accommodate *n* bit adder subsystem was suggested to simplify planning and routing stage in the overall system design. A logic generation and propagation model specifically for designing higher order *n* bit adder subsystem was designed to share the topographical and logic propagation information of the design. The stick diagram representation is suggested to offer quick footprint approximation for NML subsystems, which is seen as a technology for non-real time and ultra low power applications.

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