A Design of Complex Impedance Meter

A Design Project Report

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by

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Abstract

Master of Electrical Engineering Program

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Design Project Report

Project Title: A Design of Complex Impedance Meter

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Abstract:

The Complex Impedance Meter presented in this report is a high precision, low power consumption impedance conversion system which provides programmable frequency sweep and tuning capability for impedance measurement from 5kΩ to 1.1MΩ with system accuracy of 2%. The system is built with an AVR microcontroller ATmega32, an Analog Device network analyzer AD5933, two analog multiplexers ADG706, a CTS low jitter clock oscillator MXO45HS, two accurate resistor networks with designed resistance values and a liquid crystal display RCM2034R. It allows an unknown external impedance to be excited with a known frequency. The response signal from the impedance is sampled by the on board ADC, and the DFT is processed by a DSP engine which returns a real and imaginary data word at each excitation frequency. The magnitude of these data words is further scaled by calibrated Gain Factor in order to return the actual impedance value. The prototype of the system is implemented and system calibration is done to improve the overall accuracy.

Report Approved by
Project Advisor: Date:

Executive Summary

A prototype of the Complex Impedance Meter is designed and implemented. The system is a microcontroller based, high precision and low power device. Due to the simple structure, it can be made as a portable impedance measurement device, which is used in a lot of scientific and industrial fields such as electrochemical analysis, bioelectrical impedance analysis and material property analysis. The accuracy of 2% is realized through the appropriate design and system calibration. This accuracy is good enough for most of the biomedical impedance measurement applications.

The system has been designed as an intelligent and friendly device, which does not need any adjustment or configuration before a measure. The maximum system response time is 0.5 second, which means in the worst case users can read the measured impedance on the LCD within half a second. If the impedance being measured is out of range, it will also give a message on the display indicating the error. The hardware design was implemented on several prototype boards. The values of the precision resistance were carefully calculated and chosen so that good linearity and measurable range (5kΩ to 1.1MΩ) can be achieved. Operating software was designed and implemented to realize the intelligence and easy-to-use features. The design trades off the maximum system response time with the intelligence and keeps a good balance between these two specs. Finally calibration was carried out and two methods were used to further improve the linearity of the system.

Introduction

From biological cell analysis to fuel cell tests, from coatings to cement paste quality control, Complex Impedance Measurement (CIM) has become a powerful tool in the vast environment of those applications. The basic principle of CIM is modeling the unit under test (UUT) in a combination of electrical components, applying small amplitude of AC voltage or current to the ends of UUT, over the frequency band of interest. For each frequency in the range, the measured impedance is usually a complex ratio between the input and output signal.

In the design presented in this report, this principle is adopted into the architecture of the system. As Figure 1 shows, the on board frequency generator generates stimulus signal with known frequencies. The external unknown resistor is connected between the input and output ports. The response current from the impedance is converted into voltage by a trans-impedance amplifier. The output voltage of this amplifier is sampled by an on board ADC and the DFT is processed by a DSP engine at each excitation frequency. The real and imaginary results from the DSP are further processed by the microcontroller. They are compared with the results obtained from a known precise resistance using the same configuration on the signal path. The actual impedance value can be calculated from the known resistance together with the above measured results.

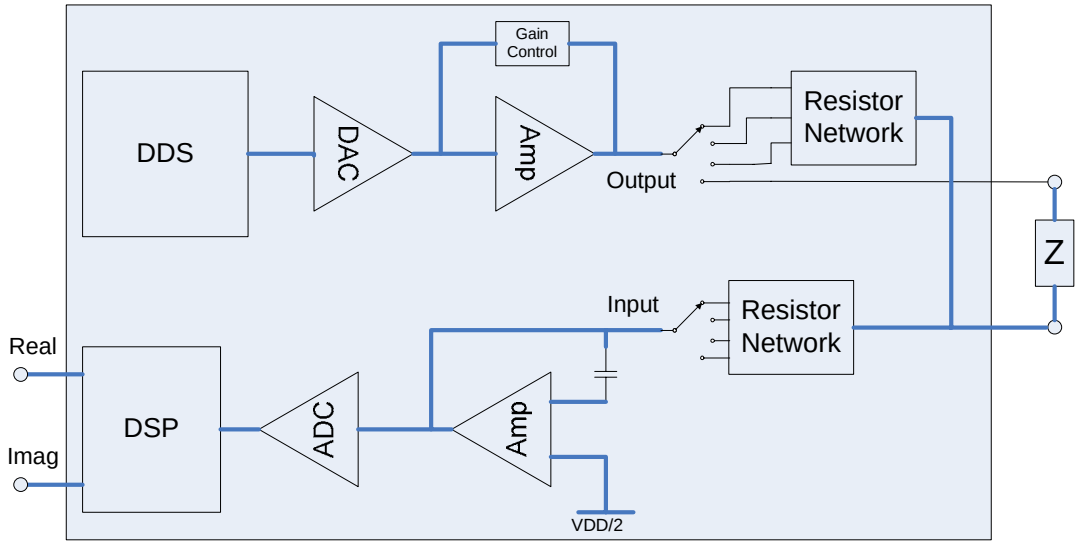

Fig.1 System Block Diagram

The Principle of Measurement

The basic measurement method of AD5933 is calibration and comparison. As the signal path shown in Figure 2, V_{OUT}, the output of the signal generator, can be modeled as a voltage source. The unknown impedance is connected between V_{OUT} and V_{IN}. V_{IN} is biased at VDD/2 causing the AC current through $Z_{unknown}$ and R_{FB} to be equal to $V_{OUT}/ Z_{unknown}$. If V_{OUT}, R_{FB} and the gain along the signal path is known, the unknown impedance can be calculated by sampling and processing the voltage at the output of low pass filter.

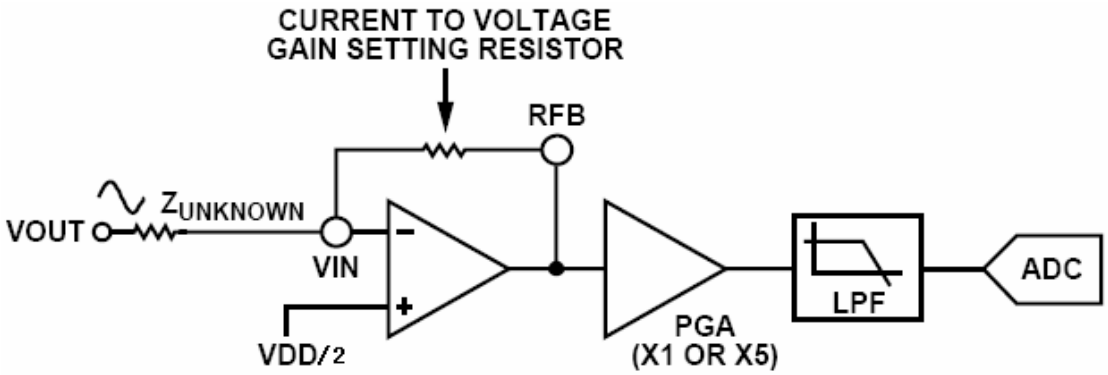

Fig. 2 AD5933 Signal Path

For accurate measure of the impedance, it is important that the receive stage is operating in its linear region. This requires careful selection of the excitation signal range, current-to-voltage gain resistor, and PGA gain. The gain through the system shown in Figure 2 is given by

$$SystemGain = OutputExcitationVoltageRange \times \frac{GainSetting\ \mathrm{Re}\,sistor}{Z_{Unknown}} \times PGAGain$$

---------- (1)

There are two issues related to the signal saturation problem. First, current from the external unknown impedance flows through the V_{IN} pin and into a trans-impedance amplifier which has a user determined external resistor across its feedback path. The output voltage of the trans-impedance amplifier is determined by the closed loop gain $-R_{FB}/Z_{unknown}$ and V_{OUT}. The positive node of the amplifier is biased at a fixed value of VDD/2, large difference between the positive and negative nodes can saturate the output the amplifier. The R_{FB} and the V_{OUT} should be chosen so that this voltage remains in the linear region. Second, the gain of the PGA should be properly set to make best use of the dynamic range of the ADC but not to saturate the following stages. Both of these issues rely on an approximation of the $Z_{unknown}$ and proper selection on the feedback resistor.

As the datasheet of AD5933 suggests, to get best accuracy, the $R_{FB}/Z_{unknown}$ ratio should be within 0.066~0.2. The resistance values of the feedback network are determined as 4.7k, 10k, 27k, 57k, 200k, 470k, 1M. The measurable impedance range is then divided into 7 segments. One of the values is picked after the range of the unknown impedance is estimated. The way to estimate the unknown impedance is discussed in the software design part.

System Design

The microcontroller is the control unit and data processor in the system. It controls the AD5933 and two analog switches during the measures. After calculation and calibration based on the data from AD5933, the microcontroller sends the results to the LCD, where users can read the impedance values.

The hardware connections between the microcontroller and the functional chips are shown below.

Name	Connection Type	Line numbers	Description
AD5933	I^2C	2	AD5933 control and data transfer
ADG706 (1)	Parallel	4	Feedback resistor selection
ADG706 (2)	Parallel	4	Calibration resistor selection
RCM2034R	Parallel	7	LCD control and data transfer

Table.1 Intrasystem Connection

The microcontroller used in this project has four 8-bit I/O ports. All I/O pins are shared with alternate function pins. By setting the I/O ports to a proper status, they can be used as either general digital I/O or I/O pins of functional blocks in ATmaga32.

I^2C bus

I^2C bus is a Serial Interface Protocol. The AD5933 is connected to this bus as a slave device, under the control of a master device, which is the ATmega32 here. The AD5933 has a 7-bit serial bus slave address. When the device is powered up, it will do so with a default serial bus address, 0001101.

Figure 3 shows the timing diagram for general read and write operations using the I^2C interface.

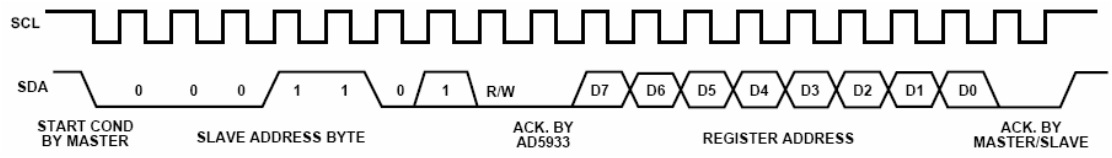

Fig. 3 General I^2C protocol

The master initiates data transfer by establishing a start condition, defined as a high to low transition on the serial data line (SDA) while the serial clock line (SCL) remains high. This indicates that a data stream follows. The slave responds to the start condition and shifts in the next 8 bits, consisting of a 7-bit slave address (MSB first) plus an R/W bit, which determines the direction of the data transfer. That is, whether data is written to or read from the slave device (0 = write, 1 = read).

The slave responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/W bit is 0, then the master writes to the slave device. If the R/W bit is 1, the master reads from the slave device.

Data is sent over the serial bus in sequences of nine clock pulses, 8 bits of data followed by an acknowledge bit, which can be from the master or slave device. If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction telling the slave device to expect a block write, or it may be a register address that tells the slave where subsequent data is to be written. Data can flow in only one direction as defined by the R/W bit.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device releases the SDA line during the low period before the ninth clock pulse, but the slave device does not pull it low. This is known as a no acknowledge (NACK). The master then takes the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a stop condition.

LCD connection and control

The RCM2034R is a reflective TN type liquid crystal module with a built-in controller / driver LSI and a display capacity of 16 characters with 2 lines. It supports both 4-bit and 8-bit operations. That is, data transfer with two transmissions of 4 bits at a time or one transmission of 8 bits at once. When using 4-bit operation mode, data is transferred along DB4 through DB7 buses and DB0 through DB3 buses are not used. (DB0-DB7 is the bi-directional data bus on RCM2034R.) Data transfer is completed after two transfers of 4 bit data. First the upper nibble (contents of DB4 through DB7 during 8-bit interfacing) is transferred and then the lower nibble

(contents of DB0 through DB3 during 8-bit interfacing) is transferred.

The 4-bit operation mode is used in this system so that a single 8-bit port connection is enough for this operation mode. Besides 4-bit data bus, three control lines need to be connected to complete the hardware connection between the microcontroller and the LCD. Table-2 shows the connection details and their functions.

Symbol	Input/output	Function	MCU Connection
RS	Input	Register selection signal.	PD0
R/W	Input	Reading and writing selection signal	PD1
E	Input	Data reading and writing start signal	PD2
DB4-DB7	Input/output	4-bit operation data bus	PD4-PD7

Table.2 LCD Connection

Analog Switches control

The ADG706 is a low-voltage, CMOS analog multiplexers comprising 16 single channels. The ADG706 switches one of 16 inputs (S1–S16) to a common output, D, as determined by the 4-bit binary address lines A0, A1, A2, and A3. An EN input is used to enable or disable the device. When disabled, all channels are switched off. An 8-bit parallel port is just good for two switches with both of the EN inputs are tied to VCC. They are used to switch the resistor networks between V_{OUT}, V_{IN} and R_{FB}. The common terminals of these two switches are connected to V_{OUT} and V_{IN} respectively. The reference resistors are connected together to R_{FB} on one end while the other ends are connected to different inputs on the switch. Similarly, the calibration resistors are connected together to V_{IN} on one side. Figure 4 shows the connection of the resistor networks and switches.

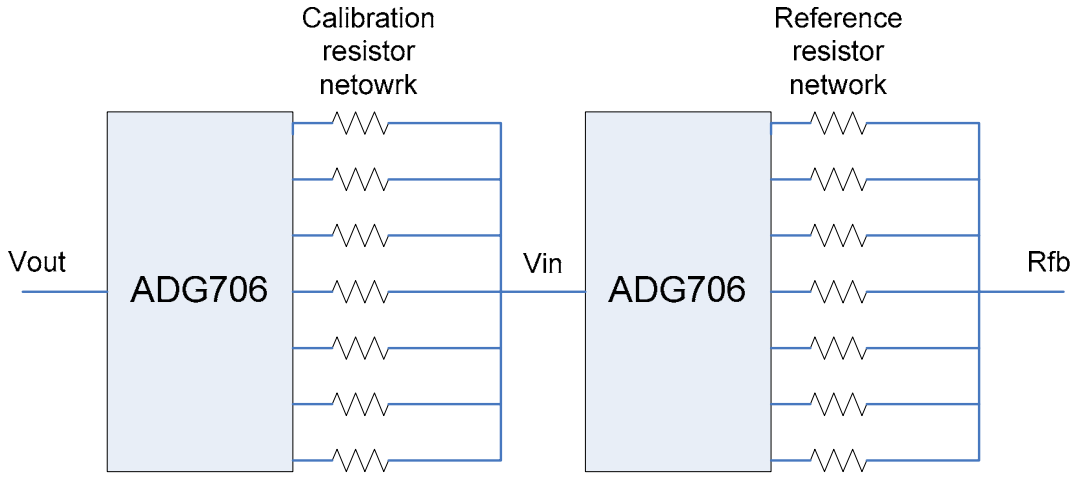

Fig. 4 Precision resistor networks

Crystal Oscillator

The frequency generator in AD5933 is based on DDS technique. There are two choices to get the reference frequency. The AD5933 has an on chip RC oscillator, which has an output frequency of 16.7MHz±0.2 MHz with a 330ppm jitter spec. Relatively high phase noise of this internal oscillator can seriously affect the output stimulus signal, thus the accuracy of the measured impedance because all the following calculation is based on the nominal output frequency. The other choice is using an external clock to feed the 16.6MHz reference. A crystal oscillator with high stability of 50ppm is used. Though it consumes extra power, the frequency accuracy of the output signal can be greatly improved.

Software design

I^2C bus

Since the commands and data bytes between microcontroller and AD5933 are transferred through I^2C bus, it is necessary to establish a function library containing all the read and write functions for the communication before applying high level application commands. In this design, the function library is divided into two levels. As shown in Figure 5, the low level functions complete the basic operations including register setting, reading and writing. The high level functions are based on the low level one. They use these basic register operations, as well as appropriate timing and protocol of AD5933, to complete all the communication operations AD5933 supports. Those functions include byte writing/reading, block writing/reading, address point setting. They are the routines called by the application level.

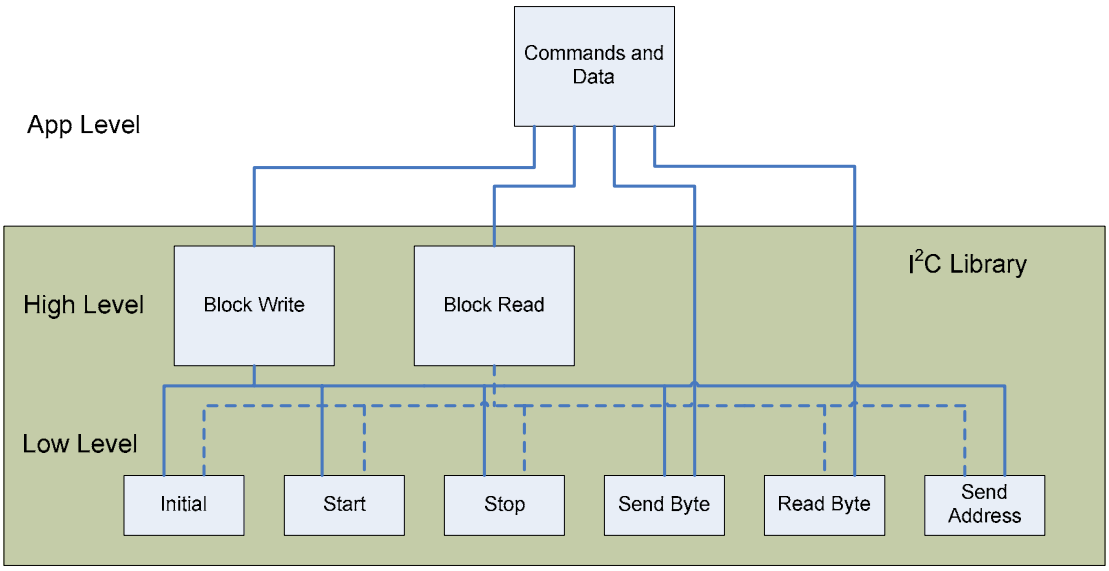

Fig. 5 I^2C bus function library

LCD display

There are existing functions for LCD control in ATmage32 function library. But most of them are low level functions which can only complete such tasks as putting one

character on the screen, move the cursor to certain point or clear the screen. Higher level functions are needed to bridge the low level to the application level. Since the only information that needs to be shown on the screen are the current testing frequency and the measured impedance, the format of the displayed words are similar. A function with two inputs, the frequency and impedance, is written as the interface to the application level. After every measurement, the application program calls this function to output the measured results.

Estimate the unknown impedance

The AD5933 is capable of measuring impedance values by providing the real (R) and imaginary (I) code. The magnitude of the real and imaginary data contents is given by $Magnitude(f) = \sqrt{R^2 + I^2}$. This magnitude value is equal to a scaled value of the actual impedance under test at the frequency point f. In order to determine actual impedance value users must multiply the magnitude by a number called Gain Factor GF(freq, Vdd, temp), which is a value representing the accumulative gain through the signal path of the system for known calibration impedance for a specified value of output gain voltage/pre ADC gain and feedback resistor settings. Therefore the actual impedance at any sample instance is given by the following,

$$\text{Im}\, pedance(f) = GainFactor \times Magnitude(f)$$

The Gain Factor is measured using a known external impedance, e.g., a precision resistor, connected between Vout and Vin as close as possible to the pins. Calculating the GF in this way calibrates out the parasitic impedance between Vout and Vin at a given frequency. The parasitic impedance is made up of a parallel capacitance between Vout and Vin as well as a series resistance and series inductance mainly due to the bond wires and solder joints.

As there are several gain settings on the signal path, any adjustment to the supply voltage, calibration frequency, output excitation level, external feedback resistance value, and pre-ADC voltage gain will require a recalculation of the GF. If the GF is not recalculated after any system gain parameter adjustment then the impedance value returned by the AD5933 will have an error associated with it. Therefore the accuracy of final results depends upon the value of the GF.

The gain factor is dependant upon the ratio of the trans-impedance feedback resistance value R_{FB} to the impedance under test, $Z_{unknown}$. In order for the AD5933 to return accurate values, it is necessary to ensure that the largest signal is returned to the ADC while ensuring that gain factor will not vary significantly over the unknown impedance range. Minimising the gain factor variation is achieved by placing the AD5933 operating point in the flat region the variation of the gain factor. The ratio of feedback resistance to calibration impedance should lie in the range of 0.2~0.066, recommended in the data sheet.

These two values are chosen based on the knowledge of the range of unknown impedance. A straightforward and good way to estimate the unknown impedance is trial and error. Figure 6 shows the impedance estimation flow diagram. The estimation starts from the middle of the measurable impedance range, e.g., 27kΩ-57kΩ. The feedback resistor corresponding to this impedance range is chosen. Then the magnitude code of this unknown impedance under this feedback situation can be obtained. Compare this value with the upper and lower limit of the magnitude codes, which are the boundary values for the input signal staying in the linear range. If the measured value is not within the limits, the estimation process will stay in the loop and go through the steps discussed above again with a changed impedance range/feedback resistor. When the magnitude is larger than the upper limit, the next larger resistor will be chosen. When smaller, the next smaller resistor will be chosen. The loop will keep running until it finds a proper feedback resistor which makes the magnitude code within the limits or the unknown impedance is out of range. In either way, the loop stops. The magnitude code is recorded as one of the outputs of the loop when the impedance range is found while an error routine is called when it is out of range.

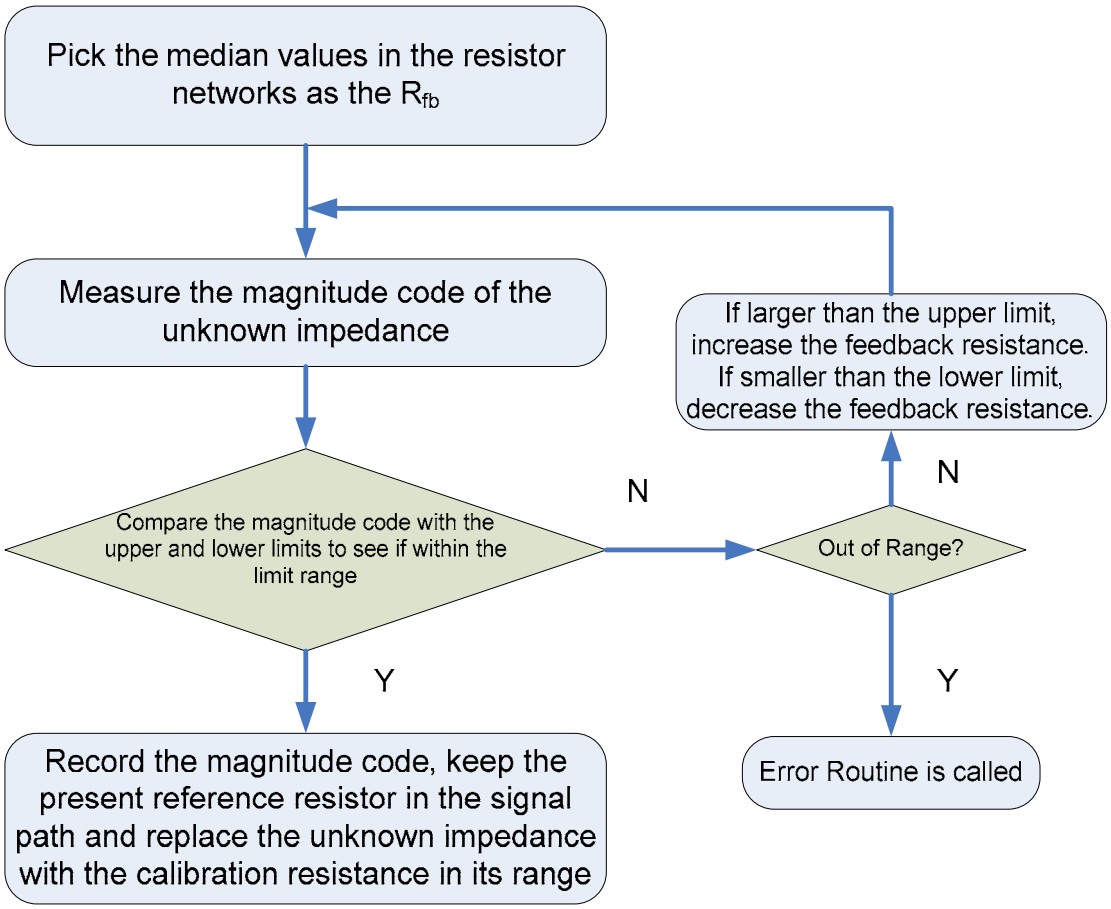

Fig. 6 Impedance Estimation Flow Diagram

Words define

Since both the operation of I^2C bus and control of AD5933 have lots of command and status words, it is convenient for use by defining those hex numbers to more meaningful constants. Similarly, all the register addresses in AD5933 are defined in the same way.

System test and calibration

The prototype of system is implemented with resistor networks consisting of high precision resistor (0.5%). Since these resistors are only accurate under low frequency, the test and calibration is conducted within its precision range. According to the discussion above, a proper feedback and calibration resistor should be chosen so as to get the best measurement accuracy. However, even if the case, the measurement results may not be within the accuracy range of 2%. An important assumption of the measurement is that the gain factor within one of those defined impedance ranges is constant. That is, the magnitude code is simply a linear function of the impedance. But the real situation is that the magnitude code becomes non-linear gradually as the unknown impedance approaches the boundaries of the defined impedance range. If the magnitude code of the calibration impedance is still used as a reference for such cases, results are not accurate. Figure 7 shows the linearity of magnitude code from 33KΩ to 72KΩ. It can be seen that if the unknown impedance is located in the lower part of this impedance range, the results may have large errors due to the non-linearity.

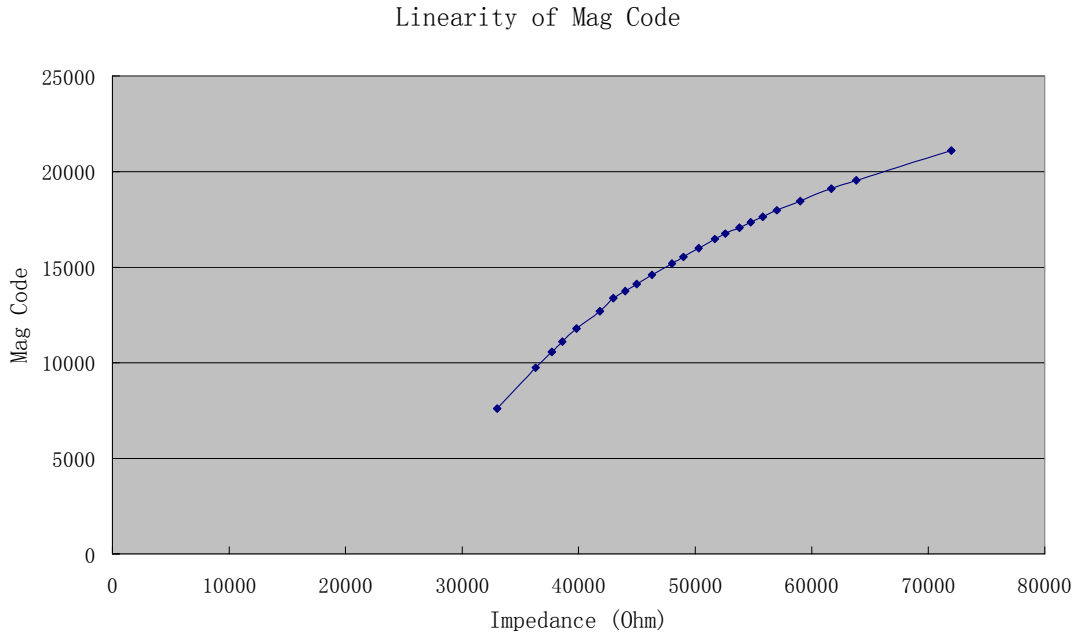

Fig. 7 Linearity of magnitude code

There are two ways to decrease the effect of this phenomenon. The first is to divide

the impedance range into more sections. It is easy to see that if we can divide the impedance range shown in Figure 7 into 3 sections, 33K~45K~56K~72K, each of which is much more linear inside the range. However the cost of this way is to complicate the resistor networks, thus the whole system and more important, the measurement speed will be greatly lowered because of the nature of the impedance estimation method. In the worst case, the measurement time increases by three times as one impedance range is divided into three. The second way is to take advantage of the feature of signal path gain control on AD5933 to linearize the system. Since the magnitude code has linear relation to the gain through the system and the gain can be expressed as (1), changing the magnitude of output signal and/or the gain of the preamplifier has the same effect of changing the value of feedback resistor (gain setting resistor) on the magnitude code. So we can use two adjacent values of the feedback resistors (one in the impedance range where the unknown impedance located and the other in the adjacent range) to cover the same impedance range. Since the feedback resistors used in these two measurements are different, two different linearity curves can be obtained, which can be used to linearize the magnitude code to the desirable linearity. This needs to completely plot the linearity curves for all the impedance ranges and finely tune the parameters to get the best combination of these two linearity curves. But all these work can be done in the design stage. So it will not affect the measurement time during the use. The final design of this project adopted both of the two ways and the slowest measurement takes 0.5 second, which occurs in very low frequency range. Figure 8 shows the system linearity of the final design for the whole measurement range. The linearity can be calculated as

$$Linearity = \frac{Largest DeviationFromTheIdealCurve}{TheFullMeasurementRange} = \frac{21K\Omega}{1100 - 5K\Omega} = 1.9\%$$

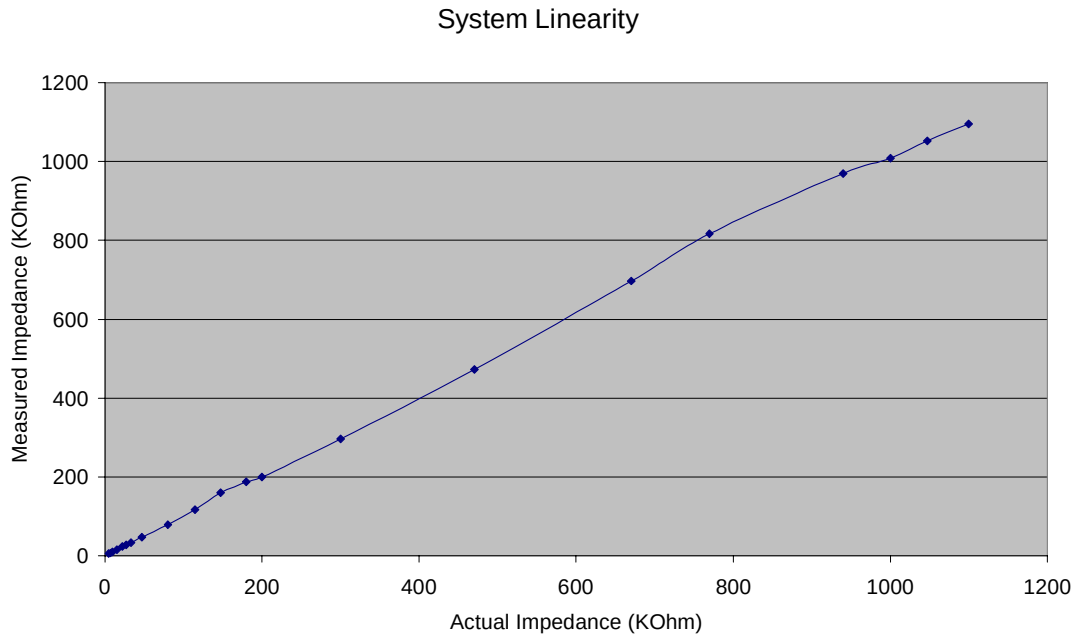

Fig. 8 System Linearity

Conclusions and Future work

A prototype of complex impedance meter is designed and implemented. The system is a microcontroller based, high precision and low power device. Due to the simple structure, it can be made as a portable impedance measurement device, which is used in a lot of scientific and industrial fields such as electrochemical analysis, bioelectrical impedance analysis and material property analysis. The accuracy of 2% is realized through the appropriate design and system calibration. This accuracy is good enough for most of the biomedical impedance measurement applications.

Due to the limitation of the precision resistor networks used in the system, the accuracy is only proved in relatively low frequency. For the next step, frequency independent high precision resistors can be adopted and the system needs recalibrated for the best results. The second thing for the future work is the prototype can be further implemented on a PCB board to achieve less parasitic parameters and low noise. This may further increase the accuracy of the measurement.

Acknowledge

Designing a measurement device begins with a great deal of excitement. However, during the system design, chip ordering and implementation many unexpected issues need to be studied and solved. I got the initial idea and successfully completed this project under the guidance of Mr. Bruce Land. It is only appropriate that I express my best appreciation to him here. During the design work, I obtained quite a few valuable advice and suggestion from Mr. Land. What's more, he provided me lots of electrical components which were not easy to get by myself. This greatly facilitated the design progress and finally helped me complete a good job.

Reference

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