# INTEGRATED CIRCUITS

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

# **74HC/HCT42**BCD to decimal decoder (1-of-10)

Product specification
File under Integrated Circuits, IC06

December 1990





# BCD to decimal decoder (1-of-10)

# **74HC/HCT42**

### **FEATURES**

- · Mutually exclusive outputs
- 1-of-8 demultiplexing capability
- · Outputs disabled for input codes above nine
- · Output capability: standard
- I<sub>CC</sub> category: MSI

## **GENERAL DESCRIPTION**

The 74HC/HCT42 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT42 decoders accept four active HIGH BCD inputs and provide 10 mutually exclusive active LOW outputs. The active LOW outputs facilitate addressing other MSI circuits with active LOW input enables.

The logic design of the "42" ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input  $(A_3)$  produces an useful inhibit function when the "42" is used as a 1-of-8 decoder. The  $A_3$  input can also be used as the data input in an 8-output demultiplexer application.

## **QUICK REFERENCE DATA**

GND = 0 V;  $T_{amb} = 25 \, ^{\circ}C$ ;  $t_r = t_f = 6 \, \text{ns}$ 

SYMBOL	PARAMETER	CONDITIONS	TYP	UNIT	
STWIBOL	PARAIVIETER	CONDITIONS	нс	нст	ONL
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $A_n$ to $\overline{Y}_n$	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	14	17	ns
Cı	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per package	notes 1 and 2	37	37	pF

## **Notes**

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

 $f_i$  = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs}$ 

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is  $V_I$  = GND to  $V_{CC}$ For HCT the condition is  $V_I$  = GND to  $V_{CC}$  – 1.5 V

### ORDERING INFORMATION

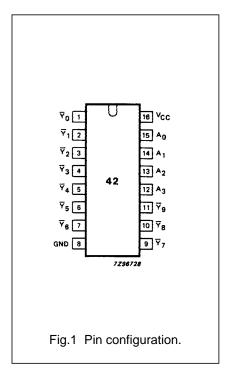
See "74HC/HCT/HCU/HCMOS Logic Package Information".

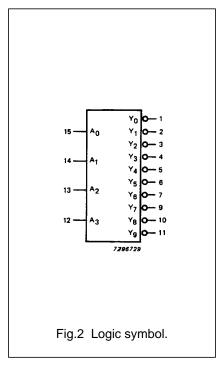
# BCD to decimal decoder (1-of-10)

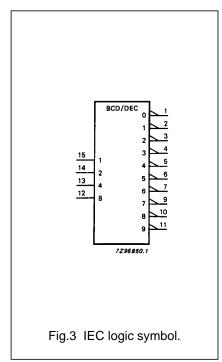
# 74HC/HCT42

# **PIN DESCRIPTION**

PIN NO.	SYMBOL	NAME AND FUNCTION				
1, 2, 3, 4, 5, 6, 7, 9, 10, 11	$\overline{Y}_0$ to $\overline{Y}_9$	multiplexer outputs				
8	GND	ground (0 V)				
15, 14, 13, 12	A <sub>0</sub> to A <sub>3</sub>	data inputs				
16	V <sub>CC</sub>	positive supply voltage				



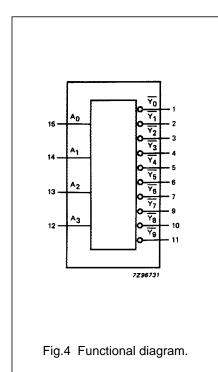




Philips Semiconductors Product specification

# BCD to decimal decoder (1-of-10)

# 74HC/HCT42

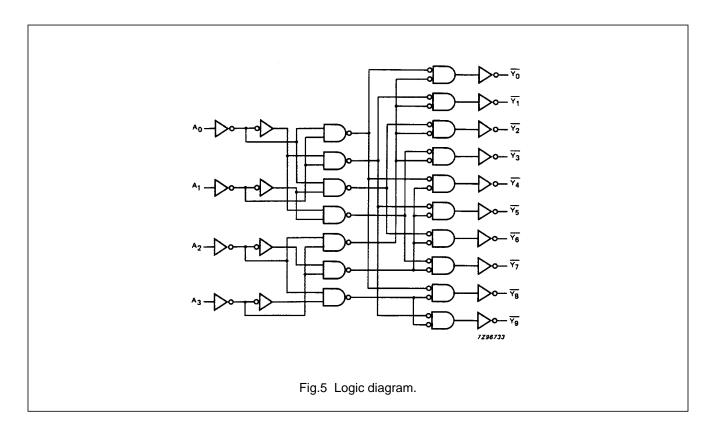


# **FUNCTION TABLE**

	INP	UTS		OUTPUTS										
<b>A</b> <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	<b>Y</b> <sub>5</sub>	₹ <sub>6</sub>	<b>Y</b> <sub>7</sub>	₹ <sub>8</sub>	₹ <sub>9</sub>	
L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	
L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	
L	L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	
L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	Н	
L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н	Н	Н	
L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	Н	
L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н	Н	
L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	Н	
Н	L	L	L	Н	Н	Н	Н	Н	Н	Н	Н	L	Н	
Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L	
Н	L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	
Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	
Н	Н	L	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	
Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	
Н	Н	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	
Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	

## Note

H = HIGH voltage level
 L = LOW voltage level



# BCD to decimal decoder (1-of-10)

74HC/HCT42

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## **AC CHARACTERISTICS FOR 74HC**

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS	
											WAVEFORMS
		+25		-40 to +85		-40 to +125		UNIT	V <sub>CC</sub> (V)	WAVEFORING	
		min.	typ.	max.	min.	max.	min.	max.		( ,	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay		47	150		190		225	ns	2.0	Fig.6
	$A_n$ to $\overline{Y}_n$		17	30		38		45		4.5	
			14	26		33		38		6.0	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19	75		95		110	ns	2.0	Fig.6
			7	15		19		22		4.5	
			6	13		16		19		6.0	

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

 $I_{CC}$  category: MSI

# Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A <sub>n</sub>	1.0

# **AC CHARACTERISTICS FOR 74HCT**

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$ 

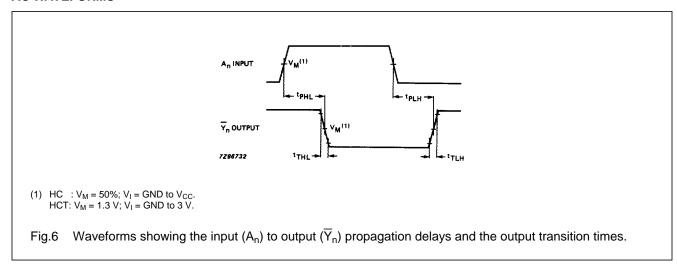
	PARAMETER	T <sub>amb</sub> (°C)								TEST CONDITIONS		
SYMBOL		74HCT									WAVEFORMS	
		+25			-40 to +85		-40 to +125		UNIT	V <sub>CC</sub>	WAVEFORING	
		min.	typ.	max.	min.	max.	min.	max.		(		
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay $A_n$ to $\overline{Y}_n$		20	35		44		53	ns	4.5	Fig.6	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6	

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# BCD to decimal decoder (1-of-10)

# 74HC/HCT42

# **AC WAVEFORMS**



# **PACKAGE OUTLINES**

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".