Design of Lower Power 4×10Gb/s VCSEL Driver Array

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Abstract-A 4-channel Vertical Cavity Surface Emitting Laser (VCSEL) driver array is designed in a 0.18μm CMOS technology. Simulated results show that each channel works at 10Gb/s (12.5Gb/s max) under a supply voltage of 1.8 V. Thus, aggregated total capacity of 40 Gb/s can be obtained from 4 channels. The power dissipation of each channel is only 50mW. To decrease the fall time of the output waveform, C^3A (Capacitively Coupled Current Amplifier) technique [1]is exploited. The VCSEL driver can be used in optical inter-connections between high speed chips.

I. INTRODUCTION

Recently, development of VLSI technology has increased the capability of data processing and the clock rates of integrated circuit and system operating. The transmitted data suffers from signal decay and the distribution of the clock signal generates clock skew which are bottlenecks of high speed systems. Some digital systems are limited by the data throughput limits of conventional interconnect. Future increased data rates will eventually make conventional electrical interconnect methods impractical. Optical interconnects, with speed potential into Terabits/s, are expected to be one of the best solutions to overcome the bottleneck in bandwidth, transmission length, and electromagnetic interference in conventional metallic transmission media. Also, characteristics such as low crosstalk, low-loss, and low distortion make parallel optical interconnects well suited to very short reach (VSR) applications such as chip-to-chip or board-to-board interconnection[2].

Vertical cavity surface emitting lasers (VCSELs) offer great advantages over conventional edge emitting lasers, such as extremely low threshold current, single longitudinal mode, especially surface emission laser with very small beam divergence and simple fabrication, which makes VCSELs very well suited for high density parallel optical interconnects. Also, due to the cost consideration, VCSEL diodes are now widely used.

MANY researchers and engineers implemented VCSEL drivers for data rates above 10-Gb/s using SiGe BiCMOS process[3] or using □-□compound semiconductor that provides high bandwidth and good quality passive components such as GaAs and InP. However, in low-cost and high volume short-haul applications at data rates of around 10 Gbps (such as LAN, MAN, and board-to-board interconnection), there has been an increasing interest in commercial CMOS technology for implementing the VCSEL driver. Because CMOS technology has unique advantages such as low power and low cost of fabrication, it is the result of high yield and a high degree of integration. Therefore, the object of this paper is to investigate the possibility of implementing a high-speed CMOS VCSEL driver for these cost sensitive applications[4-5].

In this paper, design and implementation of a high speed low power 4 x 10-Gb/s CMOS VCSEL driver array is reported.

II. DESIGN DETAILS

Fig. 1 shows the entire block diagram of a VCSEL driver. Each channel incorporates two pre-amplifiers and a main driver. The pre-amplifiers are cascaded to boost high frequency gain, while the first pre-amplifier has LVDS/CML compatible input configuration by adding center-tap control voltage (VT).

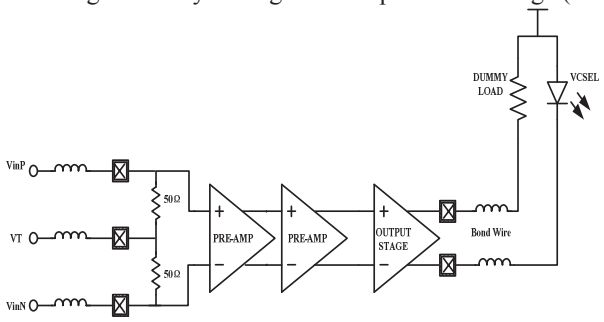

Figure 1. Block Diagram of VCSEL Driver

A. *Architecture of the VCSEL driver*

In this design, we implement the circuit with all the four channels keeping the same architecture. In each channel, fully differential amplifier is proposed to amplify the high speed input signal to a certain amplitude in order to drive the output stage.

B. *implementation of pre-amplifier*

Due to large modulation current of the VCSEL driver, the differential MOS pair of the output stage will possess large width and thus large parasitic capacitance for the pre-amplifier，which poses a big challenge for us to design very high speed driver.

There have been several traditional ways to reduce the impact of parasitic capacitance and to enhance the bandwidth

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of the pre-amplifier. As Fig. 2 shows, source followers are used as loads of the differential amplifiers. On the one hand, it lowers the central voltage of the output signals to a certain degree, on the other hand, it reduces the output resistance of the previous stage and thus enhances the bandwidth.

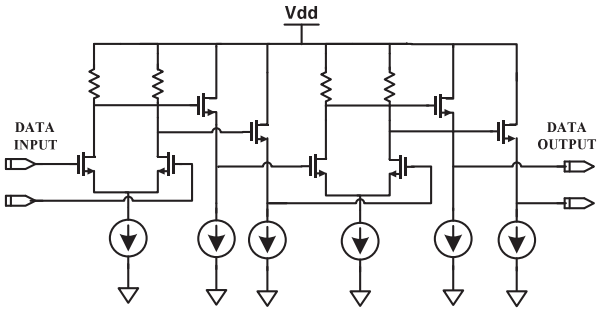

Figure 2. using source followers to enhance bandwidth

Another way to cancel the impact of the parasitic capacitance from next stage, as is shown in Fig. 3, is to connect a passive inductance in series with load resistance. This method is known as shunt peaking technique.

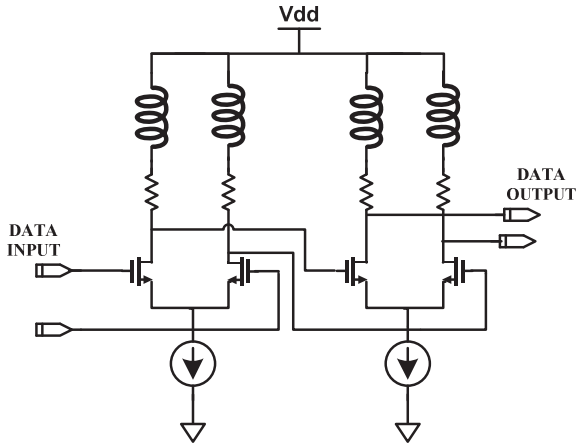

Figure 3. using shunt-peaking to enhance bandwidth

However, methods mentioned above are not appropriate for our design due to following reasons. First of all, in order to keep source followers working at saturate region all the time, the minimum output voltage of the differential amplifier should be 2Vth+3Vov, which is a large value for our 1.8V supply voltage, thus the output voltage swing of the pre-amplifier will be considerably impaired. Secondly, the channel width of our chip should be 250μm to keep physical pitch with VCSEL arrays. It is difficult for us to meet this requirement if we use four inductances in each channel.

In our design, as is shown in Fig.4, we propose a pre-amplifier with multi-stage low load resistance differential amplifiers cascaded to solve these problems. Low load resistance can effectively enhance the bandwidth of the pre-amplifier. Although low load resistance reduces the voltage gain of each stage at the same time, it can be compensated by adding extra stages.

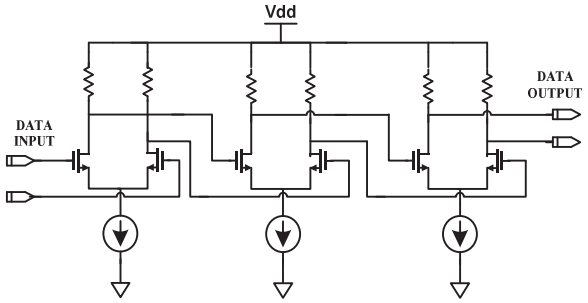

Figure 4. cascading low load resistance amplifier to enhance bandwidth

C. *Implementation of output stage*

Schematic of the output stage is shown in Fig. 5. A dummy resistance is connected at the other side of the output stage to match the equivalent resistance of the VCSELs. In order to reduce the switch-off time of the VCSELs, C^3A technique is adopted by putting a capacitance Cc between the sources of M1 and M6.

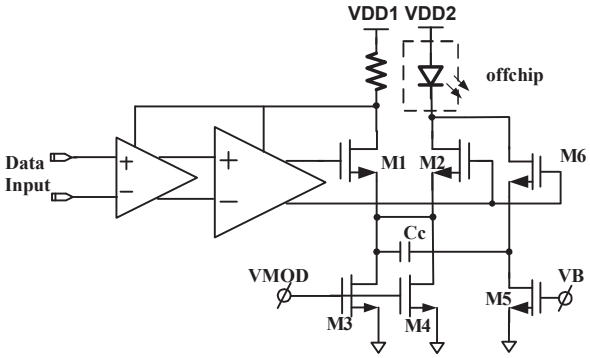

Figure 5. Proposed output stage using C^3A technique

III. LAYOUT AND SIMULATION

This VCSEL driver was fabricated in a standard 0.18μm CMOS process with a chip area of 1.3mm×0.7mm. The layout of this VCSEL driver is shown in Fig. 6. The total DC power dissipation is only 230mW from a single 1.8-V supply.

By adding a pair of PRBS31 voltage signals with Vpp=400mV at the differential input, Fig.7 and Fig.8 show the simulation results of the VCSEL driver at 10Gbps and 12.5Gbps respectively. The simulated rise/fall time of the output current is below 40ps for 0.2pF VCSEL capacitance.

IV. CONCLUSION

The designed VCSEL driver chipset provides high speed solution in smaller area without passive inductor. Using the open drain circuit topology, the VCSEL driver has a 13mA modulation current with power consumption of 50mW per channel. Therefore, it can be applied to short-haul application.

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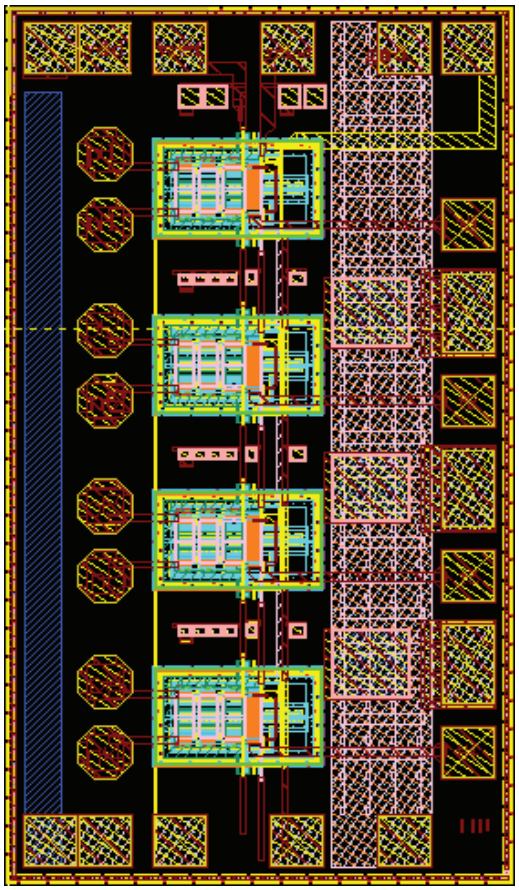

Figure 6. Layout of 4 channels VCSEL driver

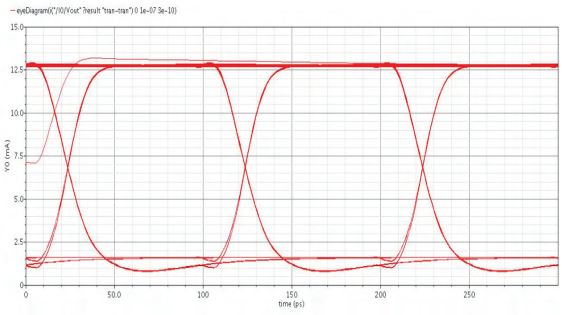

Figure 7. Current eye diagram of VCSEL driver at 10Gbps

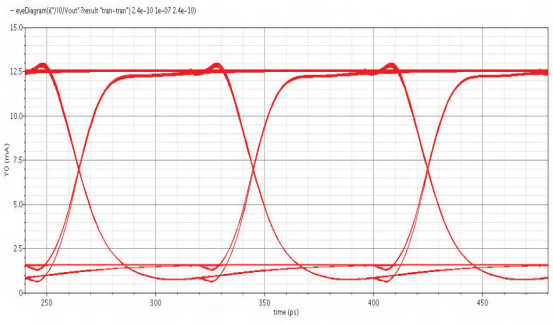

Figure 8. Current eye diagram of VCSEL driver at 12.5Gbps

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