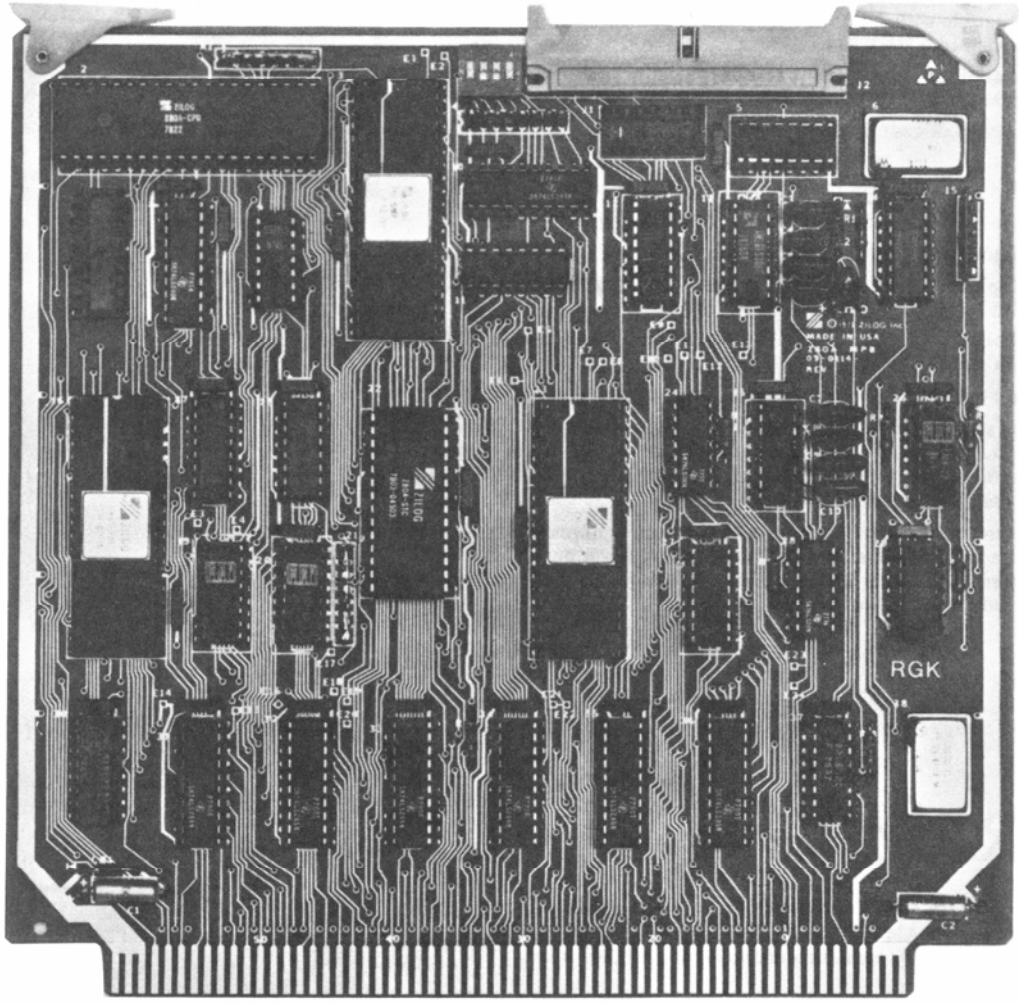
Zilog

4 MHz Microcomputer Boards



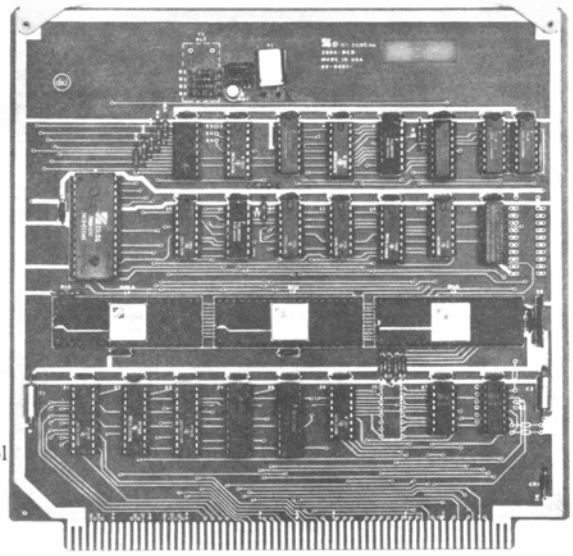
Z-80A MPB

The Z-80A Microcomputer Board (Z-80A MPB) is the principle card in a family of boards designed to operate at 4 MHz. The MPB includes the Z-80A Microprocessor and four of the Zilog I/O peripheral components. (Z-80A SIO, Z-80A CTC, Z-80A PIO and Z-80A DMA). These peripheral devices are configured to support a line printer interface, two independent full duplex serial communication channels and direct memory access control.

Features

- Z-80A Microprocessor operating at 4 MHz.
- Board size: 7.7 x 7.5 in. with 122 Pin edge connector.
- Two independent full-duplex serial interface channels implemented with the Z-80A SIO and buffered for RS422 and RS423 interface. RS232 type terminals are also compatible with the MPB.
- Two on-board oscillators for CPU clock and baud rate reference clock.
- Baud rates, programmable via on board-switches.
- Programmable baud rate clock obtained from a Z-80A CTC with unused channels fed to edge connector for easy access.
- Sixteen programmable parallel I/O lines implemented with Z-80A PIO directly interfaces to line printer. Buffers are located in sockets for easy replacement and jumper programmable for direction and tri-state buffer control.
- Optional block transfer and data search control using Z-80A DMA.
- Flexible peripheral selection throught PROM decoding.
- Hysterisis buffers are supplied on data, address and control lines for off board expansion.
- Interrupt daisy chain configured with "look ahead" and "wait" state generation logic to facilitate Priority Ripple during interrupts. This logic will support a daisy chain of up to 11 Z-80A peripheral devices.

Z-80A FDC



The Z-80A FDC is a highly verastile single-board disk controller that is part of Zilog's 4MHz OEM Microcomputer Board Series.

The Z-80A FDC provides direct control of up to 8 single-density floppy or mini floppy disk drives. Double sided drives are also supported.

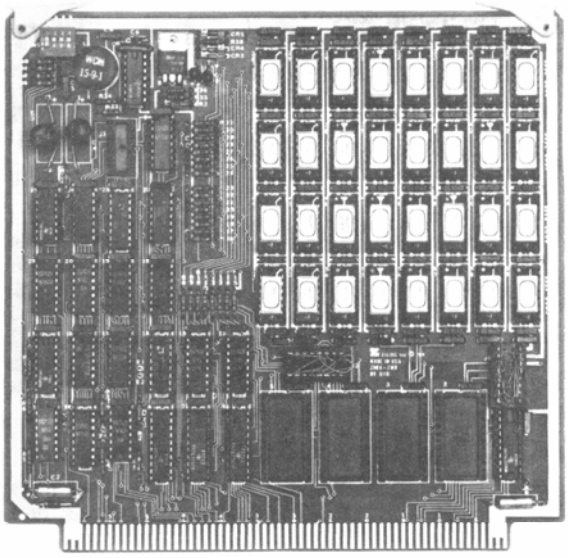
All file formatting and mapping functions are controlled by PROM-based software, which gives the FDC considerable flexibility regarding disk compatibility, file organization and drive configurations.

The FDC is designed to interface to Shugart 400, 450, 800, 850 series floppy disk drives, but the control and data port bits are I/O programmable, allowing configurations that can be tailored to the needs of the individual user.

Features

- Functionally compatible with Z-80 MDC. File written on 2.5 MHz systems can be immediately upgraded to 4 MHz.
- For system configurations that require processor-free data exchange, a Zilog Z-80A DMA can be programmed for direct data transfer between memory and disk.
- A Z-80A CTC provides all counting and timing functions as well as interrupt control for the DMA.
- Board size: 7.7 in. (19.6 cm) x 7.5 in. (19.1 cm) with a 122 pin edge connector.
- On-board oscillator for disk control and data recovery timing.
- A Z-80A PIO is used for disk status and control.
- An on-board multiplexor selects standard or mini floppy data rates, and is software-controlled by an output bit of the Z-80A PIO.
- A digital "Phase-Lock" oscillator and data separator encodes and decodes FM data, allowing both clock and data channels to be recovered by a Z-80A SIO.
- FDC supports both radial and binary select and both single and double sided drives.
- All on-board ports are addressed by an on-board port decoding PROM. This allows the user to tailor the port space of each board for custom configurations requiring non-standard port assignments, of for configurations requiring multiple Z-80A FDC's on the same backplane.
- Increased buffer drive to support two independent cables to normal "Shugart" termination. This is useful when expanding to additional drives outside the main enclosure. It does not require the user to remove termination from drives which are already mounted in the enclosure.

Z-80A RRM



The Z-80A RRM provides the 4 MHz OEM Microcomputer Board family with either 16 or 64K bytes of dynamic RAM memory. In addition, there are sockets for up to 8K bytes on non-volatile memory consisting of PROM or EPROM.

Features

- Provides for 64K bytes of dynamic RAM in four banks of 16K bytes each.
- RAM implemented with 16K x 1 dynamic RAM element.
- Four sockets allow up to 8K bytes of non-volatile memory using 5 volt 2716 EPROM's or equivalent.
- Wait state, jumper programmable for use with slow access time EPROM's.
- Two modes of RAM memory bank selection:
  - Mode 0: Enable both RAS and CAS to selected bank only.
  - Mode 1: Enable RAS to all banks and use CAS to select the appropriate bank. (For refresh during extended DMA).
- On-board DIP switch determines boundry between ROM and RAM.
- Non-volatile memory may be completely disabled to allow full access to 64K bytes of memory. This feature also allows bootstrap ROM implementation.
- Hysterisis buffers on all address and data lines.
- External bank selection allows card to be configured for operation in a system exceeding 64K bytes.

10340 Bubb Road, Cupertino, California 95014
Printed in U.S.A.

Zilog

Telephone: (408) 446-4666 TWX: 910-388-7621