OPERATION MANUAL

Please read Operator's Manual prior to installing or operating this device. Your warranty may be affected by failure to read the Operator's Manual prior to installation.

BRUCE DETTON

D·G ELECTRONIC DEVELOPMENTS CO.

(214) 465-7805
700 South Armstrong
Denison, Texas 75020

REGULATORY INFORMATION

This equipment complies with the requirements in Part 15 of FCC Rules for a Class A computing device. Operation of this equipment in a residential area may cause unacceptable interference to radio and TV reception requiring the operator to take whatever steps are necessary to correct the interference.

Congratulations on the purchase of your new HEARTBEAT computer. This product has been provided to you by an authorized HEARTBEAT dealer who will also provide warranty service for your system. If you should experience difficulties during installation or operation return the product to your dealer for repair during the first 90 days. Your dealer is qualified and authorized to make necessary modifications and/or repairs.

D-G Electronic Developments Company, Inc. does provide repair services for a nominal fee after the warranty has expired. The purchaser should contact D-G Electronic Developments Company, Inc. at AC(214)465-7805 prior to returning the unit to receive the necessary "RETURN MERCHANDISE AUTHORIZATION" number. Failure to do so will result in the return of the unit without repairs.

To qualify the unit for "after warranty" service from the factory you must complete the attached registration card and return it to:

D-G Electronic Developments Company, Inc.
700 South Armstrong
Denison, TX 75020

********** KEEP THIS PORTION FOR YOUR RECORDS **********

DETACH ALONG THIS LINE

PURCHASE REGISTRATION CARD

(Please print plainly or type)

PURCHASER

NAME:_____

ADDRESS:_____

CITY, STATE:_____ZIP CODE:_____

HEARTBEAT SERIAL NUMBER: 01-1007

DATE PURCHASED_____

DEALER

NAME:_____

ADDRESS:_____

CITY, STATE_____ZIP CODE:_____

YOU MUST COMPLETE THIS CARD TO QUALIFY FOR AFTER-WARRANTY SERVICES AND TO RECEIVE FUTURE PRODUCT ANNOUNCEMENTS.

LIMITED WARRANTY

The DG HEARTBEAT computer is warranted for a period of ninety (90) days from the date of purchase to be free from defects in material and workmanship. Should this product fail to perform satisfactorily, arrangements should be made with the authorized dealer from whom you purchased the unit computer for warranty service.

Your authorized dealer may at his option, repair or replace defective units received during the warranty period. This warranty is invalid if the product has been misused or modified. Warranty is limited to replacement of defective materials and no responsibility is assumed for damage to other equipment. If it becomes necessary to deliver this product to the factory for warranty service you agree to insure the product or assume the risk of loss or damage in transit, to prepay shipping charges to the factory and to use the original shipping container or equivalent.

All express and implied warranties for this product including the warranties of merchantability and fitness for a particular purpose, are limited in duration to a period of 90 days from the date of purchase, and no warranties, whether express or implied, will apply after this period. Some states do not allow limitations on the duration of implied warranties, so these above limitations may not apply to you.

In no event shall D-G Electronic Developments Company, Inc. be liable to you for any damages, including any lost profits, lost savings or other incidental or consequential damages arising out of the use of or inability to use this product. Some states do not allow the exclusion or limitation of incidental or consequential damages for consumer products, so these limitations may not apply to you.

This warranty gives you specific legal rights, and you may have other rights which vary from state to state.

TABLE OF CONTENTS

PREFACE

This manual provides you with an introduction to the D-G Heartbeat computer. Included are sections on system set-up, basic operation, installation of additional peripheral devices and basic theory of operation. You may find upon first reading through this manual several terms and concepts with which you are not familiar. This, of course, is due to the fact that the personal computer is the result of new and fast changing technologies. Although it is not necessary to fully understand these technologies, the learning of a few basic concepts and the terminology (or "buzz words") used to describe them will prove invaluable as you begin to use your computer. A glossary of computer terms has been included to help you through the early learning process.

The first-time user of a personal computer may also find it useful to discuss with his computer dealer (or a local computer club) the various computer publications for beginners. Many well written text are available describing basic computer operation as well as the many programming languages available for use on your Heartbeat computer. Remember that your personal computer is a "tool". A strong understanding of that tool and its capabilities will broaden the nature and scope of problems which it will solve. .

***** INTRODUCTION *****

The D-G Heartbeat is a compact computer system designed to be hardware and software compatible with the popular Heath/Zenith Z89/90 computer product line. The Heartbeat offers advanced features not found on the standard Heath/Zenith computer such as 4 MHZ operation, real-time clock/calendar, two RS-232 serial ports, five peripheral expansion slots, 128 Kbytes (expandable to 256 Kbytes) parity checked RAM and provisions for an optional AM9511 Arithmetic Processor. The Heartbeat may be used with most popular video terminals on the market although the Heath/Zenith H/Z19, H/Z29 and ZT-10/11 video terminals are recommended for full Heath/Zenith software compatibility. The Heartbeat cabinet design provides for inclusion of hard and/or floppy disk drives as well as other desired peripheral interfaces and is color-coordinated for use with the Zenith Z29 and ZT-10/11 video terminals.

A typical Heartbeat system will consist of the Heartbeat "main-frame" with two floppy disk drives installed, a video terminal and a printer. In this configuration the lower disk drive will be Drive "0" (or "A" in a CP/M system) and the upper disk drive will be Drive "1" (or "B"). Since many other Heartbeat system configurations and options are available, the user should discuss his particular system configuration with his dealer before attempting to use his Heartbeat system.

Physical Description

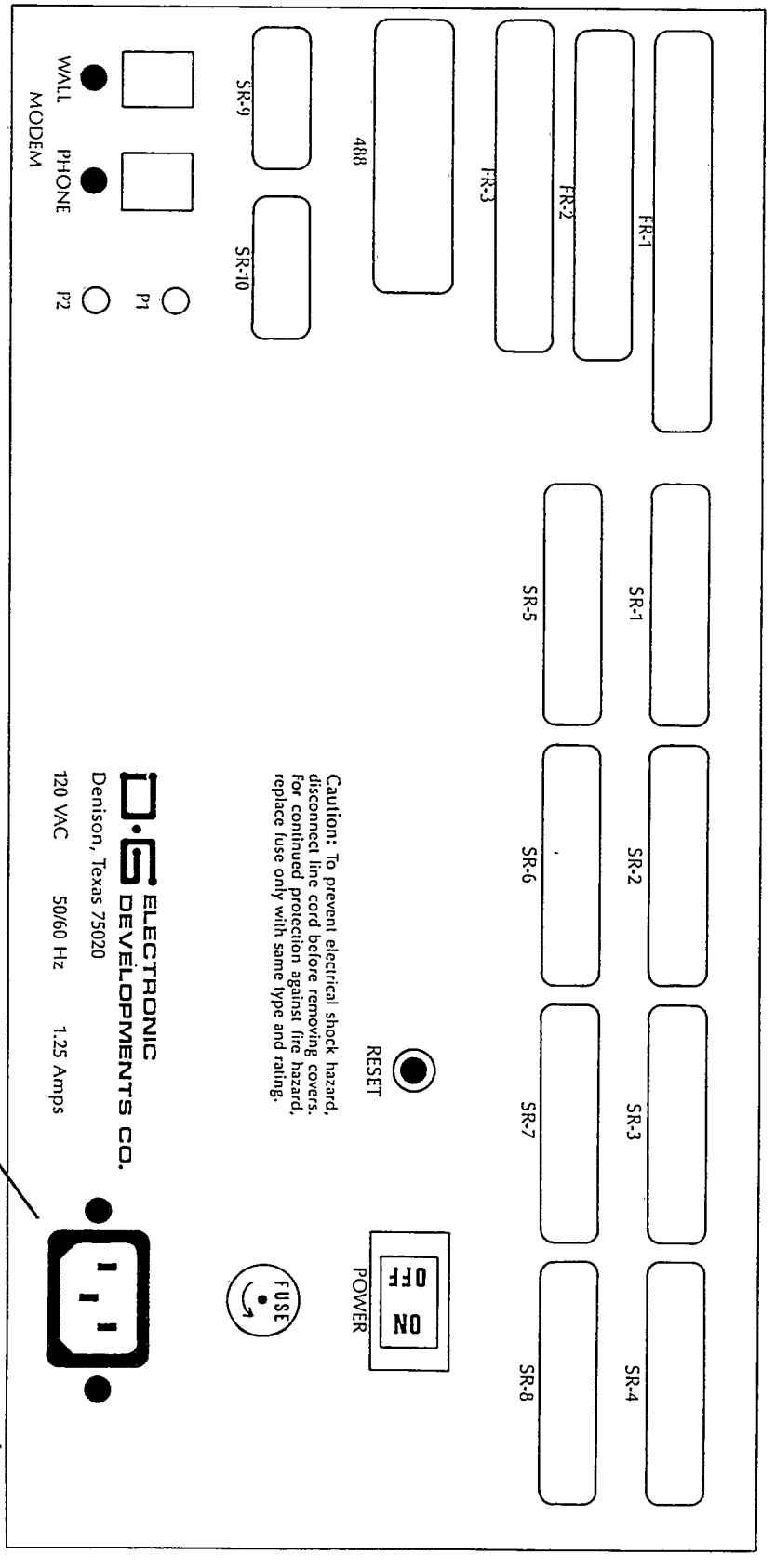
The D-G Heartbeat is packaged in a compact metal enclosure which may be placed on a desk top or "hidden" within the desk or work cabinet. The unit contains a low-noise ventilation fan and should have access to a moderate air opening. The front panel of the cabinet consists of the power-on LED indicator, internal drive activity indicator and the access door(s) of the disk drive(s). The rear-panel contains the AC line connector, fuse-holder, power switch, system reset pushbutton switch and the following peripheral connector cutouts (refer to FIGURE 1 for rear-panel layout).

QUANTITY	DESCRIPTION
8	RS-232 25-pin "D" Connectors
2	9-pin "D" Connectors
1	IEEE 488 Connector
1	5Ø-pin Ribbon Cable Connector
1	4Ø-pin Ribbon Cable Connector
1	34-pin Ribbon Cable Connector
2	Modular Telephone Connectors

General Specifications

Power Source	115 VAC 5Ø/6Ø Hz 15Ø Watts max (23Ø VAC unit available)
Internal Supplies	+5VDC +/- Ø.2% @ 1ØA +12VDC +/- 5% @ 4A (5A PEAK; less than 1Ø seconds) -12VDC +/- 5% @ 1A
Weight	Approximately 25 pounds
Physical Dimensions	7.2" x 13.6" x 14.4" (HWD)
Operating Temperature	15 to 3Ø degrees C

*** FIGURE 1 - HEARTBEAT BACK PANEL ***



***** SYSTEM SETUP *****

The D-G Heartbeat is available in many system configurations and may be used with a wide variety of system peripherals. This procedure assumes that your Heartbeat was purchased from a computer dealer or system integrator who has installed the appropriate interface devices and set switch and jumper options for your desired system. If you are adding peripheral devices or otherwise changing the configuration of your Heartbeat, you should refer to the System Configuration section of this manual before proceeding.

1) Place your Heartbeat on a desk or worktable so that the rear panel of the computer is accessible.

2) Locate rear panel connector "SR-1" and plug the cable coming from your console or video terminal into this connector.

3) If you are using a serial printer in your system, plug the printer cable into connector "SR-5" on the Heartbeat rear panel.

4) Make sure that the Heartbeat power switch is in the "OFF" position (the "OFF" label on the switch should be depressed) and that the computer line cord is not plugged into an AC outlet. Plug the AC line cord into the Heartbeat rear panel connector first and then into an AC outlet.

5) Place the power switch of your video terminal to the "ON" position and then turn on the Heartbeat computer. The front panel power LED should light and you should hear several short "beeps". After a short warm-up period, you should see the following display on the video terminal screen.

```
4 MHz MTR-S89 (Vxxxx)

Valid bank: Ø
Valid bank: 1
 DG:
```

The reported number of "valid banks" may differ from the above example depending on the amount of memory installed in your Heartbeat. A Heartbeat with 128K RAM will report two valid banks (Ø and 1), a Heartbeat with 192K RAM will report three valid banks and a Heartbeat with 256K RAM will report four valid banks.

6) Refer to the 'Operation' section of this manual for a description of available monitor commands and disk system "boot-up" procedure.

If your Heartbeat does not "sign-on" as described above, carefully re-perform the setup procedure. If the computer still does not perform properly, contact your Heartbeat dealer or system integrator for assistance.

***** OPERATION *****

Operation of the Heartbeat computer normally begins with powering on the video terminal and the computer. At this point, the computer will be in the "monitor" mode of operation. The Heartbeat system monitor is basically a collection of programs stored in read-only memory (ROM) and entered upon system power-up. These programs allow the user to review system options, set the Heartbeat real-time clock, "boot" the desired mass storage device (disk drive) or perform simple system diagnostics. The advanced user may use commands provided by the monitor for entering and debugging programs in Heartbeat system memory.

Most of the time, the system monitor will be used for "booting" the computer's disk system. Operation of a disk system with the computer requires another set of programs, called a Disk Operating System (DOS). The Disk Operating System manages, in an orderly fashion, the use of the computer system's components by applications software and other programs. The "boot" or "bootstrap" procedure is the method by which the operating system is loaded from a diskette into the computer's memory and initialized for operation. Portions of the operating system itself are responsible for this initialization procedure so it may be compared to a person "pulling himself up by his own bootstraps".

MONITOR COMMANDS

The following commands and functions are provided by the DG Heartbeat monitor. When typing commands and hexadecimal values, letters (except for register names in the "Register" command) may be typed in either upper or lower case. Only the first letter of a command should be typed; the computer displays the entire command. At any point prior to typing the RETURN key, a line may be cancelled by typing the DELETE key. When typing in a hexadecimal or octal value, errors may be corrected by retyping the entire correct value; the monitor uses only the last digits typed.

```
**************************************************************
**                                                          **
**  IN ALL OF THE FOLLOWING EXAMPLES USER INPUT IS DESIGNATED  **
**  BY AN UNDERSCORE.  THE COMPUTER OUTPUT AND EXPLANATIONS  **
**  CONSIST OF THE NORMAL TYPE WITHOUT THE UNDERSCORE.  A  **
**  USER SUPPLIED CARRIAGE RETURN IS INDICATED BY THE SYMBOL  **
**  <CR>, A SPACE BY <SP>, AN EQUAL SIGN BY <=>, A MINUS SIGN  **
**  BY <-> AND THE DELETE KEY BY <DEL>.                     **
**                                                          **
**************************************************************
```

Help

The "Help" command provides a display of the available Heartbeat monitor commands and their options.

EXAMPLE:

```
DG: Help <CR>

Command/options:
          Boot
          Check
               Disk
               Ram
          Date/time
               Display
               Set
          Exit to HDOS
          Go
          Help
          In
          Memory
          Number base
               Hexadecimal
               Octal
          Out
          Register
          Step
          View

DG:
```

Boot

This command provides for "booting" of system mass-storage devices. Typing "B" followed by the RETURN key initiates boot from Drive Ø of the default boot device. (The default boot device is chosen by the setting of Switch S2 on the Heartbeat CPU board.) In the typical Heartbeat system, this will be the lower floppy disk drive on the computer front panel. Any other disk device present in the system may be booted by typing "B" followed by the appropriate device type letter shown in the "Boot help" list below. A disk unit (i.e. a specific drive) other than "Ø" may be booted by following the device type with the unit number, then the RETURN key.

A command string may be passed to the "bootstrap" code by typing a slash ("/") and then the command string after the device and unit and before the RETURN key. This feature allows for selection of bootable "partitions" in disk systems such as the Heath/Zenith Z67. Refer to the Z67 Operation Manual for a discussion of partitioning of large capacity disk devices and use of the command string.

If the read of the boot track is not complete after 16 seconds, or if an I/O error occurs, the boot is aborted with the message "Boot error". The boot procedure may also be aborted by depressing the DELETE key.

Pressing the "H" key (Help) after the Boot command will provide a display of the boot device types, their device type identifiers and the permissible number of units of each type in the system.

Examples:

DG: Boot <CR> (Unit Ø of the primary boot device is booted.)

DG: Boot J: 1/CPM <CR> (Unit 1 of the Z-67 is booted, and a command string of "CPM" is passed to the bootstrap code.)

DG: Boot H: <CR> (The boot "Help" list will be displayed.)

Dev	Units	Cntlr
A	6	H17
B	4	H37
C	9	CORVUS
D	4	CDR
E	4	H47 @ 78
F	4	H47 @ 7C
G	8	DG
J	8	H67 @ 78
K	8	H67 @ 7C
L	4	LLL
M	8	MMS
P	3	RAM

Date/time

This command displays and alters the date and time values maintained by the Heartbeat real-time clock. If you type "D" for "Date" followed by "D" for "Display" and then the RETURN key, and the clock has been set, the day of the week, the date and the time will be continuously displayed and updated. If the clock has not been set the message "Clock not set" will be displayed and you will be prompted for new clock values. Typing "D" followed by "S" for "Set" will also allow the clock to be set.

Values entered are not checked for validity, except that they must be decimal values. For each prompt you may then type a new value followed by a space or only a space (which produces the prompt for the next clock value). Typing only a space in response to any prompt does not change the clock value associated with that prompt, but only produces the prompt for the next clock value. Any time a value followed by a space is entered in response to the "minutes" prompt, the clock's "seconds" value is set to zero, and the clock is started. Note that the day of the week is entered as a single digit from 1 (Sunday) to 7 (Saturday).

Example:

(This example sets and then displays the clock values.)

```
 DG: Date/time Set<CR>
Clock not set
Min: 3Ø<SP>
Hr: 16<SP>
Day: 15<SP>
Wkday: 6<SP>
Mo: 1Ø <SP>
Fri   Oct 15, 1982   16:3Ø:Ø9.2
 DG: Date/time Display <CR>
Fri   Oct 15, 1982   16:3Ø:11.7<DEL>
 DG:
```

Check RAM

The Heartbeat memory check is initiated by typing "C" for "Check", "R" for "RAM" and then the RETURN key. The display will show the address limits of the system RAM tested, and will show a varying "Bank:" and "Mask:" value. The bank value is the bank number being tested; the mask value is used along with the address bits to generate a test value of either AA or 55 (hexadecimal) for each byte in memory. The test uses 16 mask values for each bank, beginning with AB (hexadecimal), and then repeats. An error is indicated by an error message and a beeping tone from

the computer. The error message will show a memory location and a byte value. The memory bit in error may be determined by comparing the error byte to either AA or 55 (hexadecimal). This command is terminated by resetting the computer.

Example:

(This example initiates the dynamic RAM test.)

```
 DG: Check RAM <CR>
4 MHz reset
Dynamic RAM test 2ØØØ to FFFF
        Bank: Ø  Mask: AB
```

Check disk

This command is only functional with the Heath/Zenith H-88-1 hard-sector disk controller. Insert any diskette in mini-floppy disk drive "Ø" and type "C" for "Check", "D" for "Disk" and then the RETURN key. The diskette is not altered; any initialized or uninitialized hard-sectored (1Ø sectors per track) diskette may be used. The display will show the word "Rotation" flashing, and, if the disk drive is within tolerance (1%), the display will show a number between 1FB and 2Ø5 (hexadecimal). The drive should be adjusted to show a number as close to 2ØØ as feasible. The disk drive test may also be used with a drive other than drive "Ø" by typing "C", "D", the disk drive unit number and then <CR>. This command is terminated by depressing the DELETE key.

Example:

(This example tests the rotation speed of mini-floppy drive 1.)

```
 DG: Check disk 1 <CR>
       Rotation time: Ø2ØØ
```

DEBUGGING COMMANDS

The following commands provide for modification and debugging of data and programs in the Heartbeat system memory.

Number Base

This command sets the number base (radix) for numeric values of all monitor commands except for the "Check RAM" command. The options for this command are "H" for hexadecimal and "O" for octal. The RETURN key should be pressed after the option.

Example:

```
DG:Number base Octal <CR>
DG:
```

This example changes the numeric base to octal.

View

The View command displays on the console the contents of blocks of memory in the current radix and in ASCII. The display begins at the address specified (ØØØØH if no address follows the View command) and extends for 256 bytes if the current radix is hexadecimal and 128 bytes if the current radix is octal. The next address to be viewed appears on the last line of the display. The command may be terminated by pressing the DELETE key or the next block of memory may be viewed by pressing the RETURN key. Each displayed line consists of sixteen hexadecimal (eight octal) bytes followed by the ASCII equivalent values of these same bytes. Memory values whose low-order seven bytes do not represent a displayable ASCII character are displayed as a period (.).

Example: (Current radix is hexadecimal)

```
 DG: View 5ØØØ <CR>
5ØØØ  ØØ Ø1 Ø2 Ø3  Ø4 Ø5 Ø6 Ø7  ...  ØC ØD ØE ØF  ................
5Ø1Ø  1Ø 11 12 13  14 15 16 17  ...  1C 1D 1E 1F  ................
  .
  .
5Ø4Ø  4Ø 41 42 43  44 45 46 47  ...  4C 4D 4E 4F  @ABCDEFGHIJKLMNO
5Ø5Ø  5Ø 51 52 53  54 55 56 57  ...  5C 5D 5E 5F  PQRSTUVWXYZ[\]^_
  .
  .
  .
5ØFØ  FØ F1 F2 F3  F4 F5 F6 F7  ...  FC FD FE FF  pqrstuvwxyz{|}~.
51ØØ
```

If the RETURN key were pressed at the end of this example, the memory locations from 51ØØH to 51FFH would be displayed.

Memory

This command displays and alters the values in RAM segments of system memory (ROM memory values may only be displayed). Type "M" for "Memory", the memory address you wish to examine and then the RETURN key. The computer will display the memory address again followed by the memory value at that address. You may then perform one of the following actions:

1) Type a space. The display will increment to the next memory address.

2) Type a minus sign. The display will decrement to the previous memory address.

3) Type a new value, followed by the RETURN key. The new value will be entered into the displayed memory address and that address and its new contents will be repeated on the display.

4) Type a new value, followed by either a space or a minus sign. The new value will be entered into the displayed address and depending on your choice the previous or next memory address will be displayed.

5) Type an equal sign. A breakpoint "Pause" will be inserted at the displayed memory location.

6) Type the DELETE key to terminate the "Memory" command.

When a "Pause" (a "RST Ø") breakpoint is subsequently encountered during program execution, the monitor regains control. Note that any transfer of control to memory address zero (except for a hardware reset) is considered to be a "Pause"; the value in the top of the stack is assumed to be the current PC register value. If you intend to resume program execution after a "Pause", you should replace the byte at the address shown for register "PC" (in the "Pause" message) minus one, with the original value at that address (shown when the "Pause" was inserted in memory), and then transfer control to that address (via the "Go" command).

Examples:

(This example shows location 2293 examined, location 2294 altered, location 2295 examined, location 2294 altered a second time and location 2293 examined a second time.)

```
 DG: Memory 2293 <CR>
2293 78<SP>
2294 Ø3 77<SP>
2295 79 Ø<->
2294 77 76<->
2293 78 <DEL>
 DG:
```

(This example inserts a "Pause" in memory, examines three more bytes, and then transfers control to the "Pause" instruction.)

```
 DG: Memory 228Ø<CR>
228Ø AF<=>
228Ø C7<SP>
2281 C9<SP>
2282 FE<SP>
2283 Ø6 <DEL>
 DG: Go 228Ø<CR>

[Pause]
XX=1234 af=4321 bc=5678 de=8765 hl=1122 YY=5678
SP=FFFØ AF=ABCD BC=2222 DE=8181 HL=8213 PC=2281  => C9 FE Ø6 CA
 DG:
```

Register

This command displays and alters the register values of a user program. Type "R" for "Register" followed by the RETURN key; all register pair values will be displayed. You may then optionally type a register name or <CR> to terminate the command. When a register is to be altered, type the first letter of a Z8Ø primary register pair name in upper case (i.e., S(P), A(F), B(C), D(E), H(L), P(C)); type an upper case "X" or "Y" for the Z-8Ø index registers "IX" and "IY"; type the first letter of a Z-8Ø alternate register pair name in lower case (i.e, (a(f), b(c), d(e), h(l)). The computer will type the second letter of the name. The new register value should be typed after the register name, and will become effective when control is next passed to the user program (any new values entered for register "SP" are ignored). The new register values will then be displayed. You may then type the RETURN key to return to the monitor mode.

Examples:

(This example displays all of the register values.)

```
 DG: Register<CR>
XX=1234  af=5678 bc=5444 de=AB45 hl=ACAD YY=9ABC
SP=FFFØ  AF=CDEF BC=AAAA DE=BBBB HL=CCCC PC=FFFØ  =><CR>
 DG:
```

(This example displays all of the registers and alters the program counter register.)

```
 DG: Register <CR>
XX=1234 af=4321 bc=5678 de=8765 hl=ABCD YY=9ABC
SP=FFFØ AF=5678 BC=8765 DE=ABAB HL=DADA PC=FFFØ  => PC 228C<CR>
XX=1234 af=4321 bc=5678 de=8765 hl=ABCD YY=9ABC
SP=FFFØ AF=5678 BC=8765 DE=ABAB HL=DADA PC=228C  =><CR>
 DG:
```

Go

This command transfers control to a program. If you type an address after the "G", control passes to the program at that address. If you type the RETURN key after the "G", control passes to the current address value in the user PC register.

Examples:

DG: Go 228Ø<CR>	(Control is transferred to the program at 228Ø.)
DG: Go<CR>	(Control is transferred to the program at the address specified by the current value of the program counter register.)

Step

This command transfers control to a program, executes one instruction, displays all register values and the next four sequential bytes from memory, and returns control to the monitor. If you type an address after the "S", control passes to the program at that address. If you type the RETURN key after the "S", control passes to the current address value in the user PC register. Note that if the single instruction executed is a "DI" (disable interrupts), execution of the program will continue until an "EI" (enable interrupts) instruction is executed.

WARNING: You should not step through time-dependent code in operating systems (such as device drivers). If you step through a disk device driver, you might destroy information on a diskette.

Example:

(This example single steps twice the program beginning at 228Ø.)

```
 DG: Step 228Ø<CR>
XX=1234 af=1234 bc=5678 de=9ABC hl=DEFØ YY=9ABC
SP=FFFØ AF=4321 BC=8765 DE=CBA9 HL=ØFED PC=2281  => AF 57 C9 FE
 DG: Step <CR>
XX=1234 af=1234 bc=5678 de=9ABC hl=DEFØ YY=9ABC
SP=FFFØ AF=ØØ21 BC=8765 DE=CBA9 HL=ØFED PC=2282  => 57 C9 FE ØA
 DG:
```

Exit To HDOS

This command is equivalent to "Go 4Ø1ØØ" (octal) or "Go 2Ø4Ø" (hexadecimal) and is designed to aid in the debugging of programs running under the Heath Disk Operating System (HDOS). If HDOS is still in memory, the operating system will regain control and display the HDOS prompt. If section "4" of switch S1 on the CPU board is set to "Ø", memory is remapped to all RAM.

Example:

(Control is transferred to the program at 2Ø4ØH.)

```
 DG: Exit to HDOS <CR>
```

In

This command inputs a value from a Heartbeat system I/O port. Type "I" for "Input", the port address you wish to examine and then the RETURN key. The computer will display the port address and the input value. You may then type the DELETE key (which terminates the "In" command), a space (which increments the displayed port address and contents), a minus sign (which decrements the displayed port address and contents) or an equal sign (which repeats with the same port address).

Example:

(This example inputs twice from port F2.)

```
 DG: In f2 <CR>
ØØF2 2Ø<=>
ØØF2 2Ø<DEL>
 DG:
```

Out

This command outputs a value to a Heartbeat system I/O port. Type "O" for "Output", a port address and then the RETURN key. The computer will display the port address. You may then optionally type an output value followed by the RETURN key (which outputs the value to the displayed port address), a space (which increments the displayed port address), a minus sign (which decrements the displayed port address) or the DELETE key which terminates the 'Out' command.

Example:

(This example outputs two values to port EØ.)

```
 DG: Out eØ<CR>
ØØEØ 48<CR>
ØØEØ 49<CR>
ØØEØ <DEL>
 DG:
```

***** SYSTEM CONFIGURATION *****

The D-G Heartbeat is based on the D-G SUPER 89 single board computer and is therefore compatible with a variety of interface devices manufactured by Heath/Zenith and other vendors. The MTR-S89 monitor ROM used in the Heartbeat provides "boot" support for mass storage devices and interfaces manufactured by Heath/Zenith, D-G, C.D.R. Systems and Magnolia Microsystems.

Standard Jumper Settings

The following Heartbeat jumper settings should be used for the MTR-S89 monitor ROM and were set at the factory. Refer to FIGURE 2 and check the settings when configuring your Heartbeat system.

Jumper	Settings
J1	A1Ø
J2	C
J3-U37	
PIN 18	CS
PIN 21	W
J3-U36	
PIN 18	CS
PIN 21	All (A - Eleven)
RSP-36	No jumpers installed
RSP-37	6K

SC The system clock jumper should be set to the user's desired clock frequency, either 2 or 4 MHz.

MSA Set to "2"

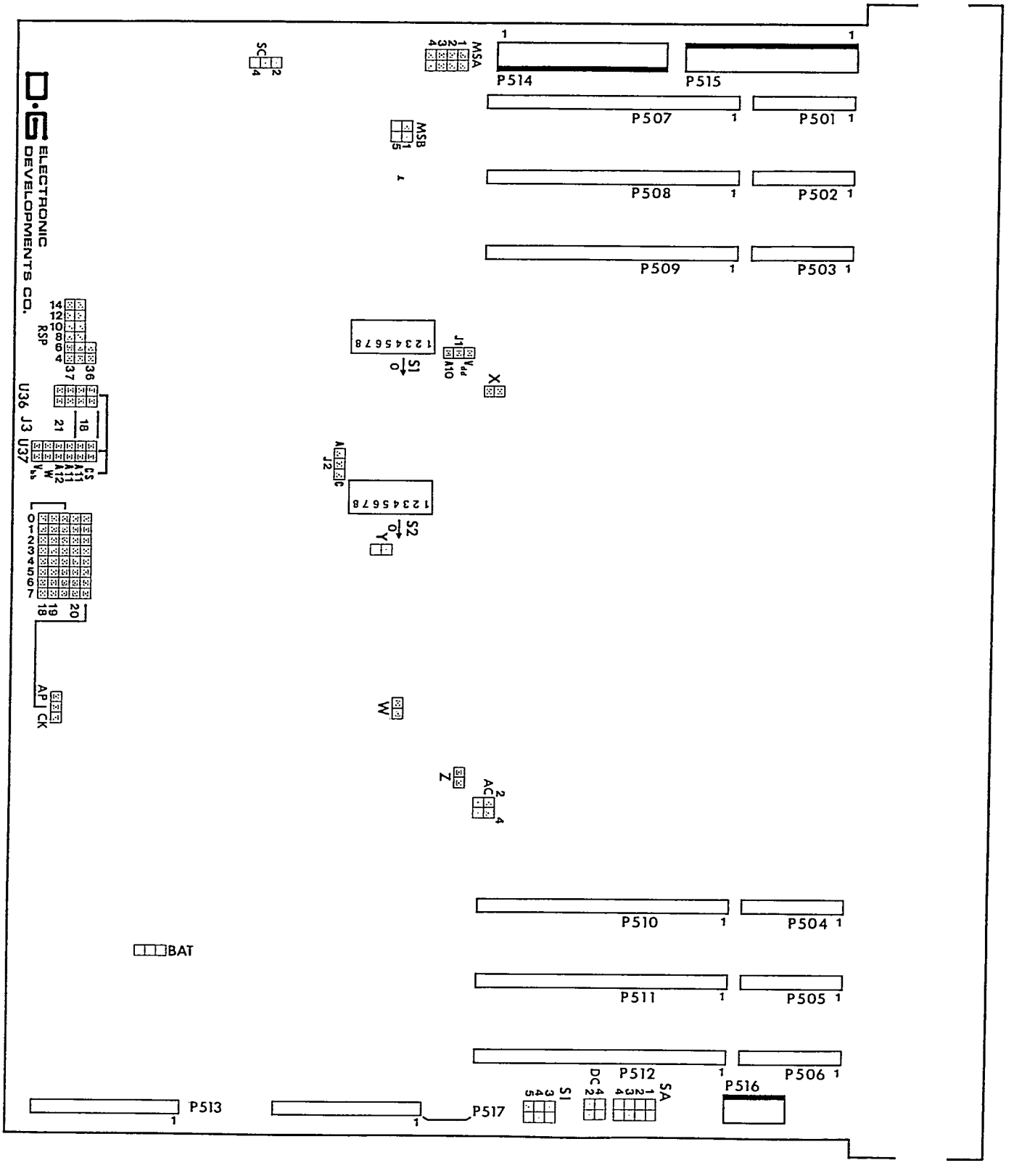
MSB Set to "1"

AC See the AM9511 installation section of this manual if the arithmetic processor is to be installed in your Heartbeat

PRIMARY JUMPER BLOCK	No jumpers installed
AP/CK	No jumper installed
X	Jumper installed
Y	No jumper installed
Z	Jumper installed
W	Jumper installed

Jumper settings and installation for specific Heath products follow. You must also set Switches S1 and S2 on the Heartbeat CPU board as described in the "System Configuration Switches" section of this manual beginning on page 29.

*** FIGURE 2 - JUMPER POSITIONS ON BOARD ***



Interface Board Installation

Interface boards may be installed on either the left-hand set of bus slots (P5Ø1/P5Ø7 or P5Ø2/P5Ø8) or the right hand set (P5Ø4/P51Ø, P5Ø5/P511 or P5Ø6/P512) in the D-G Heartbeat mainframe. Refer to Figure 2 for identification of these connectors. Choice of bus slot is usually determined by the I/O port requirements of the interface board being installed. Refer to the installation manual supplied with your particular interface board for slot selection requirements.

The board retaining bracket must be removed to install a board in the mainframe. The right-hand retaining bracket is removed by removing the two screws at the base of the bracket and pulling the bracket straight up. When the desired interface board(s) has (have) been installed, replace the bracket making sure that the boards fit into the plastic card-edge guides on the bracket. The left-hand bracket may be removed by removing the two screws which hold the bracket to the AC enclosure. When re-installed, the bracket should be pushed up against the interface boards so that they fit snugly into the plastic edge guides.

WARNING: Whenever boards are installed in the Heartbeat, make certain that the edge connectors plug properly onto the bus pins. No pins should be bent and each pin should plug into a position on the board edge connector. Permanent damage may result if interface boards are improperly installed.

The Heartbeat is fully compatible with the Heath/Zenith H-88-1, Z-89-47, Z-89-37 and Z-89-67 disk system interfaces as well as the HA-88-3 Serial Interface Accessory and the Z-89-11 Multifunction I/O card. If you intend to use the Heath/Zenith H-88-1 hard-sector controller or the Heath Disk Operating System (HDOS) you must install a Heath H-88-1 support ROM (Heath part number 444-19) at U37 on the SUPER 89 CPU board. This ROM is available from your Heathkit Electronic Center or the dealer from which you purchased your Heartbeat computer.

H-88-1 Floppy Disk Accessory

Operation of the Heath H-88-1 disk system is as described in the Heath H-88-1 instruction manual. Jumper DC (Disk Clock) should be set to the "2" position (2 MHz) and the controller board should be installed at P5Ø6/P512 on the Heartbeat CPU board.

NOTE: Heath/Zenith CP/M 2.2.Ø3 and 2.2.Ø4 require patches for proper operation of the H-88-1 hard-sectored disk system in a 4 MHz system such as the D-G Heartbeat. These patches are available from D-G Electronic Developments Company.

HA-88-3 Serial Interface Accessory

The Heath/Zenith HA-88-3 Serial Interface Card may be installed in the D-G Heartbeat at P5Ø5/P511 on the right-hand side of the CPU board or at P5Ø2/P5Ø8 on the left-hand side of the board. Normally the HA-88-3 will be installed at P5Ø5/P511. In this case, the "SA" jumper on the Heartbeat CPU board should be set to position "1". The Heartbeat on-board serial port will then be addressed at port TS1 (22Ø-227Q). Operation of the HA-88-3 serial ports will be as described in the HA-88-3 instruction manual.

If two HA-88-3 boards are to be used in the Heartbeat, then one will be installed at P5Ø5/P511 on the right-hand side and one will be installed at P5Ø2/P5Ø8 on the left-hand side. In this case, the Heartbeat on-board serial port will not be usable and should be disabled by removing the "SA" jumper on the Heartbeat CPU board. Port assignments for the six serial ports on the two boards will be as follows. Bus signal definitions are given in parentheses. Refer to APPENDIX A for bus pin identification.

HA-88-3 Port Connector	Left-hand Bus (P5Ø2/P5Ø8)	Right-hand Bus (P5Ø5/P511)
P6Ø3	24Ø-247Q (TS3)	34Ø-347Q (I/O LP)
P6Ø4	22Ø-227Q (TS1)	32Ø-327Q (I/O SERLØ)
P6Ø5	23Ø-237Q (TS2)	33Ø-337Q (I/O SERL1)

The interface cables supplied with the HA-88-3 should be installed into any three of the rear-panel openings SR-2 through SR-8.

Z-89-11 Multi-function I/O Card

The Z-89-11 Multi-function I/O Card may be installed in the D-G Heartbeat at P5Ø5/P511 on the right-hand side of the CPU board or at P5Ø2/P5Ø8 on the left-hand side of the board. Normally the Z-89-11 will be installed at P5Ø5/P511. In this case, the "SA" jumper on the Heartbeat CPU board should be set to position "1". The Heartbeat on-board serial port will then be addressed at port TS1 (22Ø-227Q). Operation of the Z-89-11 interface ports will be as described in the Z-89-11 instruction manual.

The Z-89-11 board may also be used in a system containing an HA-88-3 Serial Interface Board or a second Z-89-11 board. In this case, the HA-88-3 or one of the Z-89-11 boards should be installed at P5Ø5/P511 on the right-hand side and a Z-89-11 should be installed at P5Ø2/P5Ø8 on the left-hand side of the board. The Heartbeat on-board serial port will not be usable in this system so it should be disabled by removing the "SA" jumper on the CPU board. Port assignments for the three available interfaces on the Z-89-11 will be as follows. Bus signal definitions are given in parentheses. Refer to APPENDIX A for bus pin identification.

Z-89-11 Port Connector	Left-hand Bus (P5Ø2/P5Ø8)	Right-hand Bus (P5Ø5/P511)
P6Ø3	24Ø-247Q (TS3)	34Ø-347Q (I/O LP)
P6Ø4	22Ø-227Q (TS1)	32Ø-327Q (I/O SERLØ)
P6Ø5	23Ø-237Q (TS2)	33Ø-337Q (I/O SERL1)

The interface cables supplied with the Z-89-11 should be installed into any three of the rear-panel openings SR-2 through SR-8.

Z89-37 Double Density Disk Controller

Installation of the Heath/Zenith Z89-37 Controller is as described on pages 7-13 of the Z89-37 installation instructions with the following exceptions:

A) No power supply modifications are required on the Heartbeat.

B) References to switch and jumper settings on the Heath/Zenith CPU board should be ignored.

C) The 2Ø-pin plug with jumper (supplied with the Z-89-37) should replace the 74LS24Ø at U38 on the Heartbeat CPU board.

D) The 16-conductor cable with connectors should plug into the socket at U5Ø on the Heartbeat CPU board.

E) The 47ØØ ohm resistor with connectors (discussed on Page 9 of the Z-89-37 Installation Instructions)is not required for any configuration of the Heartbeat.

Z89-47 Interface

Installation of the Heath/Zenith Z89-47 Disk Interface accessory is exactly as described on pages 3-6 of the Z89-47 installation manual.

Z-89-67 Interface

Installation of the Heath/Zenith Z-89-67 interface is as described on pages 8 and 9 of the Z-89-67 Interface Board Operation Manual with the following exceptions and comments.

A) Unless the Z-89-67 is installed in a system using the H-88-1 controller, the Z-89-67 should be installed at P5Ø6/P512 on the Heartbeat CPU board. The DC (Disk Clock) jumper should be set to the "2" position.

B) The PROM (Heath part #444-83) at U516 on the Heath/Zenith CPU board is not used on the Heartbeat.

C) References to switch and jumper settings on the Heath/Zenith CPU board should be ignored.

D) The 4Ø-pin ribbon connector coming from the interface board should be installed at FR-2 oon the Heartbeat rear panel.

NOTE: Some Heath software products may require patches for operation at 4 MHz. Refer to APPENDICES C and D for these patches.

The D-G Heartbeat With Non-Heath Peripherals

The following products are fully compatible with the D-G Heartbeat computer. Common jumper settings for these devices are given in the previous section on page 22. Switches S1 and S2 on the Heartbeat CPU board must be set as described in the "System Configuration Switches" section of this manual beginning on page 29.

C.D.R. Systems FDC-88ØH Floppy Disk Controller

The FDC-88ØH controller may be used with the D-G Heartbeat as follows.

A) The CDR-86 port decode PROM should be installed at U9 on the Heartbeat CPU board. This is accomplished by removing the four screws at the corners of the Heartbeat memory board and carefully removing the board from its socket. U9 is located at the left-hand side of the area covered by the memory board. You should be very careful when removing and re-installing the memory board to avoid bending or mis-aligning the memory board connectors.

B) The "E" jumper on the FDC-88ØH should be set from "E2" to "E3".

C) The FDC-88ØH controller should be installed at P5Ø4/P51Ø on the Heartbeat CPU board.

D) If you intend to use the Heath Disk Operating System (HDOS) you should use CDRDVD (c) from Livingston Logic Labs as your device driver.

Livingston Logic Labs
P.O. Box 5334
Pasadena, CA 911Ø7
213/3Ø3-5342 (5 PM to 8 PM)

E) If you intend to use the CP/M operating system you should use CDRBIOS (c) from Livingston Logic Labs.

Magnolia Microsystems
Floppy and Corvus Interface Boards

The DG Heartbeat provides full compatibility with the Magnolia Microsystems 8" Floppy Disk Controller and the Magnolia Microsystems Corvus Interface when used with MTR-S89. The user should refer to the appropriate Magnolia Microsystems installation manual for installation of these devices. The following will prove helpful during device installation.

A) When using the Magnolia Microsystems devices, the Magnolia port decode PROM (part number 444-61A, B or C) should be installed at U9 on the DG Heartbeat CPU board. This is accomplished by removing the four screws at the corners of the Heartbeat memory board and carefully unplugging the board from the main board. U9 is located at the left-hand side of the area covered by the memory board. You should be very careful when removing and reinstalling the memory board to avoid breaking or misaligning the pins of the memory board connectors.

B) The Magnolia Microsystems Floppy Disk Controller requires a connector to be plugged into the socket at U553 on the Heath/Zenith CPU board. This connector should be plugged into the socket at U39 on the DG Heartbeat CPU board.

C) If the DG Heartbeat alternate serial port is used in conjunction with Magnolia Microsystems devices requiring port decode PROM 444-61A, B or C, then the 'SA' jumper on the Heartbeat CPU board should be set to position '1'. The port will then be addressed at device select TS1. Refer to APPENDIX B of this manual for the port number corresponding to this device select signal.

D) Magnolia Microsystems CP/M Versions 2.23 and 2.24 require modification for proper operation in 4 MHz computer systems. Modification instructions are available from D-G Electronic Developments Company.

Additional Compatible Devices

In addition to the above products, any interface product designed to operate on the I/O Interface Bus (right-hand bus slots) of the Heath/Zenith 89/9Ø series computers should be operational in the D-G Heartbeat. Support software for these products may require minor modification if timing loops dependent on the Heath/Zenith CPU clock rate of 2 MHZ are used.

System Configuration Switches

Switches S1 and S2 on the D-G Heartbeat CPU board allow system configuration information to be provided to the system monitor for proper system initialization. Switch positions for S1 and S2 are defined as follows.

SWITCH S1:

Switch number 1 2 3 4 5 6 7 8	Description...
Ø	Normal monitor & boot operation.
1	Upon reset (at power-up or when the Heartbeat rear-panel 'RESET' button is pressed) a boot (called an "autoboot") is made from the default boot drive (see below),unit Ø.
. Ø	Terminal baud rate is 96ØØ.
. 1	Terminal baud rate determination is automatic. This option requires a VT-52 compatible terminal (H/Z-19, H/Z-29).
. . 1	Normal monitor operation.
. . Ø	Upon reset (at power-up or when the Heartbeat rear-panel 'RESET' button is pressed) the "dynamic RAM test" is performed.
. . . Ø . . .	Normal monitor operation. On boot, the lower 8K of ROM contents are moved to RAM; and, at a CPU speed of 4 MHz, constants in the H-88-1 support ROM area are modified for proper operation. On an HDOS restart, memory is remapped to all RAM.
. . . 1 . . .	The lower 8K ROM contents are not moved to RAM. If you use the H-88-1 disk controller at a CPU speed of 4 MHz, this setting requires that you use software which supports 4 MHz H-88-1 operation with an unmodified H-88-1 support ROM,

such as UltiMeth Corporation's DKH17V2.DVD device driver for HDOS, and Livingston Logic Labs' BIOS-8Ø for Heath CP/M. This setting must NOT be used if you use under HDOS a Livingston Logic Labs' 8" single density floppy controller or a CDR double density floppy controller.

Switch number 1 2 3 4 5 6 7 8	Description...
	THESE SETTINGS SELECT THE HEATH/ZENITH DEVICE LOCATED AT PORT Ø78H (17ØQ) AS FOLLOWS.
. . . . Ø Ø . .	Soft-sectored 5.25-inch disk (H/Z37)
. . . . Ø 1 . .	H/Z47
. . . . 1 Ø . .	H/Z67
. . . . 1 1 . .	No device
	THESE SETTINGS SELECT THE HEATH/ZENITH DEVICE LOCATED AT PORT Ø7CH (174Q) AS FOLLOWS.
. . . . . Ø Ø	Hard-sectored 5.25-inch disk (H-88-1)
. . . . . Ø 1	H/Z47
. . . . . 1 Ø	H/Z67
. . . . . 1 1	No device

SWITCH S2:

Switch number 1 2 3 4 5 6 7 8	Description...
n n n n	These switch sections define the current "year minus 1982" value in binary (e.g., ØØØØ for 1982, ØØØ1 for 1983, etc.). This value, along with other values from the Heartbeat real-time clock (which does not contain the year), are used by the monitor ROM and other code.

The following switch settings define the default boot device type. The device type identifier used in the "Boot" command is shown in "[ ]":

. . . . Ø Ø Ø Ø	[A]	H-88-1 hard-sectored 5" floppy, units Ø-2.
. . . . Ø Ø Ø 1	[B]	H/Z-37 soft-sectored 5" floppy, units Ø-3.
. . . . Ø Ø 1 Ø	[C]	Corvus hard disk/Magnolia interface, partitions Ø-8.
. . . . Ø Ø 1 1	[D]	CDR 5"/8" double density floppy, units Ø-3.
. . . . Ø 1 Ø Ø	[E]	H/Z-47 8" floppy at port 78H/17ØQ, units Ø-3.
. . . . Ø 1 Ø 1	[F]	H/Z-47 8" floppy at port 7CH/174Q, units Ø-3.
. . . . Ø 1 1 Ø	[G]	D-G SASI controller at port A8H/25ØQ, units Ø-7.
. . . . Ø 1 1 1	[H]	"HELP" device (null) - provides a "HELP" list of boot devices.

Switch number 1 2 3 4 5 6 7 8		Description...
. . . . 1 Ø Ø Ø		Reserved.
. . . . 1 Ø Ø 1	[J]	D-G SASI controller or H/Z-67 disk at port 78H/17ØQ, units Ø-7.
. . . . 1 Ø 1 Ø	[K]	D-G SASI controller or H/Z-67 disk at port 7CH/174Q, units Ø-7.
. . . . 1 Ø 1 1	[L]	Livingston 8" single density floppy, units Ø-3.
. . . . 1 1 Ø Ø	[M]	Magnolia 5"/8" double density floppy, units Ø-7.
. . . . 1 1 Ø 1		Reserved
. . . . 1 1 1 Ø		Reserved
. . . . 1 1 1 1	[P]	Pseudo disk using auxillary memory.

DISK DRIVE INSTALLATION

The D-G Heartbeat disk drive "tray" is designed to accommodate one full-size 5 1/4" disk drive or two "half-height" 5 1/4" drives. All jumpers and switches on the Heartbeat CPU board should be set before installing the disk drive(s). Once switches and jumpers are set, the drives may be mounted using the mounting holes on the sides of the disk drive tray. Each drive should be secured using four screws. Note that if two half-height drives are being installed, the lower disk drive must be configured before installing the upper drive. Refer to the manuals supplied with your disk drives and disk controller for disk drive configuration.

Terminal Considerations

The Heartbeat computer may be used with any standard RS-232 compatible video terminal. If the terminal is Digital Equipment Corporation VT-52 compatible (H/Z19, H/Z29, ZT-1,1Ø,11), Switch S1 position "2" on the Heartbeat CPU board may be set to "1" to provide automatic determination of the terminal baud rate on system power-up. Acceptable terminal baud rates are 12ØØ, 24ØØ, 48ØØ, 96ØØ, 192ØØ and 384ØØ. If your video terminal is not VT-52 compatible, then Switch 1, position "2" should be set to "Ø" and the video terminal set for a baud rate of 96ØØ.

***** HEARTBEAT JUMPER DESCRIPTIONS *****

The various jumper options available on the Heartbeat are described below. Options which may be frequently changed are selected by solderless jumper shunts. All other options are selected by soldered jumpers. Refer to FIGURE 2, page 24 for jumper locations.

CLOCK OPTIONS

SC — **System Clock** - This jumper allows selection of the CPU clock frequency. This frequency may be either 2.Ø48 (SC jumper in the "2" position) or 4.Ø96 MHz (jumper in the "4" position).

MSA,MSB — **MilliSecond interrupt interval**- The millisecond interrupt interval may be selected by use of these two jumpers. Available interrupt intervals are as follows:

MSA	MSB	INTERRUPT RATE
1	1	Ø.5 MS
2	1	2.Ø MS
3	1	4.Ø MS
4	1	8.Ø MS
1	5	2.5 MS
2	5	1Ø.Ø MS
3	5	2Ø.Ø MS
4	5	4Ø.Ø MS

The factory setting for these two jumpers is be MSA = 2 and MSB = 1 thus providing a 2ms interrupt interval.

AC — **Arithmetic processor Clock** - The AM9511 Arithmetic Processor clock may be set to either 2 or 4 MHz using this jumper. This allows for the use of the lower cost version of the AM9511 without sacrificing overall system speed.

DC — **H88 Disk Clock** - When set to the "2" position this jumper allows 2 MHz to be supplied to P512 pin 13 at all times. This maintains compatibility with the H-88-1 disk controller at CPU clock frequencies of 2 or 4 MHz.

W — **Wait** - When this jumper is shorted, one "wait state" is inserted on each ROM access cycle. No wait states are inserted on RAM access cycles. This allows slow ROM's or EPROM's to be used without limiting overall system speed.

GENERAL PURPOSE SERIAL PORT OPTIONS

SA — **Serial Address** - This jumper allows the general purpose serial port to be addressed at the following device select ports.

SA	PORT NAME
1	TS1
2	I/O SERL Ø
3	I/O SERL 1
4	I/O LP

The I/O port values for these device select signals may be found in APPENDIX B on page 59 of this manual.

SI — **Serial Interrupt** - The general purpose serial port may be tied to either interrupt level 3, 4 or 5.

INTERRUPT OPTIONS

PRIMARY JUMPER BLOCK

The primary interrupt jumper block is located at the bottom center of the board. This jumper block allows the three left-hand bus interrupt lines (bus pins 18, 19 and 2Ø) as well as either the arithmetic processor or the real-time clock to be tied to any of the available interrupt levels (Ø through 7). Note that if these interrupt signals are used, support for them must be provided through software. The center row of the five rows of pins in this jumper block is the "common" row. Thus pins 19 and 2Ø of the left-hand bus would be connected to the desired interrupt level by use of a Ø.1 inch jumper and pin 18 and/or the real-time clock or arithmetic processor would be connected using a Ø.2 inch jumper.

AP/CK

This jumper, located to the right of the primary jumper block allows either the arithmetic processor (AP) or the real-time clock (CK) to be connected to the top row of pins on the primary interrupt jumper block. This allows either of these devices to be connected for use in the interrupt mode.

ROM JUMPER OPTIONS

The Heartbeat provides two ROM sockets (U36 and U37) allowing up to 16K of ROM storage. Jumpers J1, J2, J3 and RSP are used to configure the system for the various ROM's, EPROM'S and RAM's that may be used.

J1 This jumper allows either +12 volts (V_{dd}) or address line A1Ø to be tied to pin 19 of the memory device at U37. The factory setting for this jumper is "A".

J2 This jumper allows either the chip select signal (designated as C on the board) or address line A1Ø (A) to be tied to pin 2Ø of the memory device at U37. The factory setting for this jumper is "C".

J3 This set of jumpers allows pins 18 and 21 of both U36 and U37 to be properly configured. Pin 18 of either or both devices may be tied to either the chip select signal (CS) or address line A11. U36, pin 21 may be tied to either address line A11 or address line A12 while U37, pin 21 may be tied to any one of the signals CS, A11, A12, Write (W) or -5 volts (V_{bb}).

RSP ROM SPace - These jumpers assign the ROM sockets to the appropriate portion of the system memory space. The ROM device at U36 will always occupy the address space from ØK up to 4K. This is because U36 must always be a 4K byte or larger device. If an 8K byte ROM were used at U36, then the "4" and "6" sections of the RSP jumper should be set to the "36" position.

OTHER JUMPER OPTIONS

X This jumper allows an alternate PROM device to be used as the device decoder at U8. In normal operation, a jumper is soldered at this position.

Y When this jumper is connected, a non-maskable interrupt will be generated each time the system memory bank-select ports are accessed. This option may be used to provide a user access authorization check in multi-user systems. Note that if this option is used, software support must be provided by the operating system. In normal operation, a jumper should not be installed at this position.

Z **Return-to-ROM on NMI** - If this jumper is installed each non-maskable interrupt request will cause the system ROM to be turned on so that the NMI handling routine is located at its proper address location, 66H. This allows the NMI function to be used with operating systems such as CP/M which are not designed to support its use. The ROM may be turned back off by first "enabling" it through port 362Q and then disabling through that same port. This jumper is installed as shipped from the factory.

***** Advanced Features *****

The following advanced hardware features are provided for the use of the sophisticated user. Note that several of these features require software and/or firmware support which is not provided at this time by DG Electronic Developments Co..

System Clock Frequency

The Heartbeat is designed to operate at system clock frequencies of 2.Ø48 MHz or 4.Ø96 MHz. This selection is made by use of the "SC" (System Clock) jumper located on the lower left-hand side of the Heartbeat main board. If the system is to be operated at 4.Ø96 MHz, some software products may require patches for proper operation. These patches will usually be applied with the "SC" jumper in the "2" (2.Ø48 MHz) position. Refer to APPENDIX C for HDOS products requiring patches and APPENDIX D for CP/M products.

Clock Interrupts

The clock interrupt interval of the Heartbeat computer is set to be 2 ms for compatibility with Heath/Zenith 89/9Ø series computers. Optional interrupt intervals are available ranging from Ø.5 ms up to 4Ø ms. These time intervals are set by use of the MSA and MSB jumpers described in the Heartbeat Jumper Options section of this manual. Since many Heath hardware and software products depend on the 2 ms clock interrupt, this value should not be changed except for special applications.

NMI Generation

A non-maskable interrupt may occur on the Heartbeat for any of the following reasons.

1) Memory parity error

2) Attempted access of Heath PAM-8 I/O port - This NMI is used by some Heath software products to allow use of the same software package on both the Heath H8 computer and Heath/Zenith 89-9Ø series computers.

3) Attempted access of the bank select port ("Y" jumper must be installed for this NMI to occur.

Support for these possible NMI events is provided by the MTR-S89 monitor ROM as follows. If (1) occurs, a parity error message will be printed on the console and normal system operation will be suspended. If (2) occurs, the standard monitor NMI handling routine will process the NMI request. No support is presently provided for option (3) and thus it will be ignored by the system.

Parity Detection

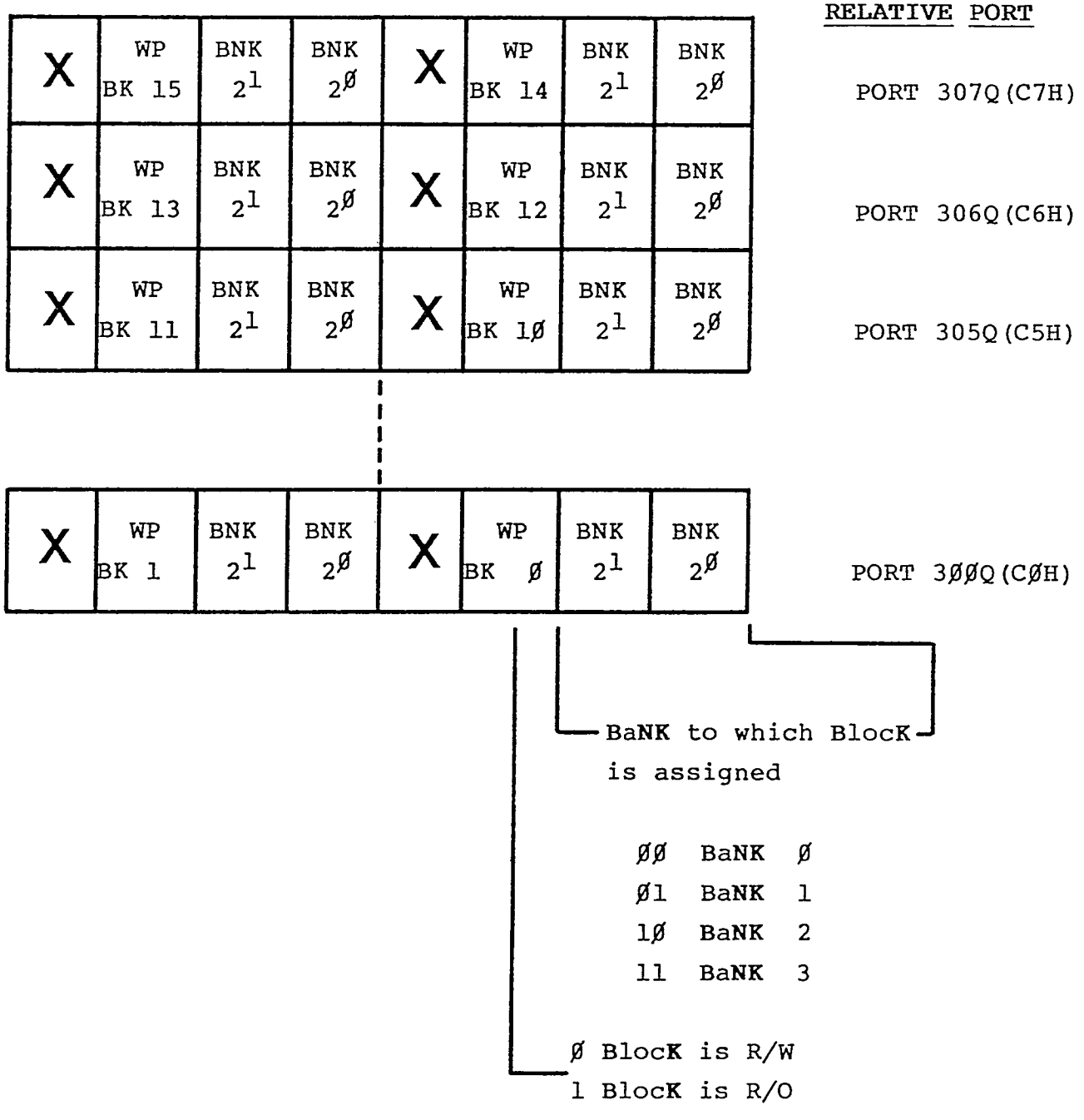
The Heartbeat provides a "parity check" on all RAM access operations. This feature allows most system memory failures to be detected thus minimizing unexplained "system crashes". When a memory failure occurs, the message "***RAM parity stop***" will be printed on the console and normal system operation will be suspended. You should at this point refer to the "Check RAM" procedure and run this memory test to determine the nature of the memory problem.

SUPER 89 BANK-SELECT DESCRIPTION

The total RAM capacity of the SUPER 89 is 256K bytes. This RAM is divided into four 64K byte BANKS which may be enabled in 4K byte increments (BLOCKS). This division of memory is shown in the figure below:

BANK Ø	BANK 1	BANK 2	BANK 3
BLOCK 15	BLOCK 15	BLOCK 15	BLOCK 15
BLOCK 14	BLOCK 14	BLOCK 14	BLOCK 14
BLOCK 13	BLOCK 13	BLOCK 13	BLOCK 13
BLOCK 12	BLOCK 12	BLOCK 12	BLOCK 12
BLOCK 11	BLOCK 11	BLOCK 11	BLOCK 11
BLOCK 1Ø	BLOCK 1Ø	BLOCK 1Ø	BLOCK 1Ø
BLOCK 9	BLOCK 9	BLOCK 9	BLOCK 9
BLOCK 8	BLOCK 8	BLOCK 8	BLOCK 8
BLOCK 7	BLOCK 7	BLOCK 7	BLOCK 7
BLOCK 6	BLOCK 6	BLOCK 6	BLOCK 6
BLOCK 5	BLOCK 5	BLOCK 5	BLOCK 5
BLOCK 4	BLOCK 4	BLOCK 4	BLOCK 4
BLOCK 3	BLOCK 3	BLOCK 3	BLOCK 3
BLOCK 2	BLOCK 2	BLOCK 2	BLOCK 2
BLOCK 1	BLOCK 1	BLOCK 1	BLOCK 1
BLOCK Ø	BLOCK Ø	BLOCK Ø	BLOCK Ø

Blocks of memory are assigned to the CPU's memory space by writing a control word to each of the 8 bank-select ports. Each block may come from Bank Ø through 3 and each control word controls the assignment of two blocks. The format of the control word is shown in the diagram below.



Each active block of memory may be write protected (R/O) or may be Read/Write (R/W). Care should be taken not to write protect

dynamic areas of memory such as stack areas or "scratch pad" status areas. Note that the bank-select port may be written to or read from so that current status is easily available.

***** Heartbeat Technical Overview *****

The "heart" of the D-G Heartbeat computer is the D-G SUPER 89 single-board computer. This board is designed around the industry-standard 4 MHZ Z8Ø microprocessor. Two 24 pin ROM sockets provide for up to 16 Kbytes of system firmware which may be disabled under software control.

System RAM is provided on a removable memory card with a maximum capacity of 256 Kbytes. Memory devices used are Motorola MCM6665AL2Ø 64K RAM's or equivalent. Parity generation and checking of the RAM is provided by a 74LS28Ø parity generator/checker. The total 256 Kbytes of RAM is divided into four 64 Kbyte banks which may be assigned to the active memory space in 4 Kbyte increments.

Two INS825Ø ACE devices provide the RS-232 serial ports. An on-board oscillator is used to generate the BAUD-rate clock for these ACE's as well as serial interface devices plugged into the I/O expansion slots.

I/O expansion is provided by five Heath/Zenith compatible expansion connectors. Each bus consists of the eight data lines, four pre-decoded I/O select signals, address lines AØ -> A3 for on-board decoding, system and serial I/O clocks, read and write strobes, wait request, three interrupt request inputs, system reset, two status lines and peripheral power and ground. I/O decoding for the expansion bus is provided by two TBP28L22 PROM's on the SUPER 89 and is easily modified by PROM replacement.

A MM58174 Real-time Clock is used for clock/calendar functions on the SUPER 89 board. This CMOS device provides its own crystal controlled clock so that its operation is independent of the CPU clock. A connector on the board allows a small battery pack to maintain time-keeping functions during system power-down.

A socket is provided on the board for the use of an AM9511 Arithmetic Processor. A jumper allows for the use of either a 4 MHZ 9511 or the lower cost 2 MHZ version of the device.

On power-up or reset, the monitor measures the processing speed of the CPU and also determines the baud rate of the terminal (the determination of baud rate may cause "garbage" characters to be displayed briefly; and on power-up may take up to one second). The monitor can detect a terminal set to any of the following baud rates:

12ØØ 24ØØ 48ØØ 96ØØ 192ØØ 384ØØ

The CPU-terminal interface is initialized and the processing speed of the CPU is displayed. The monitor then determines which banks of memory are installed. For each bank of RAM memory detected, the monitor forces correct parity for each byte of RAM, and displays a message and "beep" for each bank that has been validated. The time it takes to validate RAM memory depends on the CPU speed, the number of banks of memory, and whether RAM has correct parity. Validation takes longer on power-up due to the random state of memory parity after power-off.

The user program counter (PC) and stack pointer (SP) are set to FFFØ (hexadecimal). You may use the first 1Ø bytes of this area for a "JMP" instruction and/or other data. For example, if you have Org-Ø CP/M, you could modify your BIOS cold start routine to place there a JMP to the warm start routine (make sure that the warm start routine remaps memory to all RAM, and reinitializes any serial ports used). Then, a reset followed by the monitor "G(o)" command (with no address) performs a CP/M warm start.

The following routine entry points in the Heath MTR-88, -89 and -9Ø ROMs have been preserved at their original locations. Note that only the function of the routine has been preserved; the code may have changed. The routines have been preserved only to allow compatibility with existing programs; it is strongly recommended that you do not write code that references these routines, as Heath, UltiMeth, or D-G Electronic Developments Co. may not provide them in future ROMs. The TYPMSG routine now stops on either a null character or a character with the high-order bit on.

Heath routine name	Location	
DLY	ØØ2B	ØØØ.Ø53
INTXIT	ØØ7A	ØØØ.172
PIN	Ø137	ØØ1.Ø67
ALARM	Ø25E	ØØ2.136
HORN	Ø26Ø	ØØ2.14Ø
IOA	Ø332	ØØ3.Ø62
IOB	Ø336	ØØ3.Ø66
RCC	Ø3B2	ØØ3.262
WCC	Ø3C2	ØØ3.3Ø2
DAT	Ø613	ØØ6.Ø23
COM	Ø617	ØØ6.Ø27
TYPMSG	Ø64Ø	ØØ6.1ØØ

The following RAM locations are used or reserved by the monitor ROM.

Heath location name	Location(s)	
(reserved)	2ØØØ-2ØØ7	Ø4Ø.ØØØ-Ø4Ø.ØØ7
.MFLAG	2ØØ8	Ø4Ø.Ø1Ø
CTLFLG	2ØØ9	Ø4Ø.Ø11
(reserved)	2ØØA-2Ø1A	Ø4Ø.Ø12-Ø4Ø.Ø32
TICCNT	2Ø1B-2Ø1E	Ø4Ø.Ø33-Ø4Ø.Ø36
UIVEC	2Ø1F-2Ø33	Ø4Ø.Ø37-Ø4Ø.Ø63
(reserved)	2Ø34-2Ø3F	Ø4Ø.Ø64-Ø4Ø.Ø77

.MFLAG

The default value for this byte is zero.

If bit Ø is set, the monitor will CALL the instruction at UIVEC on each clock interrupt with all interrupts disabled; return should be made TO THE MONITOR via the "RET" instruction without enabling interrupts. After the CALL, the stack contains, in ascending order, the following items (note that this list is the same as Heath's list):

(SP+Ø) = Return location in the monitor.
(SP+2) = Stack pointer value at time of interrupt.
(SP+4) = Program status word (register AF).

(SP+6) = Register BC.
(SP+8) = Register DE.
(SP+1Ø) = Register HL.
(SP+12) = Register PC.

Note that HDOS supplies a JMP to its own clock interrupt processing routine (bit Ø is set during HDOS operation); this routine is critical to the proper operation of the mini-floppy disks.

If bit 7 is set, the monitor will not attempt to detect a halt condition (bit 7 is set during HDOS operation). If bit 7 is not set, the clock interrupt routine checks the last byte of the last instruction executed prior to each clock interrupt. If the operation code value for a "HLT" instruction is found, the monitor regains control and displays the following:

```
[Halt]
XX=nnnn af=nnnn bc=nnnn de=nnnn hl=nnnn YY=nnnn
SP=nnnn AF=nnnn BC=nnnn DE=nnnn HL=nnnn PC=xxxx => bb bb ...
```

Note that "xxxx" is the current PC register value, which is the location of the "HLT" operation code value plus one. Note that many multiple-byte instructions could have the last byte of the instruction look like a "HLT" operation code, so the monitor may falsely detect a halt condition when none exists (which is why Heath provided bit 7 of .MFLAG to disable this feature under HDOS).

CTLFLG

This byte should reflect the current value output to port FØ (hexadecimal) or 36Ø (octal). Since this port exists only on an H8, and not on an H89 or SUPER-89, the SUPER-89 hardware causes a Z-8Ø non-maskable interrupt to be generated whenever a reference is made to an H8 port address. The monitor ROM intercepts the non-maskable interrupt and, if an 8Ø8Ø "OUT" instruction reference to port FØ (hexadecimal) caused the non-maskable interrupt, the monitor changes the format of the output value to the corresponding H89 value, and outputs the value to port F2 (hexa-

decimal). (Note that the monitor "I(n)" and "O(ut)" commands use Z-8Ø input and output instructions, and thus produce meaningless results when used to reference H8 port addresses.)

User programs needing to output to port FØ (hexadecimal) should disable interrupts, get the current value of CTLFLG, alter bits 4 and\or 6 as desired, store the new value in CTLFLG, then output to the port, and then enable interrupts.

If bit 4 is set, the single step interrupt feature is disabled (the default). If bit 4 is reset, the single step feature is enabled. When the single step interrupt occurs, the monitor will JMP to the instruction at UIVEC+3 with interrupts disabled; the return to the point of interrupt is the responsibility of the user program. After the JMP, the stack contains, in ascending order, the following items (note that this list is the same as Heath's list).

(SP+Ø) = Stack pointer value at time of interrupt.
(SP+2) = Program status word (register AF).
(SP+4) = Register BC.
(SP+6) = Register DE.
(SP+8) = Register HL.
(SP+1Ø) = Interrupt return location (register PC).

Bit 6 is set to enable clock interrupts (the default). You should note that HDOS requires clock interrupts to be enabled (see above under .MFLAG).

TICCNT

This 4-byte area contains a 32-bit binary value which is incremented on every clock interrupt (every 2 milliseconds). TICCNT contains the lowest-order byte, and TICCNT+3 contains the highest-order byte. The two high-order bytes have been added to Heath's TICCNT to allow the value in TICCNT to represent more than 24 hours. HDOS disk I/O operations disable interrupts for periods exceeding 2 ms causing clock interrupts to be delayed; thus, TICCNT cannot be used as a highly accurate 24-hour clock.

UIVEC

This 21-byte area reserves a 3-byte instruction area for each possible user interrupt (1 to 7); user interrupts "1" and "2" are the clock and single step interrupts, respectively, and are discussed above under "MFLAG" and "CTLFLG". User interrupts "3" through "7" cause the monitor to JMP directly to the following entry in UIVEC with interrupts disabled.

Interrupt number	JMP location
3	UIVEC+6
4	UIVEC+9
5	UIVEC+12
6	UIVEC+15
7	UIVEC+18

After the JMP, the stack contains only the interrupt return location. The user interrupt routine must save and restore any registers it uses, and must enable interrupts before returning to the point of interrupt. Note that HDOS uses interrupt "3" (for console I/O) and "7" (for SCALLs).

AM9511/8231 ARITHMETIC PROCESSOR INSTALLATION

The Advanced Micro Devices AM9511 or Intel 8231 arithmetic processor may be installed on the SUPER 89 as follows.

1) Remove the internal disk drives and the disk drive tray from the heartbeat mainframe.

2) Remove the four screws at the corners of the Heartbeat memory card and carefully remove this card from the main board.

3) Install the arithmetic processor integrated circuit at U5 on the Heartbeat. Be very careful that the leads are straight and that the pin-1 end of the IC (denoted by a notch) is toward the top of the CPU board.

4) Re-install the memory card making sure that the connectors at the left of the board are properly engaged. Do not over-tighten the mounting screws.

5) If your arithmetic processor is an AMD AM9511A-4DC or an Intel 8231A, the AC jumper on the Heartbeat CPU board should be set to the "4" position. If your processor is an AMD AM9511ADC or AM9511A-1DC or an Intel 8231A-3 or 8231A-8 then the AC jumper should be set to the "2" position.

The data port of the arithmetic processor will be addressed at I/O port 274Q and the command port will be at I/O port 275Q.

MEMORY EXPANSION

The Heartbeat memory card allows for up to 256K bytes of bank selectable RAM. Each bank requires nine 64K RAM devices (eight data bits and one parity bit). RAM devices used must be of the 7-bit refresh (128 refresh cycles each 2 milliseconds) type and have a speed of 2ØØ nanoseconds or less. Suitable devices include the following.

Motorola	MCM6665AL2Ø
Motorola	MCM6665AL15
Fujitsu	MB8264-2Ø
Fujitsu	MB8264-15
NEC	UPD4164-2
NEC	UPD4164-3
Hitachi	HM4864-3
Hitachi	HM4864-2
Mostek	MK4564N-2Ø
Mostek	MK4564N-15
OKI	M3764-2Ø
OKI	M3764-15
Mitsubishi	M5K4164NS-2Ø
Mitsubishi	M5K4164NS-15

RAM devices should be installed with the pin-1 end of the device toward the top of the memory card.

Real-Time Clock Adjustment

The real-time clock may be adjusted by use of capacitor C1 on the lower right-hand side of the Heartbeat main board. It is strongly recommended that this adjustment be made with the computer power switch turned off. Turn the capacitor adjustment screw a small amount (less than one-eighth turn) and then power-up the computer. Monitor the time for a few minutes or hours to determine if the clock is maintaining the correct time. If further adjustment is necessary, again turn off the computer before attempting this adjustment.

Real-Time Clock Battery Backup

Battery backup may be provided to the Real-Time Clock using 3-pin connector P518. This connector is located in the lower right-hand corner of the board between IC's U55 and U56. A three pin connector shell should be wired such that the center conductor is the positive (+) supply voltage and either outside conductor is the negative (-) side of the battery pack. Battery pack voltage should be in the range of 3 VDC to 3.6 VDC.

****

WARNING: UNDER NO CIRCUMSTANCES SHOULD THE BATTERY PACK VOLTAGE EXCEED 3.6 VOLTS DC.

****

***** APPENDIX A: HEARTBEAT BUS DEFINITIONS *****

P5Ø1 > P5Ø6:

BUS PIN	SIGNAL DESCRIPTION	
	LEFT-HAND BUS	RIGHT-HAND BUS
1	GND	GND
2	DØ	DØ
3	D1	D1
4	D2	D2
5	D3	D3
6	D4	D4
7	D5	D5
8	D6	D6
9	D7	D7
1Ø	GND	GND

P5Ø7 > P512:

BUS PIN	SIGNAL DESCRIPTION	
	LEFT-HAND BUS	RIGHT-HAND BUS
1	+5V	+5V
2	GND	GND
3	AØ	AØ
4	A1	A1
5	A2	A2
6	BRD	BRD
7	BWR	BWR
8	WAIT	WAIT
9	TS1	I/O SERL Ø
1Ø	TS2	I/O SERL 1
11	TS3 (NOTE 1)	I/O LP (NOTE 2)
12	DS1	I/O FLPYØ (NOTE 3)
13	Ē	Ē (NOTE 4)
14	1.8432 MHZ	1.8432 MHZ
15	RESET	RESET

16	I/O 2	I/O Ø
17	I/O 3	I/O 1

BUS PIN	SIGNAL DESCRIPTION	
	LEFT-HAND BUS	RIGHT-HAND BUS
18	INT A	INT 3
19	INT B	INT 4
2Ø	INT C	INT 5
21	+12V	+12V
22	-12V	-12V
23	+5V	+5V
24	+12V	+12V
25	GND	GND

NOTES

1) P5Ø7 pin 11 is tied to the device select signal TS3. P5Ø8 and P5Ø9 pin 11 are tied to the device select signal DS2.

2) P51Ø and P511 pin 11 are tied to the device select signal I/O LP. P512 pin 11 is tied to the device select signal I/O FLPY1.

3) P51Ø and P511 pin 12 are tied to the device select signal I/O FLPYØ. P512 pin 12 is not connected.

4) P51Ø and P511 pin 13 are always tied to the system clock frequency, I. P512 pin 13 may be tied to either 2 or 4 MHz using jumper "DC". This allows for operation of the H88 disk controller at either 2 or 4 MHz.

5) I/O port assignments for the device select signals listed above may be found in the "I/O PORT ASSIGNMENTS" section of this manual.

***** APPENDIX B: HEARTBEAT I/O PORT ASSIGNMENTS *****

I/O port assignments for the SUPER 89 port decode PROM used at U8 are as follows.

SP-3ØØ

	OCTAL	HEX
BANK SELECT (8 PORTS)	3ØØ->3Ø7	CØ->C7
REAL-TIME CLOCK (LOWER FOUR BITS OF 16 PORTS)	2ØØ->217	8Ø->8F
SYSTEM STATUS PORTS		
DIP SWITCH S2 SECTIONS 1->4		
UPPER FOUR BITS OF PORT	2Ø1	81
DIP SWITCH S2 SECTIONS 5->8		
UPPER FOUR BITS OF PORT	2ØØ	8Ø
NMI STATUS		
UPPER THREE BITS OF PORT	2Ø2	82
AM9511 ARITHMETIC PROCESSOR		
DATA PORT	274	BC
COMMAND PORT	275	BD
LEFT-HAND BUS DEVICE SELECT PORTS:		
TS1 (8 PORTS)	22Ø->227	9Ø->97
TS2 (8 PORTS)	23Ø->237	98->9F
TS3 (8 PORTS)	24Ø->247	AØ->A7
DS1 (8 PORTS)	25Ø->257	A8->AF
DS2 (8 PORTS)	26Ø->267	BØ->B7

I/O port assignments for the port decode PROM used at U9 are as follows:

		444-61
I/O SERLØ	32Ø->327	DØ->D7
I/O SERL1	33Ø->337	D8->DF
I/O LP	34Ø->347	EØ->E7
I/O FLPYØ	17Ø->173	78->7B
I/O FLPY1	174->177	7C->7F

H47 Device Driver 4MHz Patch

The following procedure may be used to modify the standard Heath/Zenith H47 device driver so that it will function properly in systems whose clock speed is set at 4 MHz.

NOTE: This patch should be applied with the system clock (SC) jumper set to 2 MHz.

There are TWO versions of the patch provided here. The first is for the version of the device driver distributed on the HDOS 2.Ø distribution media (p/n 89Ø-64 or 89Ø-1Ø5). The second version is for the revised HDOS driver distributed with the HDOS 2.Ø New Product Update (p/n 89Ø-222).

If the values shown here do not match your values, **DO NOT APPLY THIS PATCH**. These patches have been written for standard Heath drivers. Operation is not guaranteed with custom drivers.

==========

This patch is for the HDOS Distribution version driver.

==========

```
>PATCH  <CR>

PATCH Issue #5Ø.Ø6.ØØ.

File Name?  SY.DVD  <CR>
Patch ID?  IFOJIC  <CR>
Prerequisite Code?  IFBEIADPGEFFCF  <CR>
Address?  ØØ312Ø  <CR>
ØØ312Ø = Ø4Ø/2ØØ  <CR>
ØØ3121 = 247/ <CTRL/D>
Address?  <CTRL/D>
Patch Check Code?  MFBHIADO  <CR>

PATCH Issue #5Ø.Ø6.ØØ.
```

```
File Name?  <CTRL/D>

>

================================================================
      This patch is for the HDOS New Product Update Driver.
================================================================

>PATCH  <CR>

PATCH Issue #5Ø.Ø6.ØØ.

File Name?  SY.DVD  <CR>
Patch ID?  IEGJIH  <CR>
Prerequisite Code?  IFBEIADPGEFFCF  <CR>

Address?  ØØ3161  <CR>
ØØ3161 = Ø4Ø/2ØØ  <CR>
ØØ3162 = 247/ <CTRL/D>
Address?  <CTRL/D>
Patch Check Code?  FBBFPIDI  <CR>

Patch Issue #5Ø.Ø6.ØØ.

File Name?  <CTRL/D>

>
```

***** APPENDIX D: CP/M SYSTEM PATCHES *****

If the Heath/Zenith H77/H-88-1 disk system is used with the Heartbeat at a system clock frequency of 4 MHz, patches will be required for Heath/Zenith CP/M 2.2.Ø3. These patches are available from D-G Electronic Developments Company.

***** APPENDIX E: THE ELECTRONIC DISK *****

DG-BIOS-Ø3
Version 1.Ø2

For Heath Bios 2.2.Ø3

This modification procedure will modify the BIOS.ASM that Heath and Zenith supply with their version 2.2.Ø3 of the CP/M operating system. The modifications will support the DG Electronic Disk, the Heartbeat real time clock and 4 MHz operation of the H77/H-88-1 hard-sector disk system.

The following files are contained on your distribution diskette:

SUBPATCH.SUB	BIOSØ31Ø.LIB
BIOSØ317.SUB	BIOSØ311.LIB
CHANGEMB.SUB	BIOSØ312.LIB
BIOSØ337.SUB	BIOSØ313.LIB
BIOSØ3Ø1.LIB	BIOSØ314.LIB
BIOSØ3Ø2.LIB	BIOSØ315.LIB
BIOSØ3Ø3.LIB	TIME.COM
BIOSØ3Ø4.LIB	TIME.MAC
BIOSØ3Ø5.LIB	CLOCK.COM
BIOSØ3Ø6.LIB	CLOCK.MAC
BIOSØ3Ø7.LIB	DGCONFIG.LOG
BIOSØ3Ø8.LIB	DGCONFIG.SUB
BIOSØ3Ø9.LIB	

SUBPATCH.SUB will patch the submit program to allow use of control characters.

BIOSØ317.SUB will produce the new BIOS.ASM source file on 5.25" hard sector (H77) drives. You should rename BIOSØ317.SUB to BIOSØ3.SUB if you intend to use an H77 drive system to perform the modifications.

BIOSØ337.SUB will produce the new BIOS.ASM source file for Z37, H/Z47, and Z67 disk drives. You should rename BIOSØ337.SUB to BIOSØ3.SUB if you intend to use one of these systems to perform the modification procedure. If you use BIOSØ337.SUB you will be using only a two drive system. Change all references from drive C: to drive B: in the following procedure.

CHANGEMB.SUB will produce a modified MAKEBIOS.SUB routine that will allow the proper functioning of the MAKEBIOS procedure on 5.25" hard sector (H77) drives.

The files BIOSØ3Ø1.LIB through BIOSØ315.LIB are library routines used by the BIOSØ3.SUB submit file. The files CLOCK.MAC, CLOCK.COM, TIME.MAC, and TIME.COM are programs that give an example of how to use the real time clock. DGCONFIG.SUB is a submit file which patches the Heath/Zenith "CONFIGUR.COM" file so that it will recognize the electronic disk as a valid device. DGCONFIG.LOG shows what is supposed to appear on your screen during DGCONFIG.SUB execution.

PRELIMINARY PREPARATION

The file BIOSØ3Ø2.LIB contains the declarations and values for switches DGEDK (the DG Electronic Disk), DG4MHz (optional 4 MHz operation), and DGRTC (the DG Real Time Clock). These switches are set to TRUE. If you wish to omit any of these functions you must first edit this file and set the equivalent switch to FALSE.

If you incorporate the electronic disk you may need to edit the file BIOSØ3Ø4.LIB. You should alter the value of BANKCT which is used to determine how many banks you have. If you have 128K of memory this value should be "1". For 192K of memory this value should be "2", and for 256K of memory this value should be "3". Modifications may be performed on the library routines with a text editor. The default value set in this file for BANKCT is 1. These instructions should be followed exactly to be sure the modification will be done correctly.

BEFORE PROCEEDING BE SURE THAT YOU HAVE SET ALL OF THE VALUES IN THE LIBRARY ROUTINES AS DISCUSSED IN THE PREVIOUS PARAGRAPHS. ALSO BE SURE THAT YOU HAVE NAMED EITHER BIOSØ337.SUB OR BIOSØ317.SUB TO BIOSØ3.SUB. IF YOU ARE USING A 5.25" HARD SECTOR DISK SYSTEM AT 4 MHZ TO PERFORM THE PROCEDURES BE SURE FORMAT.COM AND MOVCPM17.COM HAVE BEEN MODIFIED FOR 4 MHZ OPERATION. THE MODIFICATION PROCEDURE FOR THESE UTILITIES IS AVAILABLE FROM D-G ELECTRONIC DEVELOPMENTS COMPANY.

1) Format three (3) disks. Mark them "A", "B", and "C".

2) Sysgen the "A" disk and put a configured "BIOS" on it. It is important that this BIOS be properly configured for the number of drives in the system on which you are performing the installation procedure.

3) Copy the following files onto your disk labeled "A".

From your Heath/Zenith CP/M distribution disk

BIOS.ASM

From your DG-BIOS-Ø3 distribution disk.

All of the BIOSØ3xx.LIB files.

4) Copy the following files to your disk labeled "B"

From your Heath/Zenith CP/M distribution disk

SUBMIT.COM
XSUB.COM
ED.COM
STAT.COM
DDT.COM
ASM.COM

From the DG-BIOS-Ø3 distribution disk

SUBPATCH.SUB
BIOSØ3.SUB

NOTE: If you have less than a three drive H77 system, you must monitor the procedure and put the disks in the drives specified when the procedure prompts you. When this procedure is complete you will have a new BIOS source file on the disk labeled "C". References made to drive C: pertain only to a 3 drive 5.25" hard sector drive system.

5) Reboot your SUPER 89 from disk "A" on drive A:. The disk marked "A" will always be on drive A:, the disk marked "B" will always be on drive B:, and the disk marked "C" will always be on drive C:.

6) Type B:SUBMIT B:SUBPATCH to patch the submit program to allow the use of control characters. If your version of SUBMIT has already been patched, you can skip this step, however, no harm will come if you patch it again.

7) Type B:SUBMIT B:BIOSØ3 to build the new BIOS source file. This procedure will use all three disk drives (A:,B:, and C:) if you are using a three drive H77 system or drives A: and B: of a Z37, H/Z47 or Z67 system. When the procedure is complete you will have a new BIOS source file on disk "C" of an H77 system or disk "B" of other systems. At this time you could make any additional changes to the new BIOS source file, BIOS.ASM.

NOTE: If your system incorporates only 5.25" hard sector disk drives (H77) perform the procedure as outlined in step 8A. If you are using any other disk system proceed to step 8B.

8A) Place the MAKEBIOS, SUBMIT and all associated routines (MAKEBIOS.SUB, MAKEBIOS.COM, XSUB.COM,PREL.COM, ASM.COM and SUBMIT.COM) on a disk in drive A: along with ED.COM and CHANGEMB.SUB and type:

SUBMIT CHANGEMB

After this routine has been performed (DO NOT PERFORM THIS PROCEDURE MORE THAN ONCE) place the "C" disk with your new BIOS.ASM file that you just made in drive B:. Type the following command:

SUBMIT MAKEBIOS A:NEWBIOS B:

This will place "NEWBIOS" on drive A: which will be used to generate your new BIOS.SYS. You may then proceed with the MOVCPM17 and SYSGEN procedures.

8B) Follow the MAKEBIOS procedure to build a new BIOS.SYS file from your source file as documented in your manual from Heath/Zenith. Remember that your new source file will be on disk "B" since it was produced on a Z37, H/Z47 or Z67 disk system.

You should at this point use DGCONFIG.SUB to patch the Heath/Zenith CONFIGUR.COM program. Place all of the necessary files (XSUB.COM,, SUBMIT.COM, ED.COM AND DGCONFIG.SUB) on one disk and simply type SUBMIT DGCONFIG. This will place the completed file "DGCONFIG.COM" on the disk. This file can then be renamed to CONFIGUR.COM if so desired.

EXPLANATION

The electronic disk is the last drive on your system. If for instance you had a system configured with a H77, and H47 and electronic disk the drive letter of the electronic disk would be "F". If you have 256K of memory, the drive is a 19ØK drive. It works exactly like any other disk drive, except that it is not removable and will be erased when you power down the system. It

will NOT be erased if you RESET the computer. It should also be noted that the electronic disk is not a bootable drive.

When the CP/M operating system is cold booted, the real time clock is looked at and if it is running it is left alone. Otherwise it is set to zeros. The clock program can be used to set the real time clock and utilize some of its features. The clock program has a built in help mode. The help message is displayed when you type "CLOCK HELP". This program can either run in command mode where the commands are given on the execution line, or in menu mode where it will ask you for a command.

The time program is a simple clock display program that uses the real time clock. Both the clock and time program source code is included on your distribution disk as examples of the real time clock and its use.

The system keeps the current time and date in memory. These values are stored in BCD format. There are six (6) bytes of data. The data is stored in the order HOURS, MINUTES, SECONDS, MONTHS, DAYS, YEARS. The address of the six (6) byte string is found at location "13H. The 25th line display switch is at "15H". A value of "ØØH" indicates the 25th line display is not active. A value of "FFH" indicates the 25th line display is active.

If you use the 4 MHz option with an H77 system you will need to patch the utilities MOVCPM17, FORMAT, and DUP. Instructions for performing these patches are available from D-G Electronic Developments Company. Once you make the modification to 4 MHz, that bootable disk will no longer run at 2 MHz.

You should remember that the electronic disk does not make the usual noises a floppy drive makes. If you go through a procedure that performs a lot of disk access such as assembly or compilation of very large source programs, long periods of apparent system inactivity may result. This does not necessarily mean that your system has "died". Always give the machine fair time to complete the given task before attempting to perform further operations.

***** GLOSSARY *****

Address: Number representing the location of a byte of information in memory. The Z8Ø microprocessor used in the Heartbeat computer can address a maximum of 65,536 bytes of memory. These "addresses" range from "Ø" up to "65535" in decimal or from "Ø" up to "FFFF" in hexadecimal.

Applications Software: A program (or set of programs) that solves a specific problem or performs a specific task. Typical applications software includes business accounting packages, word processing programs and data base managers.

ASCII: Acronym for American Standard Code for Information Interchange. This code allows numbers, letters and special symbols to be stored in the computer in a recoverable format. An ASCII text file is a file that can be intelligibly displayed on a video screen or printed on paper.

Assembly Language: A language similar to machine language which uses mnemonics to represent instructions of the CPU.

Bank-select RAM: The 8-bit microprocessors used in most personal computers are limited to an address space (or usable memory capacity) of 64 Kbytes (65536 characters). This usable memory capacity may be extended by adding multiple 64 Kbyte "banks" of memory which may be turned "on" or "off" (selected) under software control. Note that any applications programs must "know" that these extra banks of memory exist and how to control them in order to make use of this extended memory capacity.

Baud Rate: A measure of the rate of transmission of information on a serial communications interface. For example, a serial device operating at 96ØØ Baud would transfer 96ØØ "bits" of information in a time period of one second.

Binary: A number system using only two digits, "Ø" and "1". Each digit of a binary number represents some power of two just as each digit of a decimal number represents some power of ten.

BIOS: Acronym for Basic Input/Output System. This portion of the CP/M operating system tailors the operating system to the specific computer on which it is being used.

Bit: The basic unit of information storage in a digital computer. A bit (actually an abbreviation of the term binary digit) is a number that can have one of two possible values, either Ø or 1. These two values may represent "true" or "false", "on" or "off" or any other idea that assumes only two possible states.

Buffer: An area of memory (or possibly a device) which is used to store something temporarily.

Bug: An error. A "software bug" is generally an error in the design or entry of a program. A "hardware bug" is a malfunction or error in the design of a hardware device.

Bus: The set of circuit board traces (or wires) which carries the electrical signals to the major subsystems (memory boards, I/O boards, etc.) of the computer.

Byte: The basic word size used by most personal computers. A byte is a number made up of 8 bits. This means that the value represented by a byte may range from Ø up to 255 in the decimal number system with which most of us are familiar.

Character: A symbol which conveys a specific meaning to people. Alphabetic letters, numbers and punctuation marks are examples of characters.

Code: A method of representing something, such as the alphabet, in terms of something else. The ASCII code is a method of representing the alphabet, numbers, various punctuation marks and special symbols in binary numbers which may be easily stored and used by a computer.

Control Character: Special characters in the ASCII character set which are not printable but are used to control various functions of the computer or its peripherals.

CP/M: Acronym for Control Program for Microcomputers. A disk operating system produced by Digital Research of Pacific Grove, California.

Disk Operating System: A computer system is generally made up of several components: CPU, mass-storage devices (disk drives), video terminal, printer, etc.. A Disk Operating System (DOS) is a collection of programs which in an orderly fashion manages the use of these system components by applications software. A well designed operating system allows the computer user to possess a minimum of knowledge of the "inner-workings" of his computer and its components.

Firmware: A collection of short programs or software routines, contained in system ROM, which are often accessed and thus preferably available at all times. Typical firmware routines include system monitors, disk system "boot code" or system initialization routines.

Floppy Disk: A flexible magnetic disk, usually enclosed in a square protective jacket, used to store information. Storage capacity of currently available floppy disk systems range from about 1ØØ Kbytes up to about 2 Mbytes. The most commonly available floppy disk packages are either 5 1/4 or 8 inches square. A disk is divided into concentric rings, called tracks. Each of these tracks is divided into multiple segments, called sectors. The amount of information stored in each sector is typically 128, 256, 512 or 1Ø24 bytes.

Hard Disk: A hard disk system contains a rigid magnetic disk which usually is not removable. The rigidity of the disk allows closer spacing of the disk read/write head to the disk and higher disk rotation speeds without damage to the disk. This allows more information to be stored on the disk than is possible with floppy disk systems.

Hardware: The physical components of a computer system. These include the computer mainframe, disk systems, video terminals, interface boards, etc..

Hexadecimal: A number system using sixteen digits, "Ø" through "9" and the alphabetic characters "A" through "F". Each digit of a hexadecimal number represents some power of sixteen just as each digit of a decimal number represents some power of ten.

HDOS: Acronym for Heath Disk Operating System.

Interface: The exchange of information between one thing and another or a device which facilitates this exchange.

Interrupt: A hardware signal to the computer's CPU that causes the current process to cease and another process, called an interrupt service routine, to take its place. Once the interrupt service routine is complete, the original process is resumed.

I/O: Abbreviation for Input/Output.

Kilobyte: 1Ø24 Bytes is usually referred to as 1 Kilobyte, 1 Kbyte or simply 1K. Note that the value 1Ø24 has been rounded to 1ØØØ for ease of written or spoken description. The value 32 Kilobytes (32K) would represent the real number 32768.

Language: A computer language is a code which allows a person to "tell" the computer the action he wishes to perform in a manner that is understandable to both the person and the computer.

Machine Code: The binary set of instructions and their operators which the computer's Central Processing Unit (CPU) "understands".

Megabyte: 1Ø24 Kilobytes or slightly over 1 million bytes.

Menu: A list, usually given on the video terminal screen, of the options available to the computer operator.

Microprocessor: The integrated circuit which is the Central Processing Unit (or CPU) of a computer system.

Mnemonic: An abbreviation, acronym or other device used to help remember something difficult. In assembly language, each instruction is given a three or four letter mnemonic such as "DAA" for Decimal Adjust the Accumulator.

Monitor: A set of firmware routines provided in many personal computers which allows the user various functional options once the system is powered up. Functions often provided by system monitors include disk system boot, setting of system real-time clocks, examination of system memory contents, etc..

MP/M: An acronym for Multi-Programming Monitor control program. This is a multi-user operating system produced by Digital Research of Pacific Grove, California.

Multi-user System: A computer system in which two or more users share a single CPU and/or group of system peripherals. Each user has his own video terminal.

Octal: A number system using eight digits, "Ø" through "7". Each digit of an octal number represents some power of eight just as each digit of a decimal number represents some power of ten.

Parallel Interface: An interface method in which one byte (eight bits) of information is transferred at one time. The word parallel refers to the fact that the eight bits are "side-by-side" or "in parallel" during transmission.

Partition: In order to more easily handle the data stored on very large mass-storage devices (such as large capacity hard disks) the drive is often broken up into two or more smaller storage areas which are accessed as if they were individual disk drives. These smaller storage areas are called partitions and the large capacity disk drive is said to be "partitioned".

Parity Check: A method by which information written into a memory location is checked on each subsequent access of that location. If the parity check indicates that the information has changed in a location, then a parity error is reported.

Peripheral Device: A device external to the CPU. For example, printers, disk systems or video terminals are not usually part of the CPU but are used in conjunction with it.

Personal Computer: A small computer system which is generally intended for the use of a single person.

Program: A sequence of coded instructions which performs a specific task.

RAM: Acronym for Random Access Memory. This type of memory device may be written to or read from at any time. The bulk of the memory in a personal computer system is RAM.

Real-time Clock: A set of registers or an integrated circuit within a computer system which keeps time of day information.

ROM: Acronym for Read-Only Memory. The contents of this type of memory device may be read but not altered. This type of memory device is generally used to contain firmware routines such as system monitors.

RS-232 Interface: An interface standard for use in serial communication. Devices which adhere to this standard should be compatible with one-another.

SASI (SCSI) Interface: Acronym for Shugart Associates Standard Interface or Small Computer System Interface. This is a definition of an interface method to connect small computer systems to a popular type of hard disk controller. The definition was originally proposed by Shugart Associates, a maker of disk drives, and later expanded by the American National Standards Institute (ANSI).

Sector: See Floppy Disk.

Serial Interface: An interface method in which one "bit" of information is transferred at a time.

Software: Programs which are executed by the CPU of a computer system.

System Integrator: A person who analyzes the computer needs of a customer and brings together (integrates) a system of hardware and software which will fulfill the customer's requirements.

TPA: Transient Program Area. This is the area of memory under the CP/M operating system in which user programs run and store data. A larger TPA provided by a computer system means that larger user programs may be written and run in that system.

Unit: Each individual drive within a disk system is often referred to as a "disk unit" or simply "unit".