Model H8-5
SERIAL I/O AND
CASSETTE INTERFACE
CARD

595-2151

OPERATION/SERVICE

MANUAL

HEATH
Schlumberger

HEATH
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Model H8-5
SERIAL I/O AND CASSETTE INTERFACE CARD

595-2151

HEATH COMPANY
BENTON HARBOR, MICHIGAN 49022
a Schlumberger company

TABLE OF CONTENTS

INTRODUCTION

Your Heath Model H8-5 Serial I/O and Cassette Interface Card provides you with two input/output ports to the Heath H8 Computer. One port provides a cassette tape interface while the other port provides a serial I/O port. The card plugs easily into the mother circuit board in the H8 Computer.

The cassette tape interface, along with the H8 front panel monitor, provides you with a fully automated Load and Dump facility. This greatly increases the system's usefulness by enabling you to store programs and data for later use. The interface will automatically compensate for variations in tape speed and will accept a wide range of input levels. Both high and low level outputs are provided to match any tape unit you may wish to use. The interface operates at either 300 or 1200 Baud and uses 2400 and 1200 Hz tones for Mark and Space respectively. A separate automatic motor control allows two tape recorders to simultaneously record (DUMP) and playback (LOAD). With this feature, you can edit either program or data files. A built-in timer will automatically delay recording until the recorder's motor attains its normal operating speed.

The serial I/O port normally operates with the system console. It provides serial communications at speeds from 110 to 9600 Baud at either 20 mA or RS-232 compatible levels. You can wire the 20 mA loop in either the active or passive mode. You can also select the data rates for receive and transmit independently from any of eight rates. These rates are derived from a crystal oscillator which provides excellent system stability. A software programmable USART allows control of port configurations by the user's program.

Each port has four interrupt flags which you can connect to your system's interrupt structure in several ways. This feature, and the USART, makes these ports very flexible.

The interface employs a port interchange switch. This allows you to dump and load data through a teletypewriter terminal as well as to a magnetic tape recorder.

A built-in logic probe is provided for the two initial adjustments needed. You can also use the logic probe for any future testing. No additional equipment is required since all signal sources are provided.

SPECIFICATIONS

SERIAL INTERFACE

Data Rate	110, 150, 300, 600, 1200, 2400, 4800, or 9600 baud
Output Levels	20 mA current loop or RS-232 compatible levels.
USART Programming Options	
Clock Rate Factor	1, 16, or 64.
Character Length	5, 6, 7, or 8 bits.*
Parity	Even, odd, or disabled.
Number of Stop Bits	1, 1-1/2, or 2.

CASSETTE INTERFACE

Data Rate	300 or 1200 baud.
Mark Frequency	2400 Hz.
Space Frequency	1200 Hz.
Audio Output Level (Into High Impedance)	500 mV peak-to-peak or 50 mV peak-to-peak.
Input Sensitivity	500 mV rms.
Input Impedance	100 Ω.
Speed Tolerance	±33% of recorded speed (wow + flutter + speed difference).
Motor Control	200 VDC maximum.
Contact Ratings	500 mA DC maximum.

GENERAL

Power Requirements	+8 VDC at 600 mA typical.
(From H8 Bus)	+18 VDC at 20 mA typical.
	−18 VDC at 20 mA typical.
Operating Temperature	0° to 40° Celcius.

The Heath Company reserves the right to discontinue products and to change specifications at any time without incurring any obligation to incorporate new features in products previously sold.

*NOTE: H8 software will not accept Baudot characters.

CARD CONFIGURATION

NOTE: If the shipping carton shows evidence of rough handling, carefully inspect the circuit board for damage. Report any damage immediately to the carrier.

JUMPER OPTIONS

Your Serial I/O and Cassette Interface Card was carefully assembled and checked at the factory prior to shipment. The card is now ready for use with the Heath H9 terminal. If you intend to use this Card with the H9 terminal, you may skip the following information and proceed directly to "Installation." If you intend to use the Card with equipment other than the Heath H9 terminal, you will have to change some of the jumper wires in the circuit board as explained in the following sections.

Refer to Pictorial 1-1 (Illustration Booklet, Page 1) for the locations of the following jumpers. NOTE: The Pictorial shows the jumpers installed as they are when the Card comes from the factory (ready for use with H9 terminal).

500 mV or 50 mV

This jumper wire selects the proper audio output level to your tape recorder. If you use the AUX or LINE inputs on your tape recorder, connect the jumper between the holes labeled 500 mV. If you use the MIC input on your tape recorder, connect the jumper between the holes labeled 50 mV.

Tape RX Baud Rate

These jumper wires, a capacitor, and the "Tape TX Baud Rate" jumper (below) select the operating speed of the tape interface; either 300 baud or 1200 baud. NOTE: Heath Software tapes require 1200 baud. Install a jumper wire at the two "H" locations for 1200 baud or install a jumper wire at the two "L" locations for 600 baud. Install a 230 pF capacitor at C107 for 1200 baud or install a 1000 pF (.001 μF) polystyrene capacitor at C107 for 600 baud.

COM (Common)

These jumper wires allow you to pick **one** tape recorder to playback (LOAD) or record (STORE) data. If you intend to use **two** tape recorders to simultaneously playback and record, these jumper wires should not be installed. If you intend to use a common tape recorder, install jumper wires at the two COM locations.

EIA or TTY

These jumper wires select the type of signals (EIA, 20 mA active, or 20 mA passive current loop) to be used with your terminal. Refer to the "Operation" section of this Manual and determine which type of signal you want to use and install jumper wires **only** as described in the corresponding section below.

EIA RS-232 (Required by H9 terminal)

Install jumper wires at the **three** EIA locations.

20 mA Active Current Loop (Required by H36 DEC Writer)

Install jumper wires at the **three** TTY LOCATIONS.

20 mA Passive Current Loop

Install a jumper wire **on**ly at the TTY location near IC122.

Tape TX Baud Rate

This jumper wire selects the operating speed of the tape interface as described under "Tape RX Baud Rate" given above. Install a jumper wire between the hole labeled TAPE TX and the hole labeled 1200 for 1200 baud or install the jumper wire between the hole labeled TAPE TX and the hole labeled 300 for 300 baud.

Serial Rx Tx Baud Rates

These jumper wires match the baud rate of the Interface Card to that of your terminal. Some common speeds are:

Teletype — 110.

H36 (High speed mechanical) — 300.

Heath H9 — 600.

Install a jumper wire from the hole labeled SER RX to a hole that matches the speed of your terminal. Also install a jumper wire from the hole labeled SER TX to a hole that matches the speed of your terminal.

Port Select

These jumper wires assign port numbers to the two USARTs. The ports used by the Heath software are as follows:

1. Load/Dump port at 370 and 371.

   AND

2. Console port at 372 and 373.

For use with Heath software, the jumper wires should be installed between the following holes:

Holt T to hole 3.

Hole W to hole 7.

Hole X to hole 2.

Hole Y to hole 0.

Interrupt Select

These jumper wires match the interrupt technique required by the software to Interface Card. For use with Heath software, the jumpers should be installed as follows:

Between the **lower** holes labeled RXR.

Between hole S and hole $\overline{13}$.

Between the holes labeled INT ON.

NOTE: The remaining holes are not used with the Heath H8 Computer.

INSTALLATION

Refer to Pictorial 2-1 (Illustration Booklet, Page 2) for the following steps.

1. Be sure your Computer is turned off.

2. Remove the two rear panel screws holding the top cover and set the top cover aside if not already done.

3. Remove rear panel screw FD. Then loosen the other screws in the tie bracket, remove the bracket, and set it aside.

Refer to Pictorial 2-2 (Illustration Booklet, Page 2) for the following steps.

NOTE: Install the cable assemblies on the circuit board as follows. Make sure you position the pin 1 end on each connector over the pin 1 end of the circuit board plugs.

4. 5-hole connector to P101.

5. 10-hole connector S102 to P102.

6. Phono plug P104 (with the heat-shrinkable tubing) to IN.

7. Phono plug P105 to OUT.

Refer to Pictorial 2-3 (Illustration Booklet, Page 2) for the following steps.

NOTE: In the next step, you will install the Card into the Computer. Install the Card in one of the unused plugs near the rear of the Computer, but do not try to install it at P10. It will not fit.

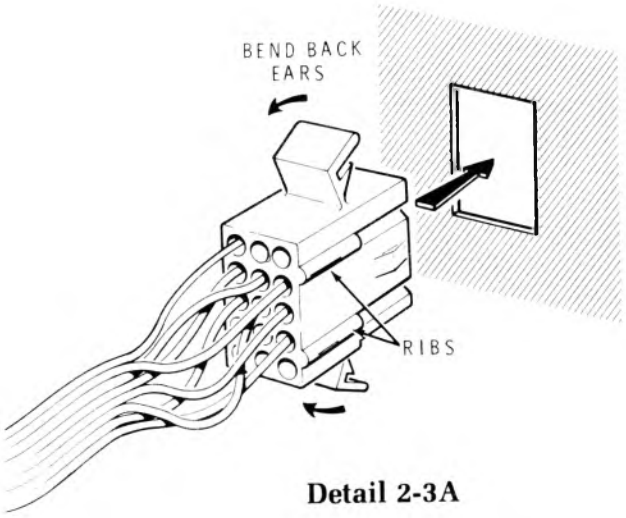
8. Plug the Serial I/O and Cassette Interface Card onto the selected plug in your Computer.

9. Refer to Detail 2-3A, bend back the two tabs, and insert the connector on the flat 8-wire cable into rear panel hole 3. Be sure the connector ribs are positioned as shown.

10. Loosen the two screws of cable clamp AG, open the clamp, route the remaining cables through the clamp, and then close the clamp on the cables and retighten the screws.

11. Install a 6-32 × 1/4" screw through the bottom of the computer chassis to hold the Card in place.

12. Reinstall the tie bracket and top cover on the Computer. Be sure to secure the Card to the tie bracket with a 6-32 × 1/4" screw.



Detail 2-3A

OPERATION

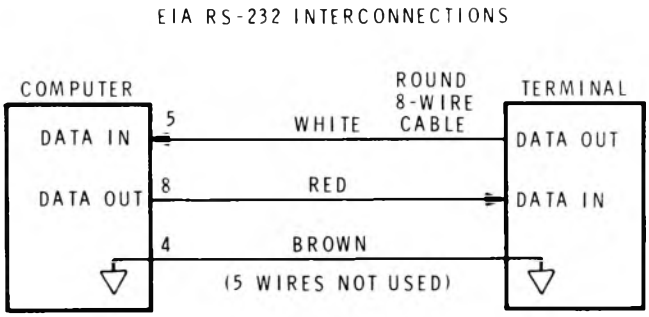
Your Serial I/O and Cassette Interface Card is very sophisticated and yet flexible. Many of its functions can be changed by moving jumpers or through software programming. This section of the Manual will help you fit the Card to your needs and take full advantage of its capabilities.

SERIAL I/O PORT

The signals that the serial I/O port uses to communicate with the terminal may be one of three types; EIA RS-232C compatible, 20 mA active current loop, or 20 mA passive current loop. The type you select must match that used by your terminal. The RS-232 levels are normally used by CRT terminals and other high speed devices. The 20 mA loops are used with teletypes or whenever very long lines are used between units.

RS-232 Levels

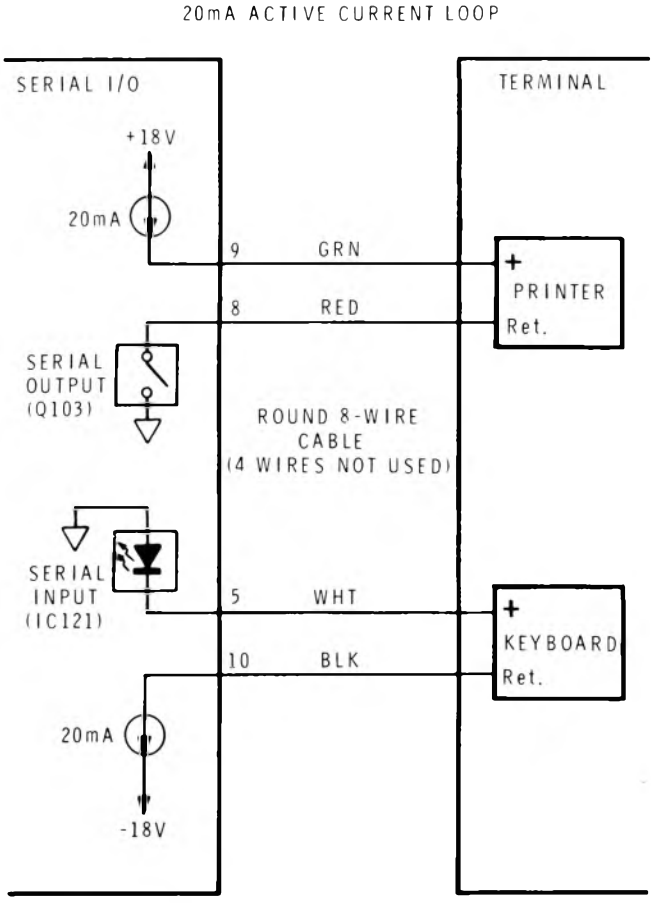
To use the RS-232 levels, the three EIA jumpers and none of the TTY jumpers should be installed. (See Page 00 of the "Card Configuration.") The cable coming from connector 3 on the rear of the Computer connects to your terminal as shown below in Pictorial 3-1.



PICTORIAL 3-1

20 mA Active Current Loop

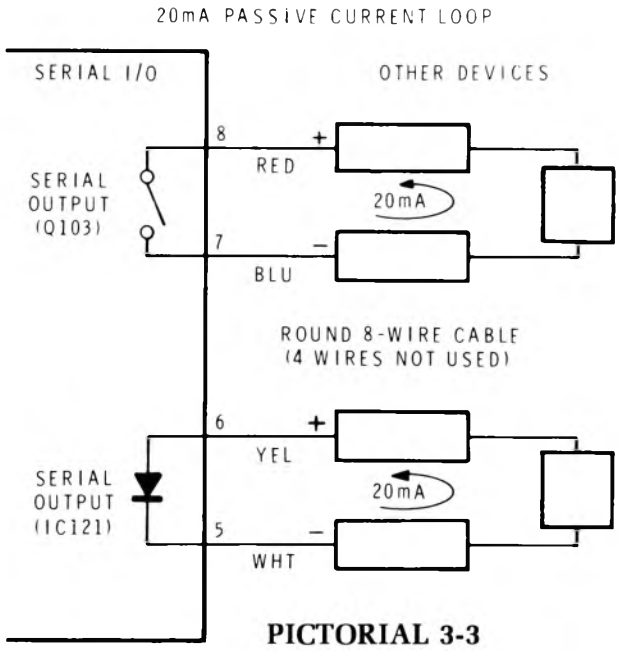
The 20 mA active current loop is used when the serial I/O interface is to supply the current for the loop. This is normally the mode used with a teletypewriter or other passive device. To use this mode, jumpers should be installed at the three TTY locations and none at the EIA locations. The cable coming from connector 3 on the rear panel of your Computer connects as shown in Pictorial 3-2.



PICTORIAL 3-2

20 mA Passive Current Loop

The 20 mA passive current loop is used when you connect the serial I/O port into a loop where another interface supplies the current. This might occur if you connect two computers together. To use this mode, only the TTY jumper near IC122 should be installed. (See "Card Configuration" on Page 4.) The cable coming from connector 3 on the rear panel of your Computer connects as shown in Pictorial 3-3.



PICTORIAL 3-3

Port Interchange Switch

The port interchange switch allows you to use a teletypewriter that has a paper punch and reader for both the system console and the load/dump port. With the switch in the NORMAL position, the teletypewriter is used as the system console, and the load and dump routines will address the magnetic tape interface. With the switch in the PORT INTCHG position, the teletypewriter (along with its paper tape punch and reader) will respond to the load and dump routines. See the software manual (supplied with your Computer) for instructions or how to reassign the system console address.

COPYING TAPES

The Cassette Interface provides the greatest reliability when tapes are played back by the same machine on which they were recorded. Therefore, it is recommended that you make a copy of the H8 software tape. This will give you maximum reliability when loading tapes and the original can be used as a backup copy if something happens to the work copy.

CASSETTE INTERFACE

Data is stored on magnetic tape one bit at a time as the tape moves past the record head. The data rate is 300 or 1200 bits per second. Since the tape moves at 1-7/8" per second, at 1200 bits per second, there will be 640 bits on each inch of tape. This means that each bit is only .0016 inches long. If a single bit is lost, the program will not run. Obviously, small defects in the tape which are not noticeable on audio recordings will be disasterous to a data storage tape. Tape defects, dust, smoke, and improper tape handling will all cause loss of data. Therefore, be very careful with your tapes.

Choose a good recorder.* One of the two biggest factors in reliability is the recorder you select. It will need an external speaker or earphone output jack and an auxiliary, radio, or microphone input jack. A motor control jack will make your system easier to operate but it is not essential. Preferably, choose a recorder that is designed to record music. Clean the tape head regularly and be sure it is free of dust.

Tape is the other biggest factor in reliability. Choose top quality tape in a well-designed housing. Use the type of tape your recorder was designed for, chromium dioxide if possible. Choose one of the shorter tapes (C-30); the tape is thicker.

To protect your tapes follow these precautions:

1. Always rewind a tape before you remove it from the recorder. This prevents contamination and scratching.
2. Always store a tape in its protective case.
3. Do not touch the tape or the leader.
4. Never place tapes near magnetic fields, as generated by motors, magnets, or TV SETS.
5. Do not expose tapes to direct sunlight or high temperatures.
6. Always have duplicate copies of all valuable tapes; like system software tapes.

When you set up your system, you may have to experiment to find the best settings for the volume control, tone control, or both. The tone control is normally set to midrange or toward the treble end. The volume control is not critical on playback once the minimum level is reached. Increasing the volume will sometimes be helpful when using poor recordings.

If your recorder has an automatic level control, defeat it if possible. Use the record level control to set the level to the highest level before overloading.

*All Heath computer hardware and software products were designed to work together as a complete system. Proper operation can be assured only when the computers are used with Heath designed or approved accessories. Heath does not assume the responsibility for improper operation resulting from custom interfacing, custom software, or the use of accessories not approved by Heath Company.

If you want to use a cassette deck that does not have a power amplifier, remove R101 from the Serial I/O and Cassette Interface Card to raise the impedance of the audio input.

If you have two tape machines, you can use one for playback while you record the other. To do this, use the audio cable and the 2-wire cable with black tubing for the playback machine. Use the other two cables for the recording machines, See the inset drawing on Pictorial 3-4 (Illustration Booklet, Page 3).

CASSETTE INTERFACE DISABLE

When you use the H10 Reader/Punch and the H8-2 Parallel Card as the load/dump port, the Cassette Interface must be disabled. To do this, remove the "Y" to "O" port select jumper. Be sure to disable the parallel port at address 370 and reinstall this jumper when you want to use the Cassette Interface again.

PROGRAMMING CONSIDERATIONS

The 8251 USARTs (IC123 and IC124) perform the serial-to-parallel data conversion and are very flexible devices. The manner in which they perform the conversion is determined by the external clocks and the control words sent from the central processing unit. For most applications, the software supplied by Heath Company will automatically take care of this. However, for specialized applications, you might need to know how to initialize and use these devices.

The following is a general set of requirements needed to properly operate the USARTs. This information is then followed by more technical and detailed information.

The following sequence of events must happen for a USART to work properly:

1. At power-up, or following a master reset, the USART is reset.

2. A MODE INSTRUCTION is sent to the USART defining the following characteristics of the I/O channel:

   - Clock rate.
   - Character length.
   - Parity.
   - Number of stop bits.

The Mode Instruction is a word sent by the CPU to the USART register at the odd-numbered port of the two ports assigned to each USART. The normal mode instruction for the Heath system is 116, which programs the USART for standard asynchronous operation.

3. A COMMAND INSTRUCTION is sent to the same port as the mode instruction. This word controls the actual operation of the USART. It enables portions of the circuitry, sets various bits, and resets the error flags.

4. A STATUS WORD may be read from this same port. It allows the CPU to determine when data may be transferred, which bits are set, and which errors have occurred.

5. Data is transferred between the USART and the CPU through the even-numbered port of the two ports assigned to each USART. (This is the port number which is actually programmed at the port decoder.) The mode and command instructions use the next higher port number.

NOTE: A New Command Instruction may be sent to the USART at any time. If, however, the USART had a character in its transmit buffer, that character would be lost.

USART DESCRIPTION

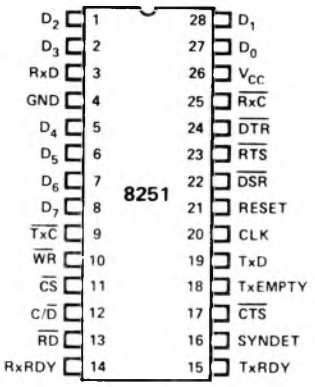
The following is Manufacturer's data concerning the USART and is supplied for your information. However, not all the information is applicable to your Serial Card.

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology. See Pictorial 3-5.

The USART has the following features:

- Synchronous and Asynchronous Operation
  - Synchronous:
    5-8 Bit Characters
    Internal or External Character Synchronization
    Automatic Sync Insertion
  - Asynchronous:
    5-8 Bit Characters
    Clock Rate — 1, 16, or 64 Times Baud Rate
    Break Character Generation
    1, 1-1/2, or 2 Stop Bits
    False Start Bit Detection
- Baud Rate —DC to 56 k Baud (Sync Mode)
  DC to 9.6 k Baud (Async Mode)
- Full Duplex, Double Buffered, Transmitter and Receiver
- Error Detection — Parity, Overrun, and Framing
- Fully Compatible with 8080 CPU
- 28-Pin DIP Package
- All Inputs and Outputs are TTL Compatible
- Single 5-Volt Supply
- Single TTL Clock

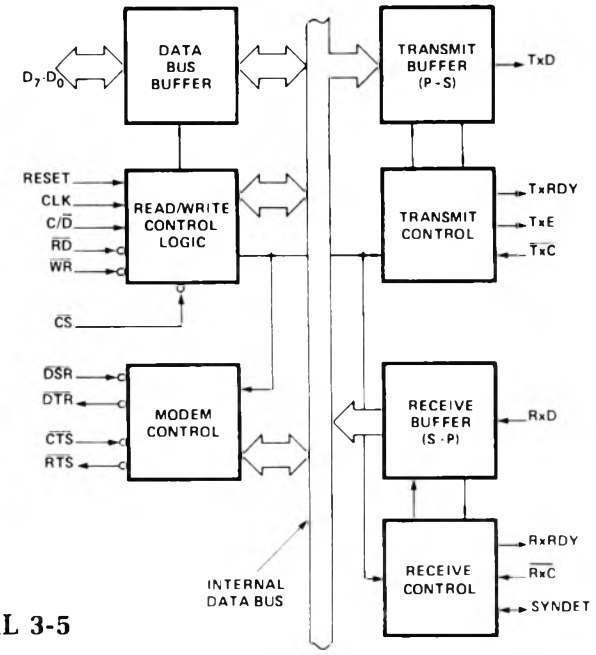
PIN CONFIGURATION



Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET	Sync Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM



PICTORIAL 3-5

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8251 BASIC FUNCTIONAL DESCRIPTION

General

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 8080 Microcomputer System. Like other I/O devices in the 8080 Microcomputer System, its functional configuration is programmed by the system's software for maximum flexibility. The 8251 can support virtually any serial data technique currently in use (including IBM "bi-sync").

In a communication environment, an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU.

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8251 to the 8080 system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the 8080 CPU. Control words, Command words, and Status information are also transferred through the Data Bus Buffer.

Read/Write Control Logic

This functional block accepts inputs from the 8080 Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for device functional definition.

RESET (Reset) — A "high" on this input forces the 8251 into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251 to program its functional definition.

CLK (Clock) — The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter clock inputs for synchronous mode (4.5 times for asynchronous mode).

$\overline{WR}$ (Write) — A "low" on this input informs the 8251 that the CPU is outputting data or control words; in essence, the CPU is writing out to the 8251. See Pictorial 3-6.

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251 ⇒ DATA BUS
0	1	0	0	DATA BUS ⇒ 8251
1	0	1	0	STATUS ⇒ DATA BUS
1	1	0	0	DATA BUS ⇒ CONTROL
X	X	X	1	DATA BUS ⇒ 3-STATE

PICTORIAL 3-6

$\overline{RD}$ (Read) — A "low" on this input informs the 8251 that the CPU is inputting data or status information, in essence, the CPU is reading from the 8251.

C/$\overline{D}$ (Control/Data) — This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs informs the 8251 that the word on the Data Bus is either a data character, control word, or status information.

1 = CONTROL 0 = DATA

$\overline{CS}$ (Chip Select) — A "low" on this input enables the 8251. No reading or writing will occur unless the device is selected.

Modem Control

The 8251 has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The modem control signals are general-purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{DSR}$ (Data Set Ready) — The $\overline{DSR}$ input signal is general-purpose in nature. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{DTR}$ (Data Terminal Ready) — The $\overline{DTR}$ output signal is general-purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

$\overline{RTS}$ (Request to Send) — The $\overline{RTS}$ output signal is general-purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for Modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send) — A "low" on this input enables the 8251 to transmit data (serial) if the Tx EN bit in the Command byte is set to a "one."

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, coverts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique), and outputs a composite serial stream of data on the TxD output pin.

Transmitter Control

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

TxRDY (Transmitter Ready) — This output signals the CPU that the transmitter is ready to accept a data character. It can be used as an interrupt to the system or, for the Polled operation, the CPU can check TxRDY using a status read operation. TxRDY is automatically reset when a character is loaded from the CPU.

TxE (Transmitter Empty) — When the 8251 has no characters to transmit, the TxE output will go "high." It resets automatically upon receiving a character from the CPU. TxE can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be transmitted automatically as "fillers."

$\overline{TxC}$ (Transmitter Clock) — The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the frequency of $\overline{TxC}$ is equal to the actual Baud Rate (1X). In Asynchronous transmission mode, the frequency of $\overline{TxC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x, or 64x the Baud Rate.

For example:
If Baud Rate equals 110 Baud,
$\overline{TxC}$ equals 110 Hz (1x)
$\overline{TxC}$ equals 1.76 kHz (16x)
$\overline{TxC}$ equals 7.04 kHz (64x).
If Baud Rate equals 9600 Baud,
$\overline{TxC}$ equals 614.4 kHz (64x).

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to the RxD pin.

Receiver Control

This functional block manages all receiver-related activities.

RxRDY (Receiver Ready) — This output indicates that the 8251 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or for Polled operation the CPU can check the condition of RxRDY using a status read operation. RxRDY is automatically reset when the character is read by the CPU.

$\overline{RxC}$ (Receiver Clock) — The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the frequency of $\overline{RxC}$ is equal to the actual Baud Rate (1x). In Asynchronous Mode, the frequency of $\overline{RxC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x, or 64x the Baud Rate.

For example:
If Baud Rate equals 300 Baud,
$\overline{RxC}$ equals 300 Hz (1x)
$\overline{RxC}$ equals 4800 Hz (16x)
$\overline{RxC}$ equals 19.2 kHz (64x).
If Baud Rate equals 2400 Baud,
$\overline{RxC}$ equals 2400 Hz (1x)
$\overline{RxC}$ equals 38.4 kHz (16x)
$\overline{RxC}$ equals 153.6 kHz (64x).

Data is sampled into the 8251 on the rising edge of $\overline{RxC}$.

NOTE: In most communications systems, the 8251 will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect) — This pin is used in SYNChronous Mode only. It is used as either input or output, programmable through the Control Word. It is reset to "low" upon RESET. When used as an output

(internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251 has located the SYNC character in the Receive mode. If the 8251 is programmed to use double Sync characters (bi-sync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as an input (external SYNC detect mode), a positive going signal will cause the 8251 to start assembling data characters on the falling edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. The duration of the high signal should be at least equal to the period of $\overline{RxC}$.

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251 is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the 8251 to support the desired communications format. These control words will program the: Baud Rate, Character Length, Number of Stop Bits, Synchronous or Asynchronous Operation, Even/Odd Parity, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251 is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251 is ready to receive a character. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251. On the other hand, the 8251 receives serial data from the MODEM of I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU that the 8251 has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU read operation.

The 8251 cannot begin transmission until the TxEN (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

Programming the 8251

Prior to starting data transmission or reception, the 8251 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251 and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

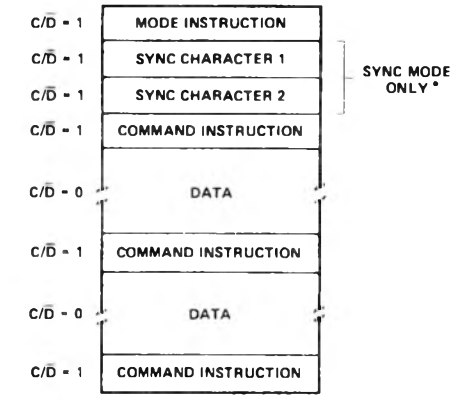
Mode Instruction

This format defines the general operational characteristics of the 8251. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the 8251 by the CPU, SYNC characters or Command instructions may be inserted.

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251.

Both the Mode and Command instructions must conform to a specified sequence for proper device operation. (See Pictorial 3-7.) The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251 for data communication.



*The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

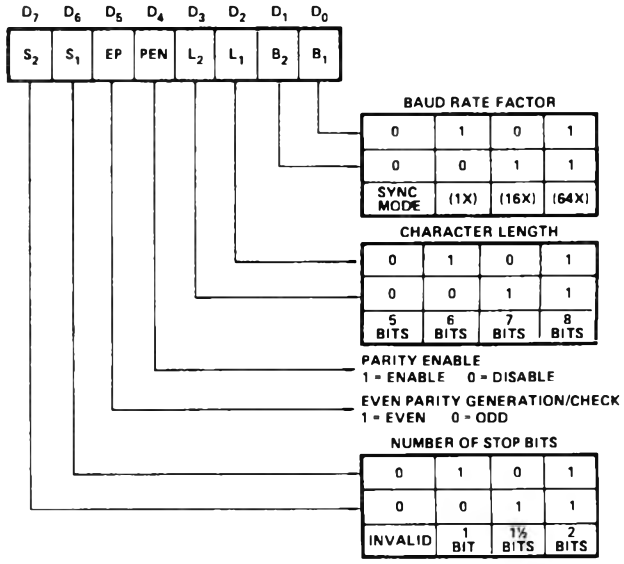
PICTORIAL 3-7

All control words written into the 8251 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251 at any time in the data block during the operation of the 8251. To return to the Mode Instruction format, a bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.

Mode Instruction Definition

The 8251 can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251, the designer can best view the device as two separate components sharing the same package, one Asynchronous, the other Synchronous. The format definition can be changed "on the fly," but for explanation purposes, the two formats will be isolated.

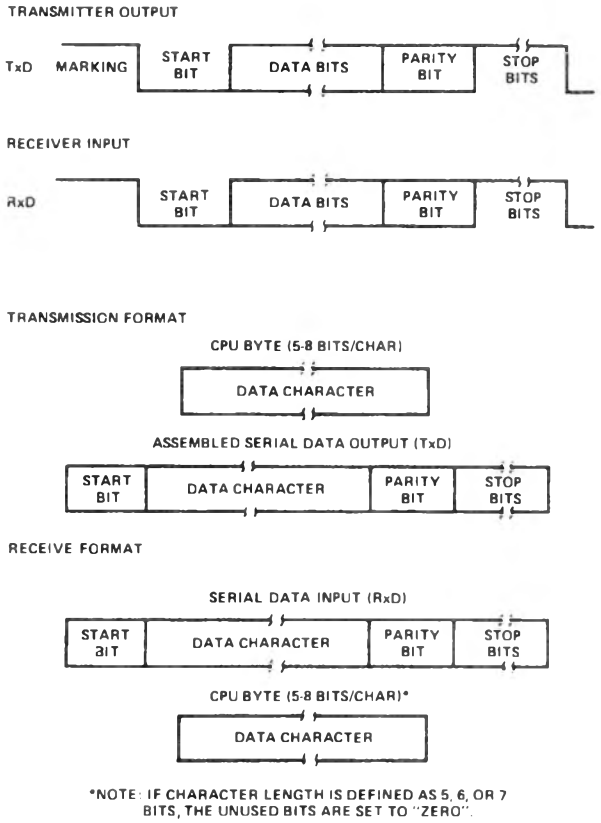
Asynchronous Mode (transmission) — Whenever a data character is sent by the CPU, the 8251 automatically adds a Start bit (low level) and the programmed number of Stop bits to each character. (See Pictorials 3-8 and 3-9). Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of the $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. Break characters can be continuously sent to the TxD if commanded to do so.



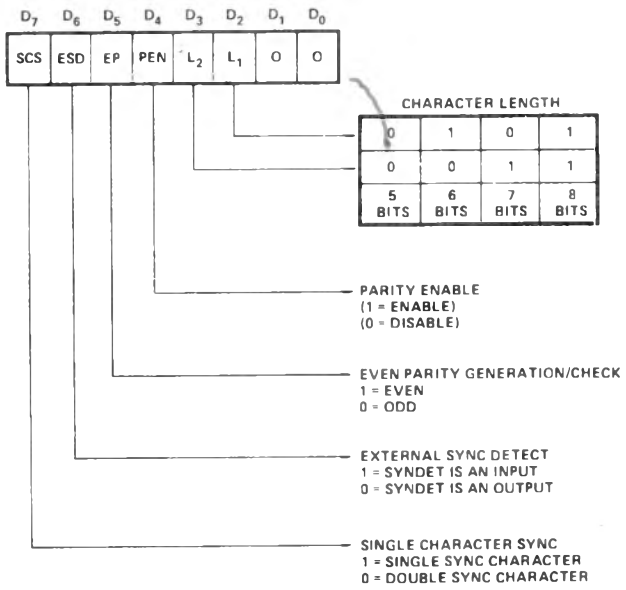
PICTORIAL 3-8

When no data characters have loaded into the 8251 the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.

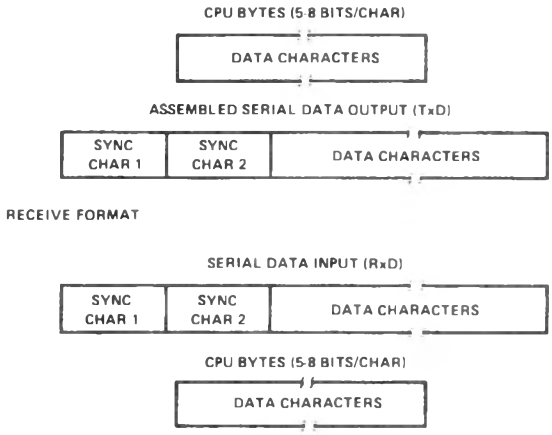
Asynchronous Mode (Receiver) — The RxD line is normally high. A falling edge on this line triggers the beginning of a Start bit. The validity of this Start bit is checked by again strobing this bit at its nominal center. If a low is detected again, it is a valid Start bit, and the bit counter will start counting. The bit counter locates the center of the data bits, the parity bit (if it exists) and the Stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of the $\overline{RxC}$. If a low level is detected as the Stop bit, the Framing Error flag will be set. The Stop bit signals the



PICTORIAL 3-9



PICTORIAL 3-10



PICTORIAL 3-11

end of character. This character is then loaded into the parallel I/O buffer of the 8251. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the Overrun flag is raised (thus the previous character is lost). All of the error flags can be reset by a command instruction. The occurence of any of these errors will not stop the operation of the 8251.

Synchronous Mode (Transmission) — The TxD output is continuously high until the CPU sends its first character to the 8251, which usually is a SYNC character. (See Pictorials 3-10 and 3-11). When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251 with a character before the 8251 becomes empty, the SYNC characters (or character if in single SYNC word mode) will be automatically inserted in the TxD data stream. In this case, the TxEmpty pin is raised high to signal that the 8251 is empty and SYNC characters are being sent out. The TxEmpty pin is internally reset by the next character being written into the 8251.

Synchronous Mode (Receive) — In this mode, character synchronization can be internally or externally achieved. If the internal SYNC mode has been programmed, the receiver starts in a HUNT mode. Data on the RxD pin is then sampled in on the rising edge of $\overline{RxC}$. The content of the Rx buffer is continuously compared with the first SYNC character until a match occurs. If the 8251 has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a Status Read.

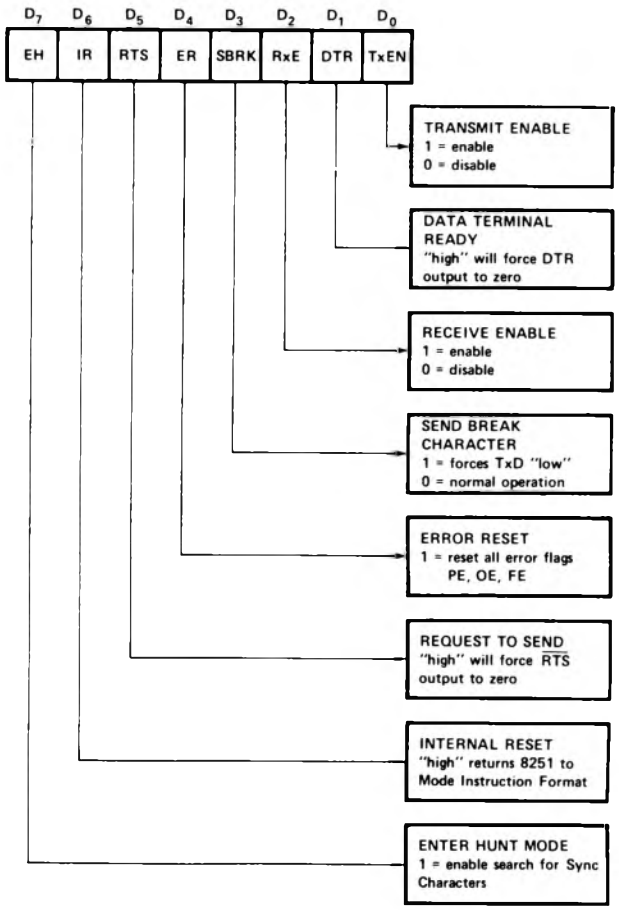
In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin. The high level can be removed after one $\overline{RxC}$ cycle.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost.

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251 has been programmed by the Mode Instruction and the Sync Characters are loaded (if in Sync Mode), then the device is ready to be used for data communication. (See Pictorial 3-12). The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset, and Modem Controls are provided by the Command Instruction.



PICTORIAL 3-12

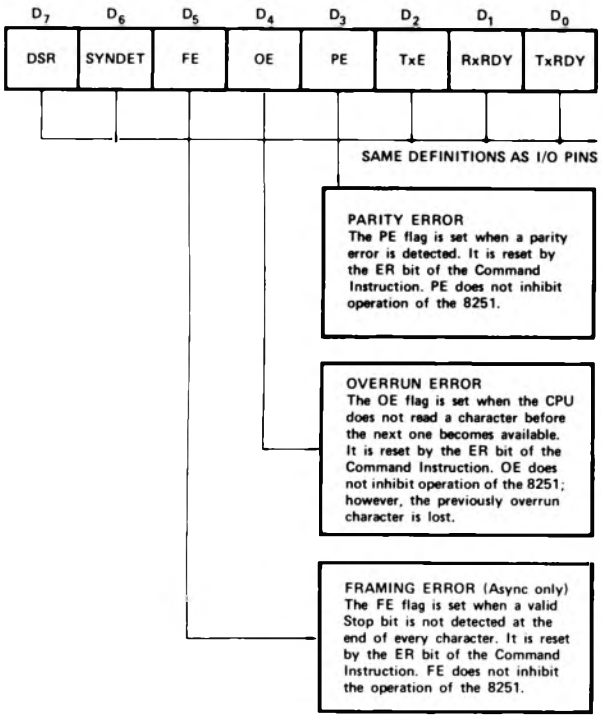
Once the Mode Instruction has been written into the 8251 and Sync characters inserted, if necessary, then all further "control writes" ($C/\overline{D}$ = 1) will load the Command Instruction. A Reset operation (internal or external) will return the 8251 to the Mode Instruction Format.

STATUS READ DEFINITION

In data communication systems, it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251 has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. See Pictorial 3-13.

A normal "read" command is issued by the CPU with the C/$\overline{D}$ input at one to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251 can be used in a completely Polled environment or in an interrupt driven environment.



PICTORIAL 3-13

TAPE HEAD ALIGNMENT

NOTE: Perform this tape head alignment only if you are experiencing difficulty when you load prerecorded cassette software information. Try to load several different programs before you decide your tape heads need alignment.

Due to the tolerances in the manufacturing of cassette recorders, you may want to realign the tape head in your recorder. This will maximize the reliability of the system when you load prerecorded tapes and will help when you use tapes in different recorders. A test tone is provided for this purpose on the standard systems software tape supplied with each H8 Computer.

Before you adjust the tape head, consult the owner's manual for your cassette recorder for information reguarding its warranty. To align a tape head:

1. Locate the azimuth alignment screw for your cassette unit. Normally this is one of the mounting screws for the tape head and is accessible through a hole or a slot when the unit is in the play mode. Note the position of the screw so that you can reutrn it to this position if necessary.

2. If you have a tone control, turn it to its full treble position.

3. Play back the test tone, which is present at the beginning of side one on the systems software tape. This is the steady, high-pitched tone.

4. Adjust the azimuth alignment screw for the loudest tone. If you have an oscilloscope, use it to monitor the signal strength.

5. Note the position of the alignment screw.

6. Turn the tape over and play back the tone on side two. (This tone is located at the end of side two, directly across from the tone on side one.)

7. Adjust the azimuth alignment screw for the loudest tone and note that position.

8. Set the alignment screw midway between the two points of maximum output.

CIRCUIT DESCRIPTION

As you read this section, refer to the Block Diagram (Illustration Booklet, Page 4) and the Schematic (fold-in).

The Serial I/O and Cassette Interface Card consists of two serial data channels. One channel is used for the cassette interface, and the other channel is buffered and used as a serial I/O port. These channels communicate with the CPU (central processing unit) through three parallel buses, an 8-bit data bus, the control bus, and the eight low-order bits of the address bus. The USARTs (universal synchronous asynchronous receiver transmitter) convert this data to a serial format to communicate with the peripheral devices.

CASSETTE INTERFACE

Digital data is recorded on standard audio tape as two audio tones, 1200 Hz for a space (logic 0) and 2400 Hz for a mark (logic 1). The cassette interface serially reads these tones and also supplies the tones to a recorder.

Limiter and Slicer

The audio output from the tape player is applied across load resistor R101, through R102, to limiting diodes D101 and D102. These diodes limit the input signal so that IC102A is not overdriven by large input signals. The output of the comparator is low during the positive half cycle of the input and high during the negative half cycle. (See the Timing Diagram in the Illustration Booklet, Page 4.) Resistors R107 and R108 provide hysteresis to ensure a proper square wave for the following digital circuitry.

Frequency Doubler

IC101A is a monostable multivibrator which is triggered on the positive edge of the signal from IC102A. IC101B is also a monostable but it is triggered on the negative edge of the same signal. As shown in the Timing Diagram, the outputs are short pulses. These pulses are combined in IC108A and are used to clock the rest of the circuitry.

Space Detector

IC103A is a retriggerable monostable which is triggered by the signal from IC108A. The pulse width at the output of this monostable (in the Timing Diagram) is set so that a 2400 Hz input will keep the monostable triggered, while a 1200 Hz input will allow it to time out.

The space detector adjustment is made by connecting an 1800 Hz signal to the audio input and adjusting the monostable so that it almost times out before it is retriggered. If the monostable does time out, TP1 will pulse high and cause test lamp LED101 to light. When the LED just goes out, the period of the monostable is adjusted properly.

Data Latch

The output from monostable IC103B at the end of each cycle is latched by IC104A on the positive-going edge of the signal from IC108A. The output from IC104A is the recovered digital data. If a 1200 Hz input had been present, IC103B would have timed out and its output would have been low when IC104A sampled it. This results in a "space" (Logic Low) being detected. If a 2400 Hz input had been present, IC103B would be retriggered before it could time out and its output would have been high when IC104A sampled it. This results in a "mark" (Logic High) being detected. IC104B is a data latch and retains the last mark bit of the data stream. The output of IC104B is fed through IC117C to the serial data input of USART IC123.

Controlled Divider

IC105A will divide by two if the audio input is 2400 Hz or it will divide by one if the input is 1200 Hz. Thus the output of IC105A will always be of the same frequency, for either 1200 or 2400 Hz inputs. This signal is used to generate the clock required to drive the USART. IC105B divides the output from IC105A by two to provide a symmetrical square wave for the phase-locked loop.

IC105A is clocked by the pulses from IC108A. If it is not set by IC103A, IC105A will toggle on each positive edge and divide the frequency of the signal by two. For a 2400 Hz audio input, the output of IC103B will stay high and IC103A will not be triggered; thus IC105A will divide by two.

For a 1200 Hz audio input, the output of IC103B will go low during each cycle, which then triggers IC103A. IC103A is a monostable multivibrator which puts out a short pulse for each negative transition at its input. This pulse sets IC105A. At the beginning of the cycle, IC105A was toggled to the reset state and is now being set again. Thus the output of IC105A goes through a complete cycle for each cycle of the signal at pin 3 if the input signal was 1200 Hz; so it divides by one.

Phase Locked Loop Clock Synthesizer

IC106 and IC107 form a phase locked loop which multiplies the frequency of the output signal from IC105B by 16. The output from IC105B is used as the reference input to the phase detector of IC106. The feedback for the loop is provided by IC107, which divides the output of IC106 by 16. The output of the phase detector inside IC106 is filtered by R122, R123, and C108; and fed to the voltage-controlled oscillator section. The frequency of the VCO is determined by R118, R119, and C107.

The phase detector produces a signal which is proportional to the difference in frequency of its two input signals (pins 14 and 3). This signal controls the VCO whose output is then divided by 16 in IC107 and fed back to the phase detector input. If the two input frequencies are to be the same (loop locked), then the output frequency must be exactly 16 times the reference frequency applied to pin 14. This results in a multiplication of the reference frequency by 16. The signal from IC108B is used as the receiver clock input to USART IC123. Since the clock is derived from the data on the tape, the speed of the tape is not critical.

The phase locked loop is adjusted for a center frequency of 19,200 Hz. This is done by "ANDing" a 2400 Hz signal from the clock scaler with the output of IC107 which will also be 2400 Hz when the PLL is adjusted properly. When both signals are of the same frequency, but 180° out of phase, the output of IC117A will always be low. When the signals differ slightly in frequency, the output of IC117A (TP2) will pulse slightly which can be seen with the test lamp. When the frequencies differ greatly, the lamp will glow steadily.

Frequency Shift Keying Modulator

The transmit data from USART IC123 is inverted by IC112A and fed to IC111B. When the USART is in a mark state (logic high), IC111B is held reset and IC111A divides the 4800 Hz signal from the clock scaler by two. This is the 2400 Hz mark signal which is recorded on the tape. When the USART output goes low, the J and K inputs of IC111B go high and allow it to toggle. IC111A and IC111B then form a divide by four circuit and generate a 1200 Hz tone. The output from IC111A is filtered by R136 and C112. R137 and R138 form a divider for a low level microphone output signal.

Motor Control

When a tape is to be read, the CPU sets the RTS bit in the command word going to the USART. This causes the $\overline{\text{RTS}}$ pin on the USART to go low, which is inverted by IC112D and fed to relay driver transistor Q101. When Q101 conducts, it energizes relay RL102 which starts the tape player's motor. When the CPU is finished reading the tape, it resets the RTS bit in the command word and stops the motor.

When the CPU is ready to record data, it sends the first word to the USART, which causes the TxE (Transmitter Empty) pin to go low. This low is inverted by IC112B and drives Q102, energizing the relay and starting the recorder's motor. IC112C, which is also fed from Q102, then starts the 5-second timer. The output of IC112C had been low, keeping C111 discharged through D103. This forced the output of IC102B high to hold the $\overline{\text{CTS}}$ (clear to send) input of the USART high. With $\overline{\text{CTS}}$ high, the USART cannot send data.

Once the output of IC112C goes high, C111 starts charging through R132. After about five seconds, the voltage at pin 8 of IC102B reaches the voltage at pin 9 and the output will go low. This enables the USART to start data transmission. The delay allows the tape recorder to reach operating speed and provides a convenient gap on the tape for separating programs.

After the first word is transferred from the USART, the TxE pin may go high momentarily, showing that the USART is empty while a new word is being loaded. To prevent this pulse from affecting the motor control circuitry; R125, R126, and C109 filter the pulse out.

USART

The USARTs (IC123 and IC124) are the heart of the serial channels. These devices perform the parallel-to-serial conversion between the parallel system bus and the serial data ports. They are software programmable and, as such, must be initialized before they can be used.

The USART communicates with the CPU through the bidirectional data bus which carries data, command, and status words. The serial data is transferred on the TxD (transmit data) and RxD (receive data) lines at the data rate selected by the TxC (transmit clock) and RxC (receive clock) lines, respectively. These clocks normally operate at 16 times the data rate and are obtained from the data rate scaler, IC114 and IC116. The serial data lines rest in the mark state, which is a logic high.

The status flags of the USARTs may be read by the CPU through the data bus and are also available at certain pins on the IC package. These flags are gated at IC128 and IC129, which are open collector gates, by the DTR bit from the USART. The outputs from these gates may be combined and patched to the interrupt bus for systems which require immediate attention to I/O requests. The DTR bit on the USART is software controlled and is used to selectively disable the interrupts for each channel.

CLOCK AND DATA RATE SCALER

The data rate scaler provides the data clocks for the USARTs, and the audio tone for the tape interface modulator.

Inverters IC112E and IC112F are biased in their active regions and, with crystal Y101 and capacitor C113, form a 4 MHz oscillator. The oscillator signal is first divided by 13 in IC113, which produces 307 kHz at IC114 pin 2. Each of the four stages of IC114 then further divides the signal by two and produces four of the clock outputs. The 1200 baud output (IC114, pin 11) is fed to IC116 where further divisions by two give three more clock outputs. The 2400 baud output (IC114, pin 12) is fed to IC115 which divides the signal by 11. This asymmetrical signal is then fed to the divide-by-two section of IC116. This generates the 110 baud output which is also used as a calibration signal.

The following chart shows the frequencies available at the clock outputs.

DATA RATE	CLOCK FREQUENCY
9600	153.6 kHz
4800	76.8 kHz
2400	38.4 kHz
1200	19.2 kHz
600	9600 Hz
300	4800 Hz
150	2400 Hz
110	1745 Hz

SERIAL I/O BUFFER

IC's 119 and 121 optically isolate the circuit board TTL levels from external levels or currents. This allows interfacing to current loops which are not referenced to the computer's ground.

Transmit data from USART IC124 is buffered by IC122C and applied to transistor Q105. Q105 drives the optical coupler LED inside IC119, and the light controls the photo transistor inside the coupler. When the photo transistor is off, Q104 provides a constant current to the base of Q103, which keeps Q103 turned on until the LED turns on the photo transistor. Then the drive current to Q103 is shunted and Q103 stops conducting.

Q103 acts as a switch that is controlled by the transmitted data. When not transmitting, the output of the USART is high (in a "mark" state) which causes Q103 to conduct. As data is transmitted, Q103 turns off and on corresponding to the spaces and marks. Diode D107 provides reverse voltage protection should the output leads be interchanged.

For a passive 20 milliampere current loop output, pins 7 and 8 of P102 are inserted in the loop with pin 8 to the more positive side. For an active loop (current supplied by the interface), current flows from pin 9, through R144, to the loop. The return side of the loop, pin 8, is switched to ground by Q103. For an RS-232 output driver, R144 and R145 form a pull-up to +18 volts while Q103 and R143 pull the output (pin 8) negative when Q103 conducts.

IC121 provides isolation for the input signal. D108 provides reverse voltage protection and R152 improves noise immunity by shunting low level current.

When current flows through the LED in IC121, the photo transistor turns on and causes pin 12 of IC122D to go low. IC122D inverts this signal and feeds it to the data input of the USART. IC122D also buffers any direct TTL inputs from pin 3 of P102.

When used as a passive input, R151 is jumpered out of the circuit and pins 5 and 6 of P102 are inserted in the loop with pin 6 to the more positive side. When used as an active input, R151 is again jumpered, but pin 6 is jumpered to ground. The loop is connected between pins 5 and 10, with the more positive side to pin 5. R143 provides a current source to the negative supply line from pin 10. When used as an RS-232 input, pin 6 is jumpered to ground and the signal is applied to pin 5. R151 provides current limiting for the LED input of IC121.

IC122A and B, and Q106 and Q107 provide buffering for the $\overline{DTR}$ and $\overline{RTS}$ command lines from the USART. These lines are software programmable and may be used for controlling the serial I/O device.

PORT DECODER

The port decoder causes each I/O port to respond only to its particular port number. When the CPU addresses an I/O port, the port number is put out on the lower eight bits of the address bus. These lines are fed to IC125 and IC126 which may be programmed to respond when certain addresses are present. Due to the bus structure of the computer, the address (and data) lines go low when asserted.

The decoder has three sections; IC126A, IC125, and IC126B. These correspond to the three digits of the port number. IC126A decodes the most significant digit. Its selected output goes low and enables IC125 to decode the second digit. Then its selected output goes low and enables IC126B to decode the least significant digit. Notice that only even-numbered addresses are available from IC126B. This is because the USARTs require a pair of ports, one for control words and the other for data. The least significant bit of the address ($\overline{A}o$) is used to switch the USART between these ports.

The selected output of IC126B goes low when it is enabled. This enables the USART through the $\overline{Chip\ Select}$ pin. The two USART chip select pins may be interchanged with Port Interchange switch SW101 if you want the console device to respond to the Load and Dump address. This is useful when using a teletype terminal's paper tape punch/reader.

The address decoder is active during memory references and the USARTs may be enabled. This has no effect, however, since the I/O read and write pulses would not be present.

CONTROL LOGIC

The signals from the control bus are buffered by IC127. The $\overline{Reset}$ line goes low during "power up" and whenever the system is reset from the computer front panel. This signal is inverted by IC127E and resets the USARTs, IC123 and IC124. The least significant bit of the address, $\overline{A}o$, is inverted and switches the USARTs between the command ($\overline{A}o$ Lo) and data ($\overline{A}o$ Hi) modes. The I/O write line (IOW) causes a word to be written into a USART if it is enabled. The I/O read line (IOR), in conjunction with the address decoder, causes a word from the selected USART to be placed on the local data bus.

Either output from the address decoder going low will cause the output of IC118D to go high. If the I/O read line is also high, the output of IC118C will go low and enable bus driver IC132, and disable bus receiver IC131. The system clock, $\emptyset 2$, is inverted by IC127B and used as the high speed clock for the internal operation of the USARTs.

DATA BUS BUFFERS

IC131 and IC132 form a bidirectional, tri-state, data bus buffer. If neither of the ports are being read, IC131 is enabled by the low on $\overline{CE}$, and IC132 is disabled. This inverts the system data bus and puts it on the local data bus to the USARTs. Since IC132 is disabled, its outputs are in a high impedance state and have no effect.

When either USART is to be read, the output of IC118C goes low. This disables IC131 and enables IC132, which turns around the local data bus and transfers data from the selected USART to the system data bus.

LOGIC PROBE

The inverting input (pin 4) of IC102C is used to check for TTL logic levels. The noninverting input (pin 5) is held at 1.2 volts by R159 and R161. Whenever the test signal is greater than 1.2 volts, the output of IC102C goes low and discharges C114. This causes the output of IC102D to go low and LED101 to turn on. When the test input goes below 1.2 volts, the output of IC102C will go high and allow C114 to start charging. When the capacitor voltage reaches approximately 2.5 volts, the output of IC102D will go high and turn off the LED. The charging capacitor causes short input pulses to be stretched so they can be seen as the LED stays lit.

POWER SUPPLY

Unregulated, positive 8-volts DC is supplied from the main Computer bus to the circuit board. IC133 then regulates it at +5 volts.

PERFORMANCE TESTS

The following tests will help you locate a problem concerning the serial I/O port. If you get the proper response in each of the following steps, you may consider the Interface Card to be operating properly. If at any time you do not get the proper indication, turn off the Computer, proceed to the "In Case of Difficulty Section" which follows, and repair the problem.

TERMINAL TESTS

NOTE: If you do not have a terminal, proceed to "Cassette Interface Tests."

Refer to Pictorial 3-4 (Illustration Booklet, Page 3) for the following steps.

The following steps will test the operation of your terminal through the serial I/O port. The tests assume that:

- The serial I/O port is wired for 372.
- Port interchange switch SW101 is in the NORM position.
- The baud rate and interface signals have been selected and jumpered to match your terminal.

If you have a Heath H9 Terminal, plug the round 8-wire cable into rear panel connector 3 of your Computer and the serial I/O connector on your terminal. If you have other than a Heath Terminal, refer to the "Operation" section on Page 6, wire the end of the cable as necessary to be compatible with your terminal, and plug it into connector 3 on the rear panel of your Computer and into your terminal.

NOTE: If you have an H9 Terminal, be sure it was wired for 600 baud and the following keys are positioned properly:

BAUD RATE — Down.

FULL DUPLEX — Down.

OFF LINE — Up.

SCROLL — Down.

1. Simultaneously press the Ø and RST/Ø computer keys.
2. Press the MEM key. } Sends mode word
3. Enter 316 373. } to USART
4. Press the OUT key. }
5. Press the MEM key. } Sends command
6. Enter 005 373. } word to
7. Press the OUT key. } USART

8. Press the MEM key.
9. Enter 101 372.
10. Press the OUT key.

} Sends letter "A" to terminal

(Each time you press the OUT key, an "A" is typed on the terminal.)

The following steps will input a character from the terminal and echo it back to the terminal.

11. Reperform steps 1 through 7 above.

12. Press the "—" key on the Computer.

13. Press the "A" key on the terminal. (Nothing may happen that you can see.)

14. Press the Computer IN key. (The left three digits of the Computer should change to 301 or 101.)

15. Press the Computer OUT key. An "A" should be typed out each time you press the OUT key.

16. Simultaneously press the Ø and RST/Ø keys.

CASSETTE INTERFACE TESTS

NOTE: If you do not have a cassette recorder, or do not intend to use the cassette interface feature, this completes the "Performance Tests."

Make the following connections to your recorder.

1. Connect the audio cable with black tubing to the EXTERNAL SPEAKER or EARPHONE jack. NOTE: If you are using two tape machines, make this connection to the playback machine. See the inset drawing on Pictorial 3-4 (Illustration Booklet, Page 3).

2. Connect the other audio cable to the AUX (RADIO or LINE) or MIC input jack. This depends on the jumpers installed on the Card. NOTE: If you are using two tape machines, make this connection to the recording machine.

3. Connect an unmarked (without sleeving) 2-wire cable (with subminiature plug) to the motor control jack (may be marked REMOTE). NOTE: If you are using two tape machines, make this connection to the recording machine.

Only perform the next step if you are using two tape machines.

4. Connect the 2-wire cable with black tubing to the motor control jack (REMOTE) of the playback machine.

NOTE: The cassette interface is very flexible. While it will accept a wide range of input levels, you may have to experiment with the playback and record levels of your machine due to the difference in recorders.

High-level inputs to the interface will generally help by making up for some tape dropouts. However, too high a level will degrade the signal-to-noise ratio. The tone control should be set at either midrange or in the treble area. You may have to experiment to find the best settings for reliable operation.

NOTE: If you have two tape machines connected, use only the playback machine in the following steps.

5. Turn on the tape recorder and put it in the PLAY mode. The motor should not start.

6. Press the Computer LOAD key. The motor should start.

7. Simultaneously press the Ø and RST/Ø keys. The recorder motor should stop.

8. Push the recorder's STOP button.

9. Put the Heath H8 software tape into the recorder with side one up. Be sure the tape is rewound. (Do not use the blank tape supplied with this Card).

10. Put the recorder in the play mode. (The tape will not move.)

11. Press the Computer LOAD key. The tape will start. After several seconds, the Computer readout will start displaying addresses, starting at 040100 and going upward.

NOTE: If the display does not start counting upward, adjust the playback level or tone control of your tape recorder. Then:

- Rewind the tape.
- Simultaneously press the Computer Ø and RST/Ø keys.
- Put the recorder in the PLAY mode.
- Press the Computer LOAD key. The program should now load into your Computer.

12. When the tape finishes loading, the Computer will make a single beep and the tape will stop. If the Computer continues to beep:

    - Simultaneously press the Ø and RST/Ø keys.
    - Rewind the tape.
    - Press the Computer LOAD key.
    - Adjust the recorder's volume or tone control.
    - Adjust the recorder's PLAY button and load the tape into the Computer again.
    - Repeat these steps until the Computer gives a single beep when the tape stops.

The editor program is now loaded into the Computer. In the following steps you will make a copy of this program. Use the blank tape supplied with your kit.

13. If you have only one machine connected, rewind the H8 software tape and remove it from the machine. You may have to remove the plug going to the "remote" jack.

14. Advance the blank tape until all the leader is on the takeup reel and recording tape is exposed in the cassette opening.

15. Insert the blank tape into the recorder and set the machine to record. (Set the record level if necessary.)

16. Install the 2-wire cable (without the tubing) into the "remote" jack of the recorder.

17. Press the Computer DUMP key. After a short delay, the displays will start to count up.

18. When you hear the beep, the dump is finished.

19. Again press the DUMP key to make a safety copy.

20. Rewind the tape. It may be necessary to remove the motor control cable.

21. If you are using two machines, move the tape to the playback machine.

22. Reinstall the motor control cable.

23. Put the machine in the play mode.

24. Press the Computer LOAD key and the tape will load into the Computer as before.

25. If your Terminal is connected, press the Computer GO key. The Terminal will print out the title label of the editor and the editor routine is ready for you to use. (See your Computer software Manual.)

26. Simultaneously press the RST/Ø and Ø keys.

27. Rewind the tape.

28. Stop the recorder and remove the tape.

This completes the "Performance Tests."

IN CASE OF DIFFICULTY

This section of the Manual is divided into two parts. The first part, titled "Troubleshooting and Repair Precautions," points out the care that you should use when you service the unit to prevent damaging components.

The second part, titled "Troubleshooting Chart" gives difficulties and likely causes.

If the "Troubleshooting Chart" does not help you locate the problem, read the "Circuit Description" and refer to the Schematic Diagram (fold-in) to help you determine where the trouble is. Refer to the X-Ray View (Illustration Booklet, Page 5) for the physical location of parts on the circuit board.

NOTE: In an extreme case where you are unable to resolve a difficulty, refer to the "Service Information" inside the rear cover of this Manual. Your Warranty is located inside the front cover.

Troubleshooting and Repair Precautions

1. Make sure you do not short any adjacent terminals or foils when you make tests or voltage measurements. If a probe or test lead should slip, for example, and short together two adjacent connections, it is very likely to damage one or more of the transistors, diodes, or IC's.

2. Be especially careful when you test any circuit that contains an IC or a transistor. Although these components have an almost unlimited life when used properly, they are much more vulnerable to damage from excess voltage and current than many other parts.

3. Do not remove any components while the unit is turned on.

4. Handle MOS IC's properly. Static electricity can damage them.

5. When you make repairs, make sure you eliminate the cause as well as the effect of the trouble. If, for example, you find a damaged resistor, be sure you find out what damaged the resistor. If the cause is not eliminated, the replacement resistor may also become damaged when you put the unit back into operation.

6. In several areas of the circuit boards, the foil patterns are quite narrow. When you unsolder a part to check or replace it, avoid excessive heat while you remove the part. A suction-type desoldering tool makes part removal easier.

COMPONENTS

To remove faulty resistors or capacitors; first clip them from their leads, then heat the solder on the foil and allow each lead to fall out of its hole. Preshape the leads of the replacement part and insert them into the holes in the circuit board. Solder the leads to the foil and cut off the excess lead lengths.

You can remove transistors in the same manner as resistors and capacitors. Make sure you install the replacement transistor with its leads in the proper holes. Then solder the leads quickly to avoid heat damage. Cut off the excess lead lengths.

FOIL REPAIR

To repair a break in a circuit board foil, bridge solder across the break. Bridge large gaps in the foil with bare wire. Lay the wire across the gap and solder each end to the foil. Carefully trim off any excess bare wire.

Troubleshooting Chart

PROBLEM	POSSIBLE CAUSE
LED101 does not light.	1. 5-volt supply, IC133. 2. IC102. 3. LED101.
Space detector does not adjust, but PLL adjusts OK.	1. IC101, IC102, IC103. 2. R113.
PLL does not adjust, but space detector adjusts OK.	1. IC106, IC107, IC108. 2. R119. 3. Hi/Lo jumper wires installed incorrectly.
Both space detector and PLL will not adjust.	1. Y101. 2. IC112, IC113, IC114, IC115, IC116.
Both adjustments are OK, but neither cassette nor serial I/O will communicate with CPU.	1. Port interchange switch not in NORM position. 2. Wrong port numbers jumpered. 3. IC118, IC125, IC126, IC127, IC131, IC132
Cassette interface inoperative. Both adjustments OK. Serial I/O OK.	1. Cables improperly connected. 2. Tape. 3. "Tape Tx" not connected to 1200 baud clock. 4. IC104, IC105, IC111, IC123.
Serial I/O interface inoperative. Cassette interface OK.	1. Cables improperly connected. 2. Wrong clock jumpered for terminal used. 3. Wrong signal levels selected or improperly jumpered. 4. Q103, Q104, Q105. 5. IC119, IC121, IC122, IC124.
Cassette interface erratic.	1. Low quality tapes used. 2. Dirty tape heads. 3. Worn tape machine. 4. Level, or tone, or both not adjusted properly. 5. Loose cables. 6. Adjustments not performed properly.
Cassette motor continues to run after load or dump is complete.	1. RL101, RL102. 2. Q101, Q102.

RECALIBRATION

Your Serial I/O and Cassette Interface Card was accurately calibrated at the factory. However, if you find it necessary to recalibrate the Card (due to a component change, for example), use the following procedure.

Refer to Pictorial 4-1 (Illustration Booklet, Page 3) for the following steps.

1. Be sure switch SW101 is set to NORM.

2. Looking at the controls from the top of the Computer, turn the PLL ADJ control and the SPACE DET ADJ control fully clockwise.

3. Connect a suitable length of hookup wire between circuit board holes TL and TP1.

4. Connect a suitable length of hookup wire between circuit board holes TP3 and TP4.

5. Turn the Computer. LED101 should light.

6. Turn the SPACE DET ADJ control counterclockwise until LED101 just goes out.

7. Turn off the computer.

8. Disconnect both hookup wires.

9. Connect the hookup wire from TL to TP2.

10. Turn on the Computer.

11. Slowly adjust the PLL ADJ control fully counterclockwise. As you turn the control, notice the point (or points) where the LED flickers.

12. Set the PLL ADJ control to the point where the LED flickers (or where it flickers most predominantly if there is more than one point).

13. Slowly adjust the control through this point of flickering once or twice and then set it at the "null." (As you turned the control, the flickering slowed down, virtually stopped, and then started flickering again.) The "null" is where the LED slows down and virtually stops between the two positions where it was flickering.

14. Remove the hookup wire.

    Reconnect the hookup wire from TL to TP1. NOTE: You will leave the wire in this position. The LED will now always monitor tape input data.

PARTS LIST

NOTE: The following circuit component numbers correspond to the numbers on the Schematic, X-Ray View, and any related figures.

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
CAPACITORS		
C101	27-73	.047 μF Mylar*
C102	25-221	2.2 μF tantalum
C103, C104	21-163	1000 pF (.001 μF) ceramic
C105	27-73	.047 μF Mylar
C106	21-163	1000 pF (.001 μF) ceramic
C107 (300 baud)	29-5	1000 pF (.001μF) polystyrene
C107 (1200 baud)	20-111	230 pF mica
C108	27-73	.047 μF Mylar
C109	25-221	2.2 μF tantalum
C110	NOT USED	
C111	25-253	33 μF tantalum
C112	21-27	5000 pF (.005 μF6 ceramic
C113	21-6	27 pF ceramic
C114	21-176	.01 μF ceramic
C115-C117	21-95	.1 μF ceramic
C118	NOT USED	
C119	21-95	.1 μF ceramic
C120	NOT USED	
C121-C125	21-95	.1 μF ceramic
C126	NOT USED	
C127-C129	21-95	.1 μF ceramic
C130	NOT USED	
C131	25-221	2.2 μF tantalum
DIODES — INTEGRATED CIRCUITS (IC s) — LED		
D101-D103	56-56	1N4149 diode
D104	NOT USED	
D105-D108	56-56	1N4149 diode
IC101	443-90	SN74123N IC
IC102	442-616	LM3302N, LM3901, or μA775 IC

CIRCUIT Comp. No.	HEATH Part No.	DESCRIPTION
Diodes — Integrated Circuits (IC s) — LED (cont'd.)		
IC103	443-90	SN74123N IC
IC104, IC105	443-730	SN74LS74N IC
IC106	442-647	CD4046AE IC
IC107	443-640	SN7493AN IC
IC108	443-728	SN74LS00N IC
IC109, IC110	NOT USED	
IC111	443-828	SN74LS73N IC
IC112	443-18	SN7404N IC
IC113, IC114	443-757	SN74LS161 IC
IC115, IC116	443-640	SN7493AN IC
IC117	443-45	SN7408N IC
IC118	443-728	SN74LS00N IC
IC119	443-808	4N26 IC
IC120	NOT USED	
IC121	443-808	4N26 IC
IC122	443-728	SN74LS00N IC
IC123, IC124	443-776	8251 IC
IC125	443-53	SN7442N IC
IC126	443-882	SN74LS139 IC
IC127	443-858	SN7414N IC
IC128, IC129	443-54	SN7403N IC
IC130	NOT USED	
IC131, IC132	443-754	SN74LS240N IC
IC133	442-54	μA7805 IC
LED101	412-611	LED
TRANSISTORS		
Q101, Q102	417-821	MPSA06
Q103	417-865	MPSA55
Q104	417-897	FET (selected)
Q105-Q107	417-821	MPSA06
RESISTORS		
(All resistors are 1/4-watt, 5% unless otherwise listed.)		
R101	6-101	100 Ω, 1/2-watt
R102	6-103-12	10 kΩ

*DuPont Registered Trademark

Resistors (cont'd.)

R103, R104	6-102-12	1000 Ω
R105	6-103-12	10 kΩ
R106	6-104-12	100 kΩ
R107	6-332-12	3300 Ω
R108	6-104-12	100 kΩ
R109	6-102-12	1000 Ω
R110	NOT USED	
R111, R112	6-103-12	10 kΩ
R113	10-222	50 kΩ control
R114-117	6-103-12	10 kΩ
R118	6-473-12	47 kΩ
R119	10-317	200 kΩ control
R120	NOT USED	
R121	6-105-12	1 MΩ
R122	6-104-12	100 kΩ
R123	6-102-12	1000 Ω
R124-R126	6-472-12	4700 Ω
R127, R128	6-399	3.9 Ω, 1/2-watt
R129	6-103-12	10 kΩ
R130	6-472-12	4700 Ω
R131	6-101	100 Ω, 1/2-watt
R132	6-154-12	150 kΩ
R133	6-103-12	10 kΩ
R134	6-472-12	4700 Ω
R135, R136	6-104-12	100 kΩ
R137	6-103-12	10 kΩ
R138	6-102-12	1000 Ω

Resistors (cont'd.)

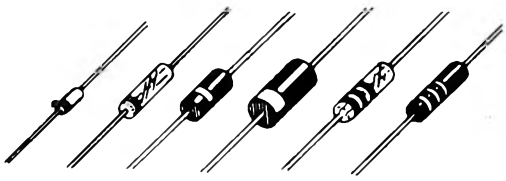
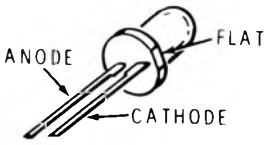
R139	6-151	150 Ω, 1/2-watt
R140	NOT USED	
R141-R144	6-681	680 Ω, 1/2-watt
R145	6-222	2200 Ω, 1/2-watt
R146	6-683-12	68 kΩ
R147	6-151	150 Ω, 1/2-watt
R148	6-472-12	4700 Ω
R149	6-102-12	1000 Ω
R150	NOT USED	
R151, R152	6-681	680 Ω, 1/2-watt
R153-R157	6-472-12	4700 Ω
R158	6-104-12	100 kΩ
R159	6-103-12	10 kΩ
R160	NOT USED	
R161	6-332-12	3300 Ω
R162-R164	6-103-12	10 kΩ
R165	6-561	560 Ω, 1/2-watt

MISCELLANEOUS

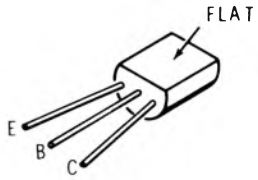
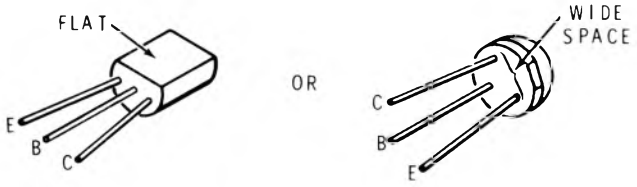
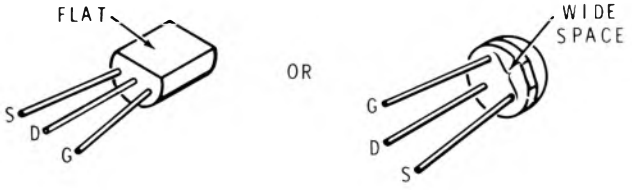
L101	40-961	100 μH coil
RL101, RL102	65-49	Reed switch
SW101	60-604	Slide switch
Y101	404-536	4.0 MHz crystal
	40-1667	Inductor (for reed relay)

SEMICONDUCTOR IDENTIFICATION CHARTS

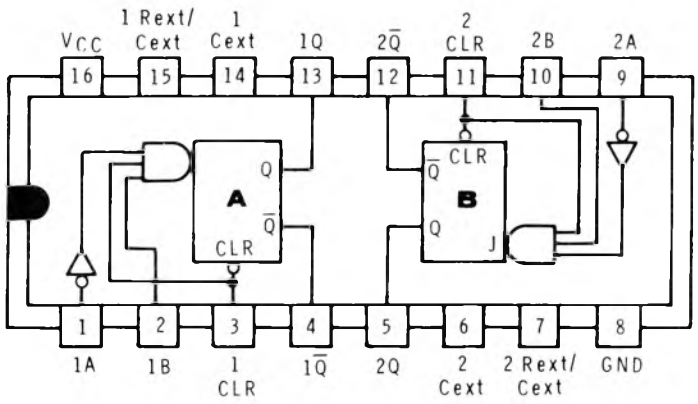
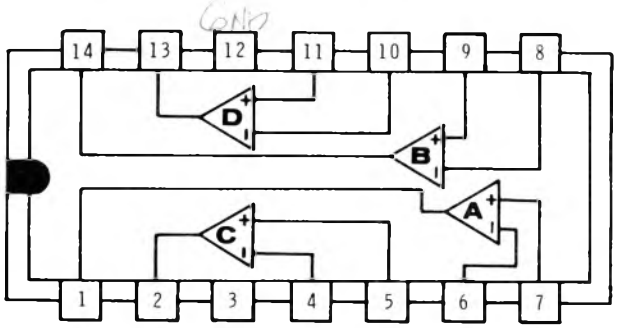
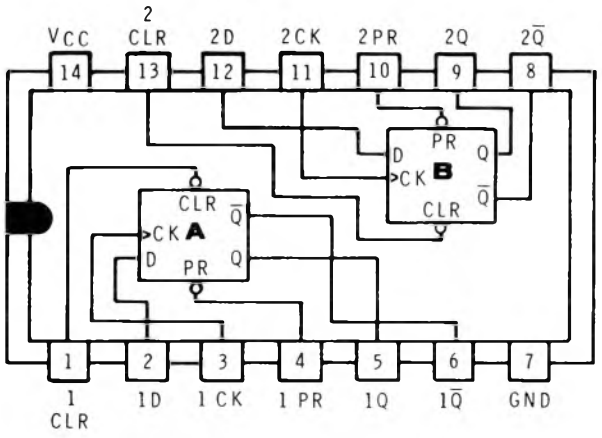
DIODES

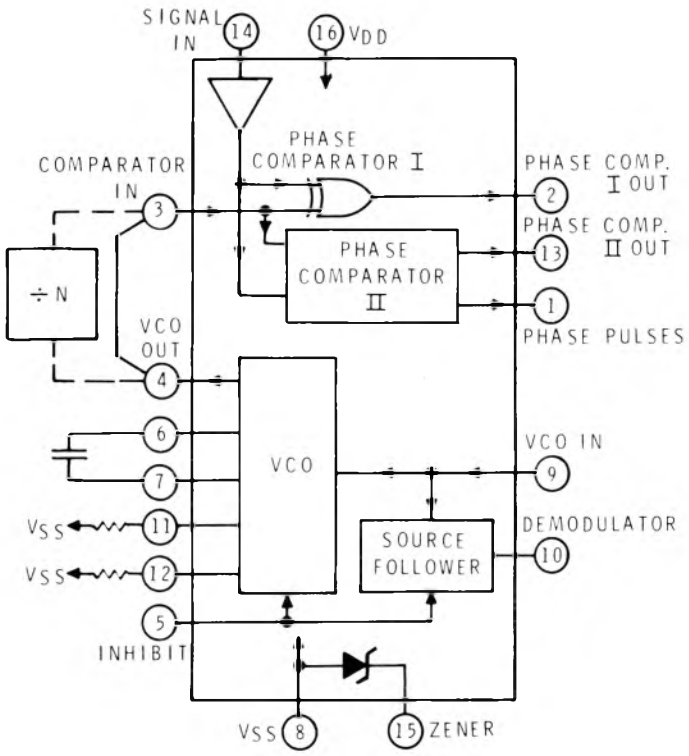
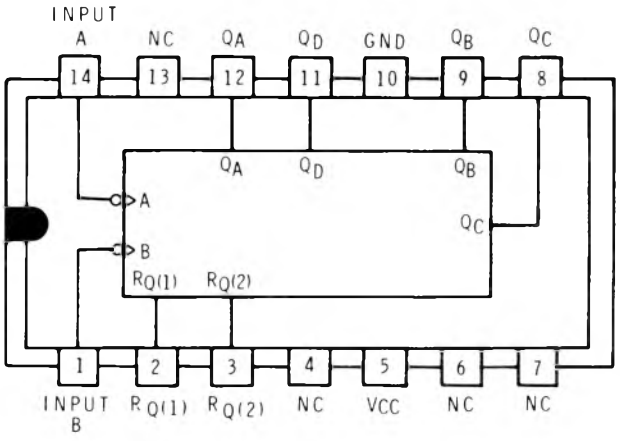
COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
D101, D102, D103, D105, D106, D107, D108	56-56	1N4149	
LED101	412-611		

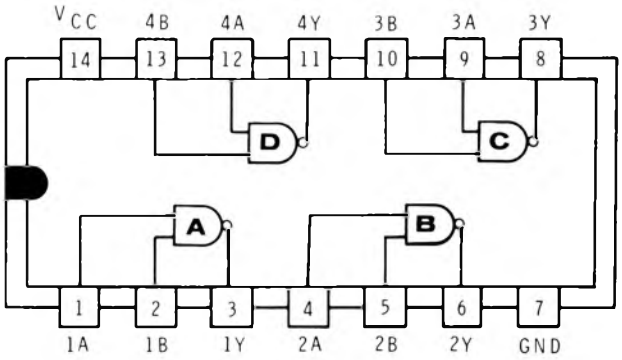
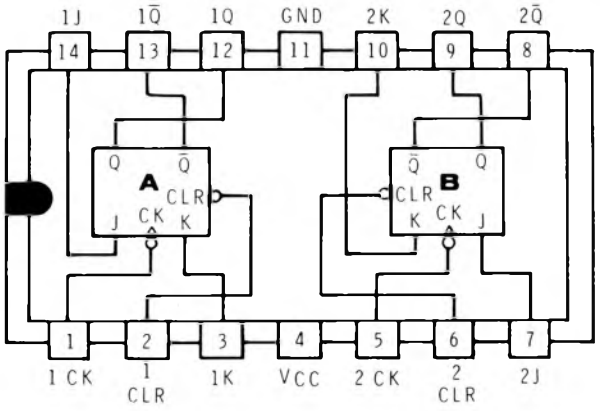
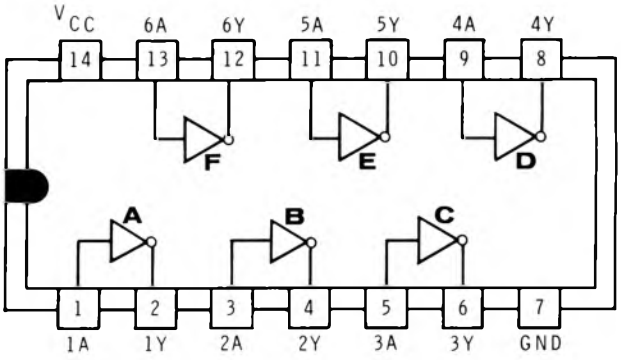
TRANSISTORS

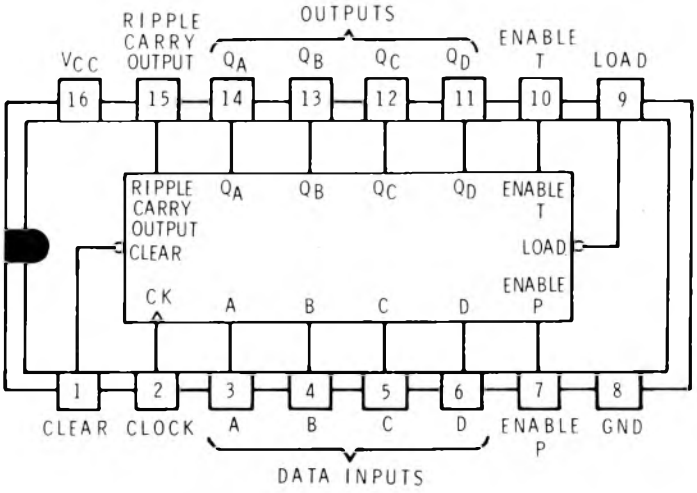
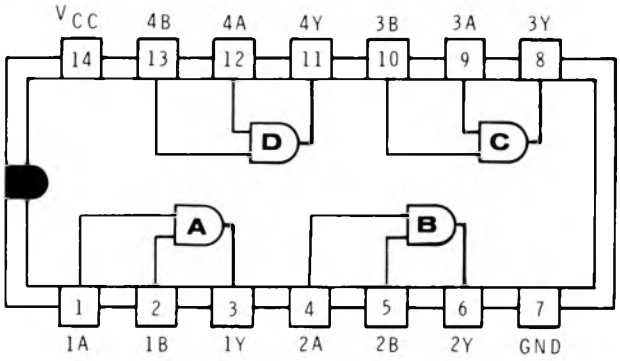
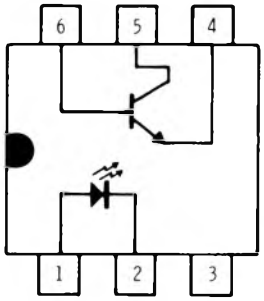
COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
Q101, Q102, Q105, Q106, Q107	417-821	MPSA06	
Q103	417-865	MPSA55	
Q104	417-897	SELECTED	

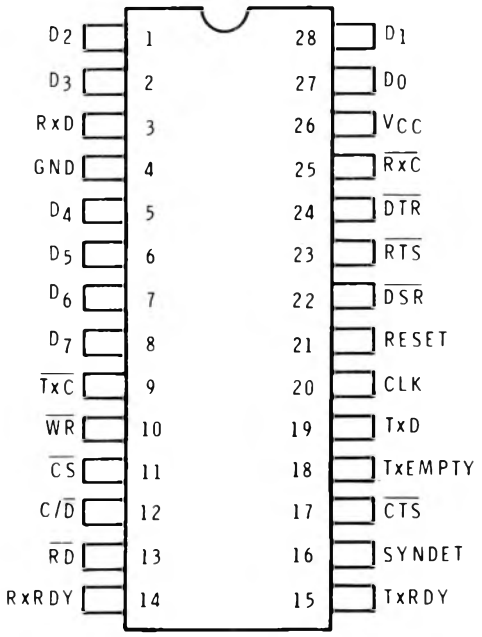
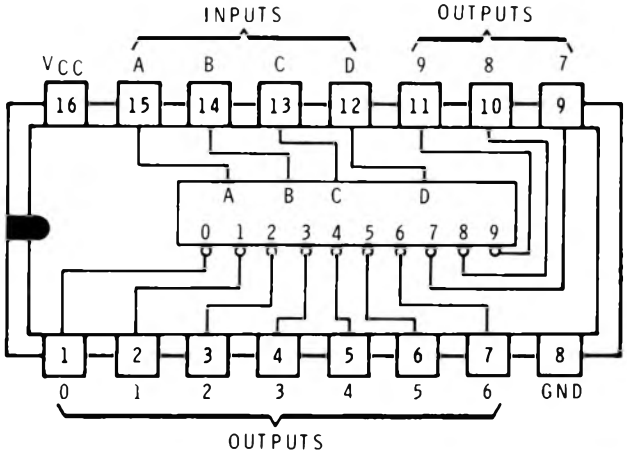
INTEGRATED CIRCUITS

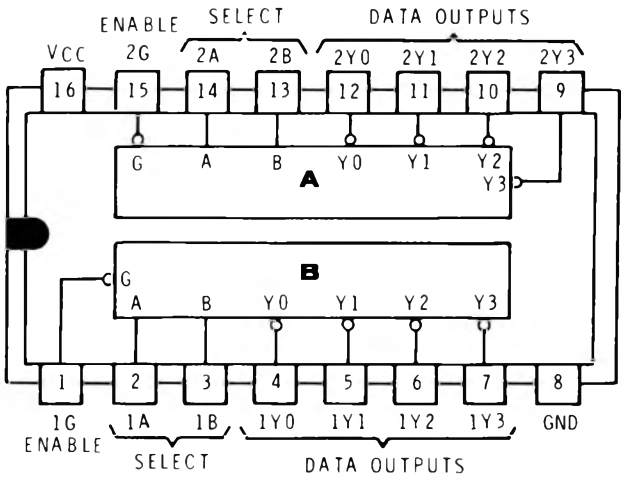
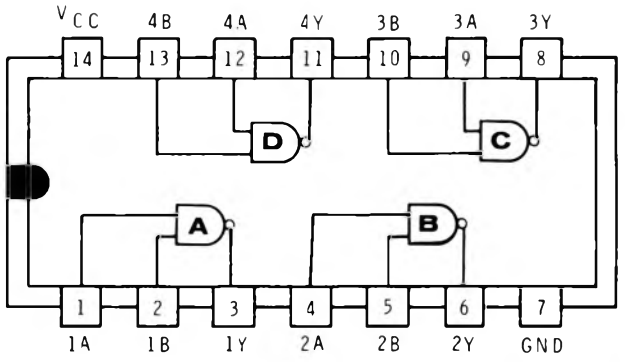
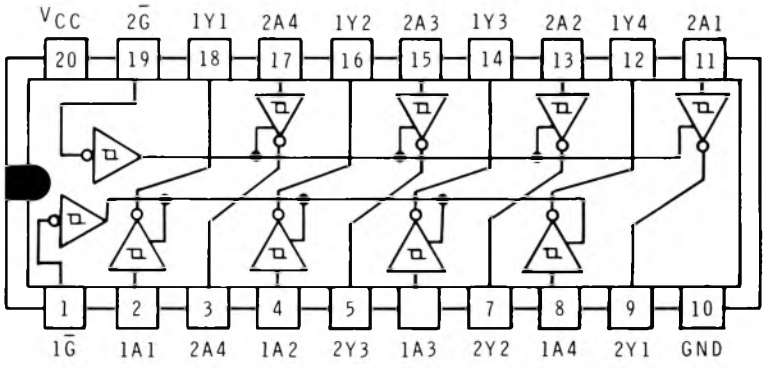
COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
IC101, IC103	443-90	SN74123	
IC102	442-616	LM3302, LM2901, or µA775	
IC104, IC105,	443-730	SN74LS74N	

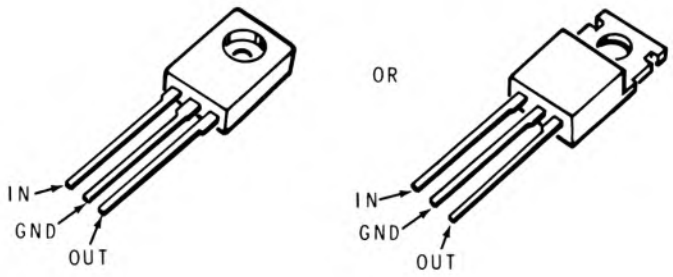
COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
IC106	442-647	CD4046	
IC107, IC115, IC116	443-640	SN7493N	

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
IC108, IC118, IC122	443-728	SN74LS00N	
IC111	443-828	SN74LS73N	
IC112	443-18	SN7404N	
IC127	443-858	SN74LS04N	

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
IC113, IC114	443-757	SN74LS161N	
IC117	443-45	SN7408	
IC119, IC121	443-808	4N26	

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
IC123, IC124	443-776	8251	
IC125	443-53	SN7442	

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
IC126	443-822	SN74LS139	
IC128, IC129	443-54	SN7403	
IC131, IC132	443-754	SN74LS240	

COMPONENT	HEATH PART NUMBER	MAY BE REPLACED BY	IDENTIFICATION
IC133	442-54	µA7805	

SERVICE INFORMATION

The following Heath Company services are available if you need them: Replacement Parts, Technical Consultation, and Factory Service. Address all correspondence to:

HEATH COMPANY
Benton Harbor, Michigan 49022

For prompt service, use a separate letter for each department you write to.

Replacement parts and repair service are also available at your nearest Authorized Service Center or Heath Electronic Center. These Centers are listed in your Heath Catalog.

REPLACEMENT PARTS

If a replacement part is needed, please include the following information in your letter:

1. Part number and description.
2. Model Number and Series Number of the equipment.

If your equipment is in the Warranty period, add:

3. Date of purchase.
4. Nature of defect.

Heath Company will fill your order promptly. Please DO NOT RETURN PARTS unless they are requested. Parts that are damaged through carelessness or misuse by the customer will not be replaced without cost.

TECHNICAL CONSULTATION

You can write to our Technical Consultants for help with any Heath equipment, or for answers to any questions about the use of this equipment.

The completeness and accuracy of the advice mailed back to you depends entirely on the information in your letter. Be sure to include:

1. The Model Number and Series Number of the equipment (on blue and white identification label).
2. Date of purchase.
3. An exact description of the difficulty. Include switch positions, connections to other units, operating procedures, voltage reading, and any other information you think might be helpful.
4. List everything you have done in attempting to correct the difficulty.

FACTORY SERVICE

If you do not have qualified repair services at your disposal, you can return your equipment to the Heath Company Service Department to have it repaired for a minimum service fee. (Equipment that has been modified will not be accepted for repair.) Refer to Shipping Instructions for details on how to package and ship the equipment.

To be eligible for replacement parts under the terms of the Warranty, equipment returned for factory service must be accompanied by the invoice or the sales slip, or a copy of either. (If you send the original invoice or sales slip, it will be returned to you.)

SHIPPING INSTRUCTIONS

Check the equipment to see that all parts are in place. Then, wrap the equipment in heavy paper. Place the equipment in a strong carton, and put at least three inches of resilient packing material (shredded paper, excelsior, etc.) on all sides between the equipment and the carton.

Seal the carton with gummed paper tape and tie it with a strong cord. Ship it by prepaid Express or insured Parcel Post to:

HEATH COMPANY
Benton Harbor, Michigan 49022

Attach a letter, containing the following information to the outside of the carton:

1. Your name and return address.
2. Date of purchase.
3. A brief description of the difficulty.
4. Your authorization to ship the repaired unit back to you C.O.D. for the service and shipping charges, plus the cost of parts not covered by the Warranty.

YOUR HEATH FACTORY ASSEMBLED PRODUCT ONE-YEAR LIMITED WARRANTY

If you are not satisfied with our service - warranty or otherwise, or with our products, write directly to our Director of Customer Services, Heath Company, Benton Harbor, Michigan 49022. He will make certain your problems receive immediate, personal attention.

Our attorney insists that we describe our warranty using all the necessary legal phrases in order to comply with the new warranty regulations. Fine. Here they are:

For a period of one year after purchase, Heath Company will replace or repair free of charge any product that is defective either in materials or workmanship. We warrant that during the first full year after purchase, our products, when used in accordance with our printed instructions, will meet published specifications.

If your Heath factory-assembled product malfunctions or fails to operate at any time during the warranty period, through no fault of yours, we will service it free upon proof of purchase and delivery at your expense to the Heath factory, or any Heathkit Electronic Center (units of Schlumberger Products Corporation), or any of our authorized overseas distributors.

You will receive free consultation on any problem you might encounter in the use of your Heath product. Just drop us a line or give us a call. Sorry, we cannot accept collect calls.

Our warranty does not cover and we are not responsible for damage caused by misuse or fire or unauthorized modifications to or uses of our products for purposes other than advertised. Our warranty does not include reimbursement for customer assembly or set-up time.

This warranty covers only Heath factory assembled products and is not extended to allied equipment or components used in conjunction with these products. **We are not responsible for incidental or consequential damages.** Some states do not allow the exclusion or limitation of incidental or consequential damages, so the above limitation or exclusion may not apply to you. This warranty gives you specific legal rights, and you may also have other rights which vary from state to state.

HEATH COMPANY
BENTON HARBOR, MI. 49022

The Heath Company reserves the right to discontinue products and to change specifications at any time without incurring any obligation to incorporate new features in products previously sold.

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