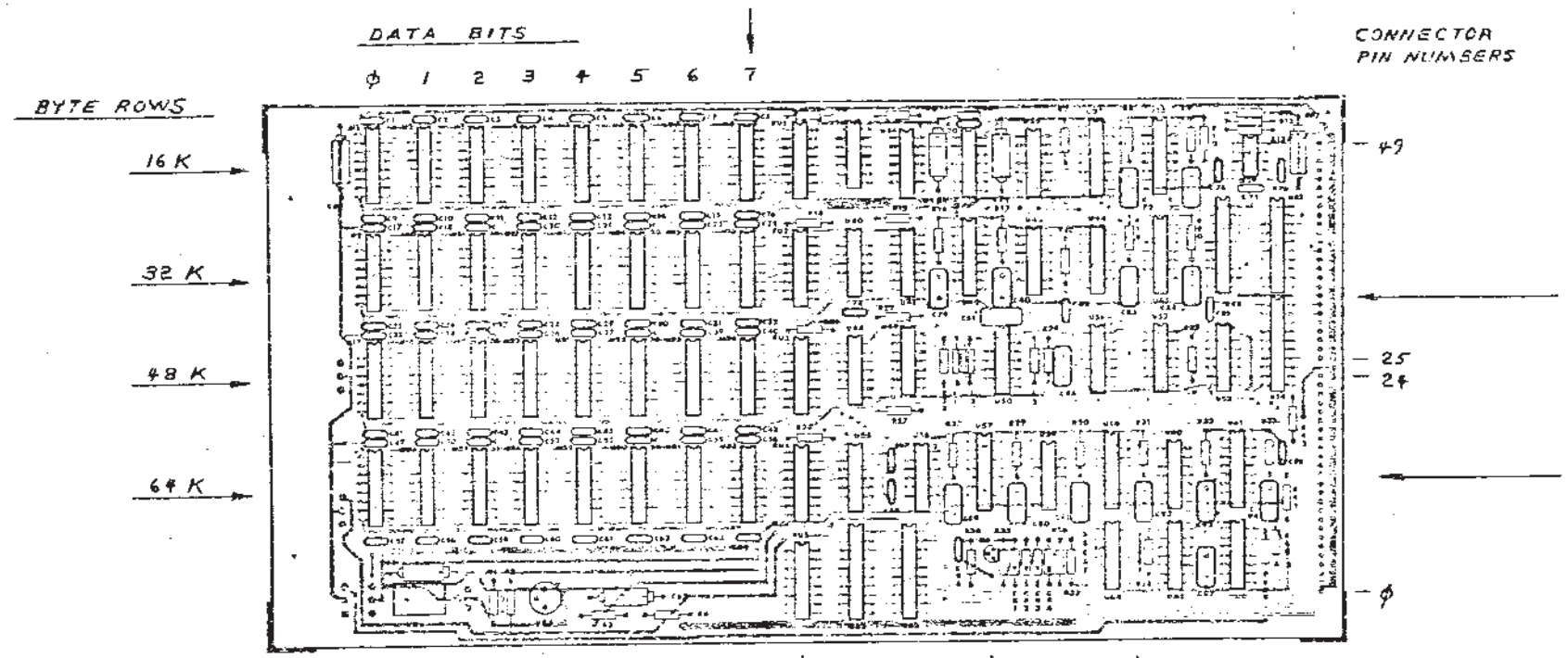
- POPULATE MEMORY STARTING WITH TOP (16K) ROW OF EIGHT MEMORY CHIPS.
- ADD MEMORY CHIPS ONE ROW AT A TIME IN A CONTIGUOUS MANNER TO EXTEND MEMORY CAPACITY. EACH ROW IS AN ADDITIONAL 16K BYTES. BE SURE TO CHANGE ADDRESSING JUMPER (BELOW) ACCORDINGLY.



CAUTION:

THE MEMORY CHIPS ARE MOS DEVICES AND ARE SUSCEPTABLE TO DAMAGE BY STATIC ELECTRICITY WHILE BEING HANDLED BEFORE INSTALLATION.

CONTRACT NO.		TRIONYX ELECTRONICS
DRAWN		DWG TITLE: M-H8 ASSEMBLY DRAWING
CHECK		
ENGR		
PROJ. ENGR		
PROD. DESIGN		SIZE: D; CODE IDENT NO.; DWG NO.: TE-A-100100
OTHER APPROVALS		SCALE: ; SHEET 1 OF 1

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

INI-L

BMP-L

SRC-H

STL-L

20 ROYIN

MEM-R 28 — 74S04 U43 — 7400 U52 — 7408 U50 — 7408 U50 — DSR-H

MEM-W 23 — 74S04 U43

C81 680 PF — 30 NS TIMING DELAY

MEMORY TIMING AND REFRESH CIRCUITS (SEE SHEET 2)

REF-H — 7408 U51 — L1 8.2 µH — 7408 U50 — L2-N.U. — R23 220Ω — 60 NS TIMING DELAY

REF-L

7400 U52 — MUX-H

74S04 U43 — 7400 U52 — MUX-L

74S04 U41 — R5 39Ω — CAS φ-L

74S04 U41 — R14 39Ω — CAS 1-L

7408 U51 — L3-22µH — 7408 U50 — R24 220Ω — C86 100PF — 90 NS TIMING DELAY

74S04 U49 — R21 39Ω — CAS 2-L

74S04 U49 — R26 39Ω — CAS 3-L

+5V3 — R17 18K — C80 33PF — 74123 — 100 NS U42 — +VB1

+5V3 — R16 18K — C79 N.U. — 74123 — 100 NS U42 — +VB1

74S04 U41 — RU1-39Ω — WRT φ-L

74S04 U41 — RU2-39Ω — WRT 1-L

74S04 U49 — RU3-39Ω — WRT 2-L

74S04 U49 — RU4-39Ω — WRT 3-L

MCS-H

RRS-H

SEL-H

74LS138 U37

A13

A14 44

A15 45

+VB1

ADDRESS DECODER

7400 U36

74S51 U37 — R6 39Ω — RAS φ-L

DCA-1

74S51 U34 — R15 39Ω — RAS 1-L

DCA-2

74S51 U35 — R22 39Ω — RAS 2-L

DCA-3

74S51 U35 — R27 39Ω — RAS 3-L

DATA BUS BUFFERS

74LS373 U63 — 74LS373 U62 — RESISTOR MODULE 39Ω-EACH RU5

DO-φ … DO-7 — 1φ-D0 … 17-D7 — DI-φ … DI-7

+VB3

DOE-L

MEMORY CONTROL CIRCUITS

H8 BUS CONNECTION

N.U. - NOT USED

TRIONYX ELECTRONICS

SIZE	CODE IDENT NO.	DWG NO.
D		TE-5-100100
SCALE:		SHEET 1 OF 4

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REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

MEMORY TIMING CIRCUITS AND REFRESH SYNCHRONIZATION —

MEMORY CYCLE TIMING CIRCUITS

DSR-H
SRC-H
BMR-L
DCA-1
DCA-2
DCA-3
SEL-H

+VB2 7474 U74 D

7400 U52 — 74S04 U56 — MCS-H

+VB2 7474 U48 D — 74S04 U56 — 7402 U60

7402 U60 — DOE-L

R41 330Ω +5V4 — 7438 U66 — B 8-24K (16K)

7402 U64 — DCA-1 / DCA-2 — C 8-40K (32K)

7402 U64 — A COMMON (ENABLE-LOW)

7402 U64 — DCA-3 — D 8-56K (48K)

74S04 U43 — SEL-H — E 8-64K (56K)

SELECT ADDRESS RANGE — CONNECT PAD "A" TO THE PAD CORRESPONDING TO INSTALLED MEMORY CAPACITY

+5V3 R28 22K C89 56PF 74123 400 NS U57 — +VB3

SYNCHRONOUS REFRESH

+VB3 7474 U58 D

+5V4 R20 18K C84 56PF 74123 450 NS U45 — +VB5

+5V4 R19 10K C83 N.U. 74123 50 NS U45 — +VB5

+5V4 R11 4.7K R12 15K U 39 NE555 C72 10PF R8 10K 74123 100 NS U38 R13 100Ω C74 1000.pf 470PF C76 .1 μF — +VB4

20 MICROSECOND PERIOD REFRESH TIMER

+5V4 1000.pf C73 470PF R9 39K 74123 5 μS U38

5 μS REFRESH TIMING ENABLE PULSE

+VB6 7474 U58 D — 7408 U51 — 7402 U60

74S04 U56 — 74S04 U56 — 74S04 U56 — C88 3300PF — ASSYNCHRONOUS REFRESH

R40 330Ω +5V4 — 7438 U66

REFRESH CYCLE TIMING CIRCUITS

+VB6 7474 U74 D — 7402 U60 — DOE-L

+5V3 R30 16K C91 33PF 74123 250 NS U59 — RAS-H — +VB

+5V3 R29 12K C90 33PF 74123 200 NS U57 — +VB3

+5V4 R32 18K C93 56PF 74123 400 NS U61 — +VB6

+5V4 R33 18K C94 22PF 74123 150 NS U61 — +VB6

7402 U60 — INI-L

+VB6 7474 U65 D — 7438 U66 — R39 1K +5V4 — STL-L

7408 U51 — REF-H

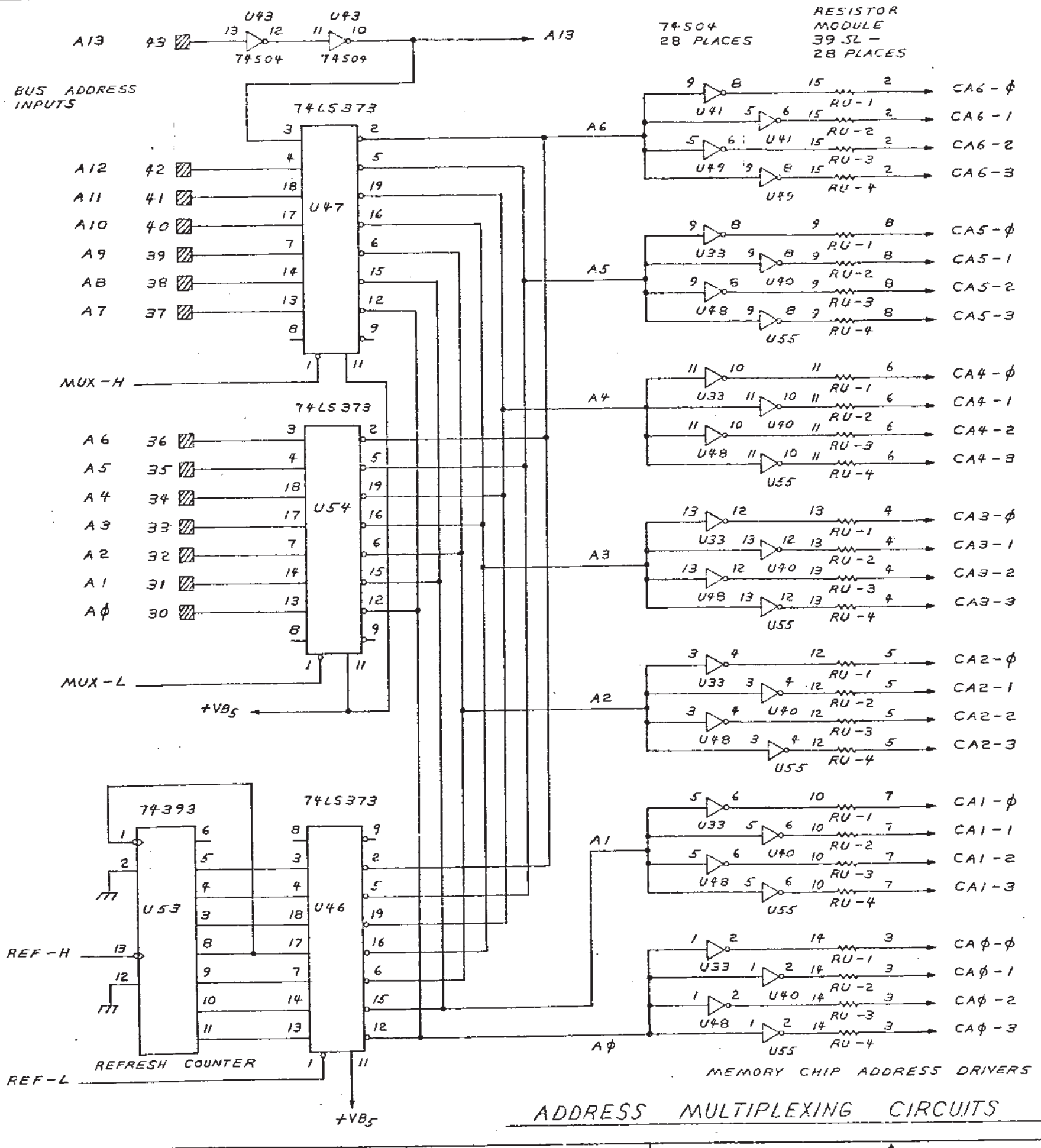
C97 560PF

+5V3 R31 27K C92 33PF 74123 250 NS U59 — REF-L — +VB4

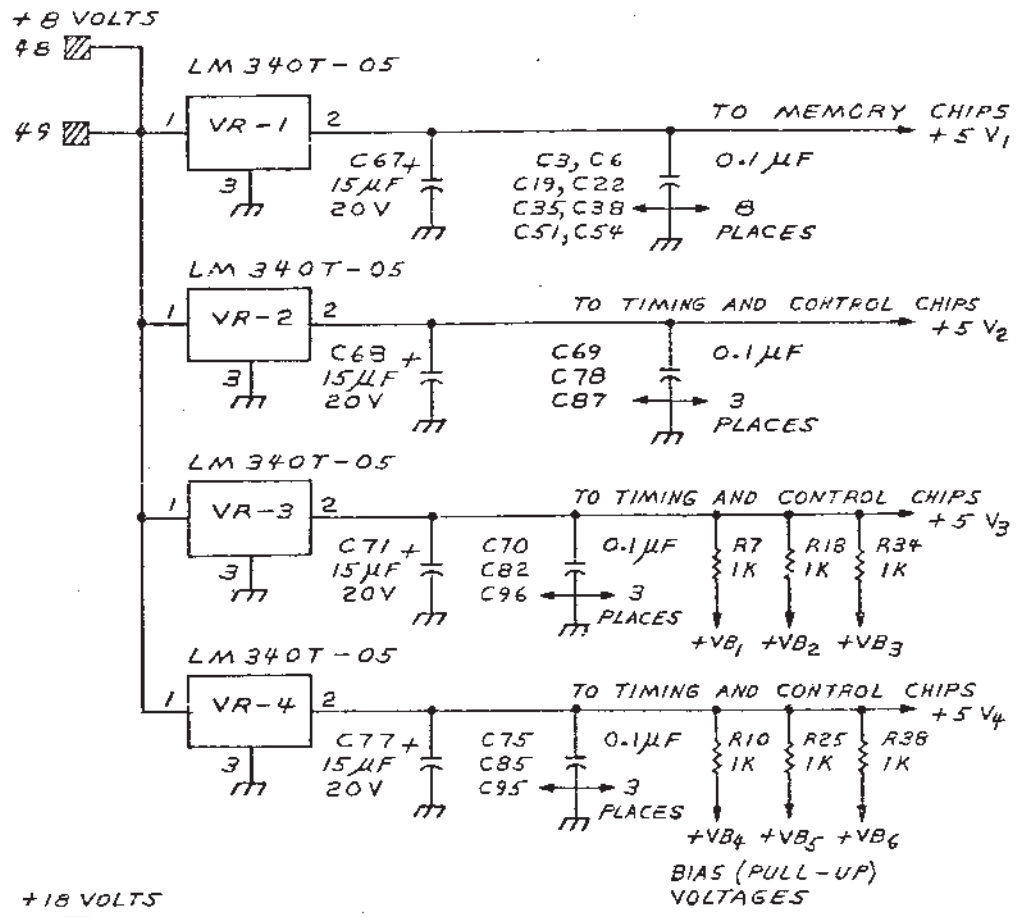
+5V4 R42 330Ω — 7438 U66 (UNUSED GATE)

SIZE	CODE IDENT NO.	DWG NO.
D		TE-S-100100
SCALE:		SHEET 2 OF 4
		DISTR NO.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

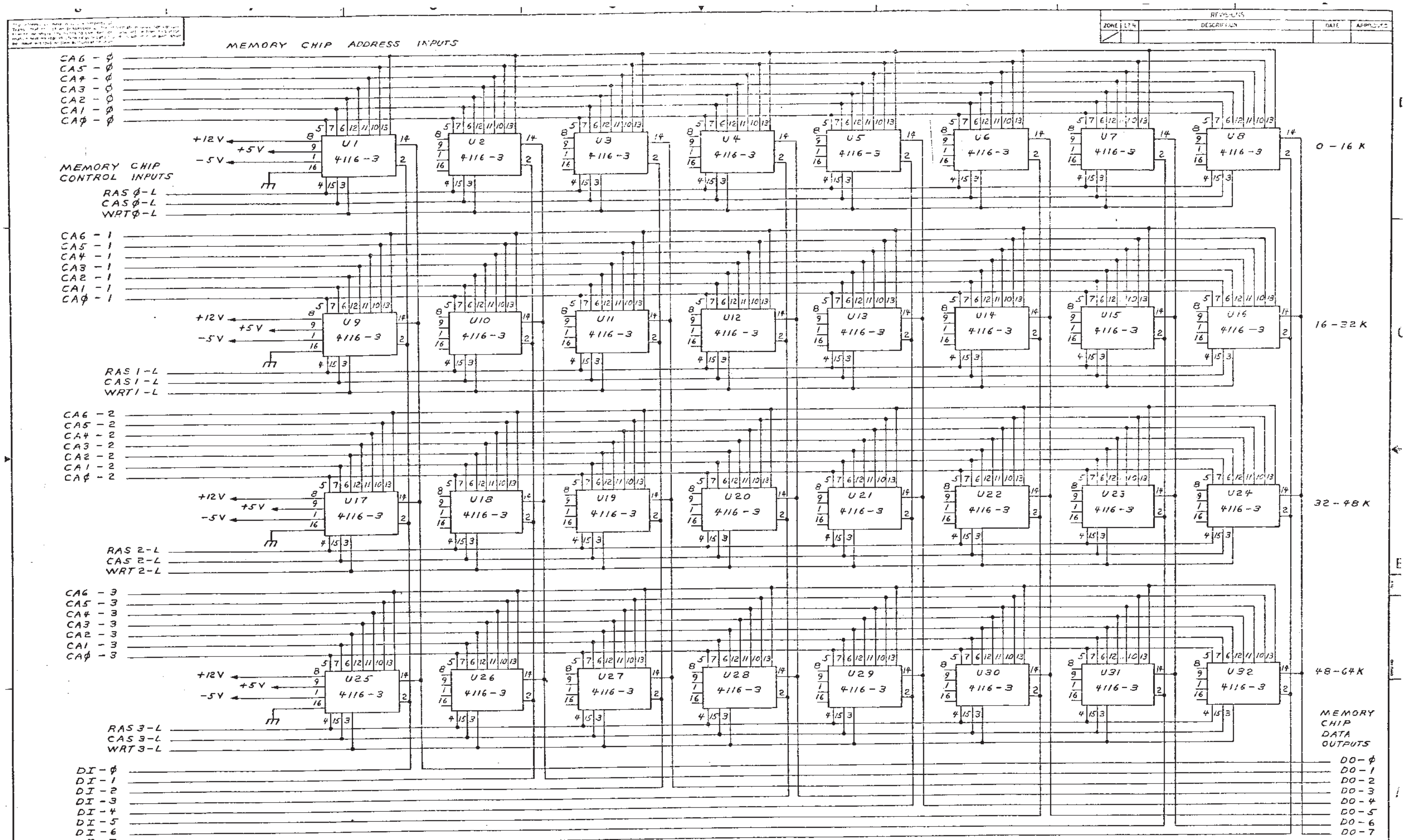


ADDRESS MULTIPLEXING CIRCUITS



POWER SUPPLY CIRCUITS

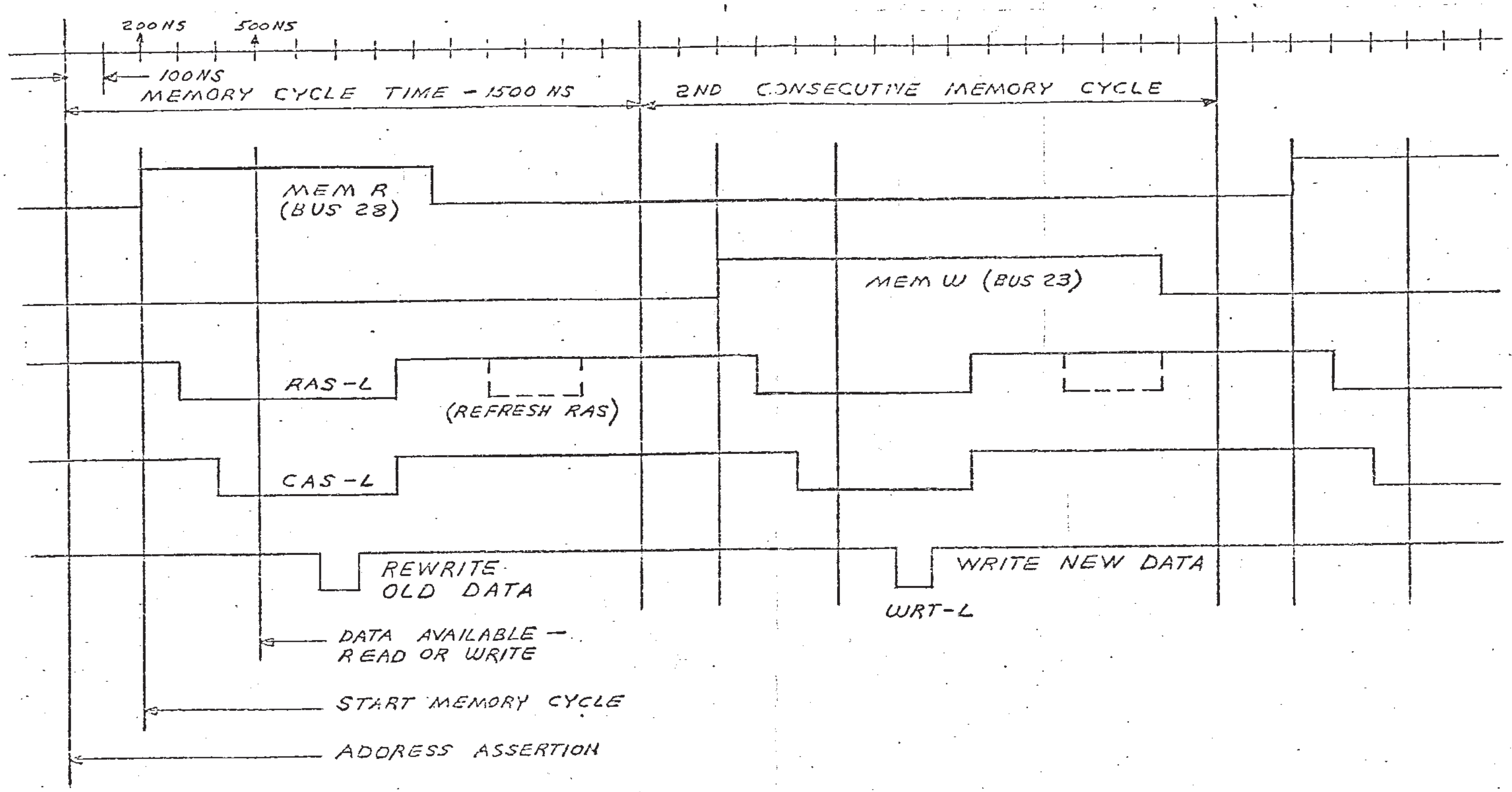
SIZE	CODE IDENT NO.	DWG NO.
D		TE-S-100100
SCALE:		SHEET 3 OF 4
		DISTR NO.



MEMORY DATA STORAGE DEVICE ARRAY (64 K x 8 BITS)

SIZE	CODE IDENT NO.	DWG NO.
D		TE-S-100100
SCALE:		SHEET 4 OF 4

DISTR NO.



MEMORY INTERFACE TIMING RELATIONSHIPS