When you set up your system, you may have to experiment to find the best settings for the volume control, tone control, or both. The tone control is normally set to midrange or toward the treble end. The volume control is not critical on playback once the minimum level is reached. Increasing the volume will sometimes be helpful when using poor recordings.

If your recorder has an automatic level control, defeat it if possible. Use the record level control to set the level to the highest level before overloading.

If you want to use a cassette deck that does not have a power amplifier, remove R101 from the Serial I/O and Cassette Interface Card to raise the impedance of the audio input.

If you have two tape machines, you can use one for playback while you record on the other. To do this, use the audio cable and the 2-wire cable with black tubing for the playback machine. Use the other two cables for the recording machines. See the inset drawing on Pictorial 4-4.

CASSETTE INTERFACE DISABLE

When you use the H10 Reader/Punch and the H8-2 Parallel Card as the load/dump port, the Cassette Interface must be disabled. To do this, remove the "Y" to "O" port select jumper. Be sure to disable the parallel port at address 370 and reinstall this jumper when you want to use the Cassette Interface again.

PROGRAMMING CONSIDERATIONS

The 8251 USARTs (IC123 and IC124) perform the serial-to-parallel data conversion and are very flexible devices. The manner in which they perform the conversion is determined by the external clocks and the control words sent from the central processing unit. For most applications, the software supplied by Heath Company will automatically take care of this. However, for specialized applications, you might need to know how to initialize and use these devices.

The following is a general set of requirements needed to properly operate the USARTs. This information is then followed by more technical and detailed information.

The following sequence of events must happen for a USART to work properly:

1. At power-up, or following a master reset, the USART is reset.

2. A MODE INSTRUCTION is sent to the USART defining the following characteristics of the I/O channel:

    ● Clock rate.

    ● Character length.

    ● Parity.

    ● Number of stop bits.

The Mode Instruction is a word sent by the CPU to the USART register at the odd-numbered port of the two ports assigned to each USART. The normal mode instruction for the Heath system is 116, which programs the USART for standard asynchronous operation.

3. A COMMAND INSTRUCTION is sent to the same port as the mode instruction. This word controls the actual operation of the USART. It enables portions of the circuitry, sets various bits, and resets the error flags.

4. A STATUS WORD may be read from this same port. It allows the CPU to determine when data may be transferred, which bits are set, and which errors have occurred.

5. Data is transferred between the USART and the CPU through the even-numbered port of the two ports assigned to each USART. (This is the port number which is actually programmed at the port decoder.) The mode and command instructions use the next higher port number.

NOTE: A New Command Instruction may be sent to the USART at any time. If, however, the USART had a character in its transmit buffer, that character would be lost.
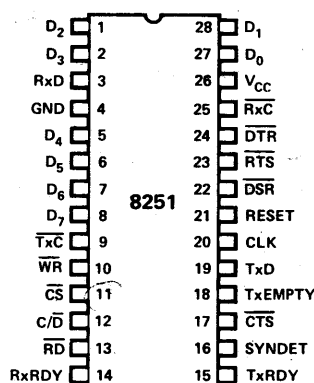
USART DESCRIPTION

The following is Manufacturer's data concerning the USART and is supplied for your information. However, not all the information is applicable to your Serial Card.

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) Chip designed for data communications in microcomputer systems. The USART is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM Bi-Sync). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPT. The chip is constructed using N-channel silicon gate technology. See Pictorial 5-4.

The USART has the following features:

- Synchronous and Asynchronous Operation

- Synchronous:
  5-8 Bit Characters
  Internal or External Character
  Synchronization
  Automatic Sync Insertion

- Asynchronous:
  5-8 Bit Characters
  Clock Rate — 1, 16, or 64 Times
  Baud Rate
  Break Character Generation
  1, 1-1/2, or 2 Stop Bits
  False Start Bit Detection

- Baud Rate —DC to 56 k Baud (Sync Mode)
  DC to 9.6 k Baud (Async Mode)

- Full Duplex, Double Buffered, Transmitter and Receiver

- Error Detection — Parity, Overrun, and Framing

- Fully Compatible with 8080 CPU

- 28-Pin DIP Package

- All Inputs and Outputs are TTL Compatible

- Single 5-Volt Supply

- Single TTL Clock

PIN CONFIGURATION

D_2	1	28	D_1
D_3	2	27	D_0
RxD	3	26	V_{CC}
GND	4	25	$\overline{RxC}$
D_4	5	24	$\overline{DTR}$
D_5	6	23	$\overline{RTS}$
D_6	7	22	$\overline{DSR}$
D_7	8	21	RESET
$\overline{TxC}$	9	20	CLK
$\overline{WR}$	10	19	TxD
$\overline{CS}$	11	18	TxEMPTY
$C/\overline{D}$	12	17	$\overline{CTS}$
$\overline{RD}$	13	16	SYNDET
RxRDY	14	15	TxRDY

8251

Pin Name	Pin Function
D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
$\overline{RD}$	Read Data Command
$\overline{WR}$	Write Data or Control Command
$\overline{CS}$	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
$\overline{TxC}$	Transmitter Clock
TxD	Transmitter Data
$\overline{RxC}$	Receiver Clock
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)

Pin Name	Pin Function
$\overline{DSR}$	Data Set Ready
$\overline{DTR}$	Data Terminal Ready
SYNDET	Sync Detect
$\overline{RTS}$	Request to Send Data
$\overline{CTS}$	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

BLOCK DIAGRAM

PICTORIAL 5-4
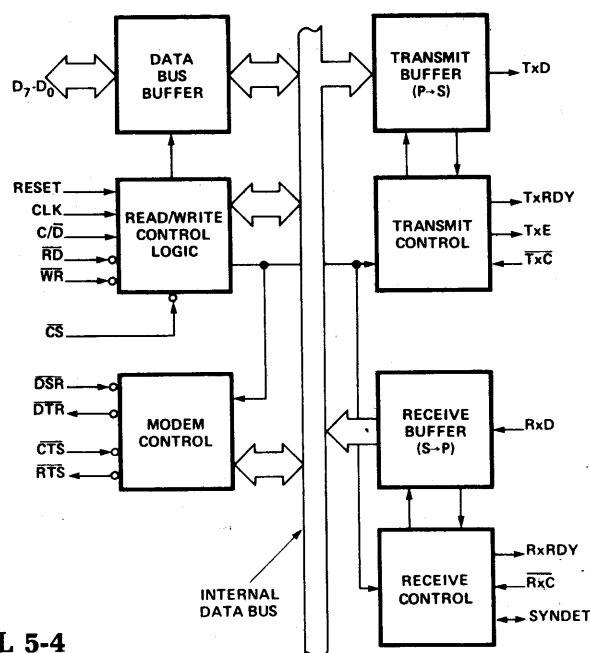
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8251 BASIC FUNCTIONAL DESCRIPTION

General

The 8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter designed specifically for the 8080 Microcomputer System. Like other I/O devices in the 8080 Microcomputer System, its functional configuration is programmed by the system's software for maximum flexibility. The 8251 can support virtually any serial data technique currently in use (including IBM "bi-sync").

In a communication environnement, an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU.

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8251 to the 8080 system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the 8080 CPU. Control words, Command words, and Status information are also transferred through the Data Bus Buffer.

Read/Write Control Logic

This functional block accepts inputs from the 8080 Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for device functional definition.

RESET (Reset) — A "high" on this input forces the 8251 into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251 to program its functional definition.

CLK (Clock) — The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the 8224 Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter clock inputs for synchronous mode (4.5 times for asynchronous mode).

$\overline{\text{WR}}$ (Write) — A "low" on this input informs the 8251 that the CPU is outputting data or control words; in essence, the CPU is writing out to the 8251. See Pictorial 5-5.

C/$\overline{\text{D}}$	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{CS}}$	
0	0	1	0	8251 ⇒ DATA BUS
0	1	0	0	DATA BUS ⇒ 8251
1	0	1	0	STATUS ⇒ DATA BUS
1	1	0	0	DATA BUS ⇒ CONTROL
X	X	X	1	DATA BUS ⇒ 3-STATE

PICTORIAL 5-5

$\overline{\text{RD}}$ (Read) — A "low" on this input informs the 8251 that the CPU is inputting data or status information, in essence, the CPU is reading from the 8251.

C/$\overline{\text{D}}$ (Control/Data) — This input, in conjunction with the $\overline{\text{WR}}$ and $\overline{\text{RD}}$ inputs informs the 8251 that the word on the Data Bus is either a data character, control word, or status information.

1 = CONTROL   0 = DATA

$\overline{\text{CS}}$ (Chip Select) — A "low" on this input enables the 8251. No reading or writing will occur unless the device is selected.

Modem Control

The 8251 has a set of control inputs and outputs that can be used to simplify the interface to almost any Modem. The modem control signals are general-purpose in nature and can be used for functions other than Modem control, if necessary.

$\overline{\text{DSR}}$ (Data Set Ready) — The $\overline{\text{DSR}}$ input signal is general-purpose in nature. Its condition can be tested by the CPU using a Status Read operation. The $\overline{\text{DSR}}$ input is normally used to test Modem conditions such as Data Set Ready.

$\overline{\text{DTR}}$ (Data Terminal Ready) — The $\overline{\text{DTR}}$ output signal is general-purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{\text{DTR}}$ output signal is normally used for Modem control such as Data Terminal Ready or Rate Select.

$\overline{\text{RTS}}$ (Request to Send) — The $\overline{\text{RTS}}$ output signal is general-purpose in nature. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{\text{RTS}}$ output signal is normally used for Modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send) — A "low" on this input enables the 8251 to transmit data (serial) if the Tx EN bit in the Command byte is set to a "one."

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, coverts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique), and outputs a composite serial stream of data on the TxD output pin.

Transmitter Control

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

TxRDY (Transmitter Ready) — This output signals the CPU that the transmitter is ready to accept a data character. It can be used as an interrupt to the system or, for the Polled operation, the CPU can check TxRDY using a status read operation. TxRDY is automatically reset when a character is loaded from the CPU.

TxE (Transmitter Empty) — When the 8251 has no characters to transmit, the TxE output will go "high." It resets automatically upon receiving a character from the CPU. TxE can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplexed operational mode.

In SYNChronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be transmitted automatically as "fillers."

$\overline{TxC}$ (Transmitter Clock) — The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the frequency of $\overline{TxC}$ is equal to the actual Baud Rate (1X). In Asynchronous transmission mode, the frequency of $\overline{TxC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x, or 64x the Baud Rate.

For example:
> If Baud Rate equals 110 Baud,
> $\overline{TxC}$ equals 110 Hz (1x)
> $\overline{TxC}$ equals 1.76 kHz (16x)
> $\overline{TxC}$ equals 7.04 kHz (64x).
> If Baud Rate equals 9600 Baud,
> $\overline{TxC}$ equals 614.4 kHz (64x).

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to the RxD pin.

Receiver Control

This functional block manages all receiver-related activities.

RxRDY (Receiver Ready) — This output indicates that the 8251 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or for Polled operation the CPU can check the condition of RxRDY using a status read operation. RxRDY is automatically reset when the character is read by the CPU.

$\overline{RxC}$ (Receiver Clock) — The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the frequency of $\overline{RxC}$ is equal to the actual Baud Rate (1x). In Asynchronous Mode, the frequency of $\overline{RxC}$ is a multiple of the actual Baud Rate. A portion of the mode instruction selects the value of the multiplier; it can be 1x, 16x, or 64x the Baud Rate.

For example:
> If Baud Rate equals 300 Baud,
> $\overline{RxC}$ equals 300 Hz (1x)
> $\overline{RxC}$ equals 4800 Hz (16x)
> $\overline{RxC}$ equals 19.2 kHz (64x).
> If Baud Rate equals 2400 Baud,
> $\overline{RxC}$ equals 2400 Hz (1x)
> $\overline{RxC}$ equals 38.4 kHz (16x)
> $\overline{RxC}$ equals 153.6 kHz (64x).

Data is sampled into the 8251 on the rising edge of $\overline{RxC}$.

NOTE: In most communications systems, the 8251 will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

SYNDET (SYNC Detect) — This pin is used in SYNChronous Mode only. It is used as either input or output, programmable through the Control Word. It is reset to "low" upon RESET. When used as an output

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(internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251 has located the SYNC character in the Receive mode. If the 8251 is programmed to use double Sync characters (bi-sync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as an input (external SYNC detect mode), a positive going signal will cause the 8251 to start assembling data characters on the falling edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. The duration of the high signal should be at least equal to the period of $\overline{RxC}$.

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251 is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the 8251 to support the desired communications format. These control words will program the: Baud Rate, Character Length, Number of Stop Bits, Synchronous or Asynchronous Operation, Even/Odd Parity, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251 is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251 is ready to receive a character. This output (TxRDY) is reset automatically when the CPU writes a character into

the 8251. On the other hand, the 8251 receives serial data from the MODEM of I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU that the 8251 has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU read operation.

The 8251 cannot begin transmission until the TxEN (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

Programming the 8251

Prior to starting data transmission or reception, the 8251 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251 and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

This format defines the general operational characteristics of the 8251. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the 8251 by the CPU, SYNC characters or Command instructions may be inserted.

Command Instruction

This format defines a status word that is used to control the actual operation of the 8251.

Both the Mode and Command instructions must conform to a specified sequence for proper device operation. (See Pictorial 5-6.) The Mode Instruction must be inserted immediately following a Reset operation, prior to using the 8251 for data communication.
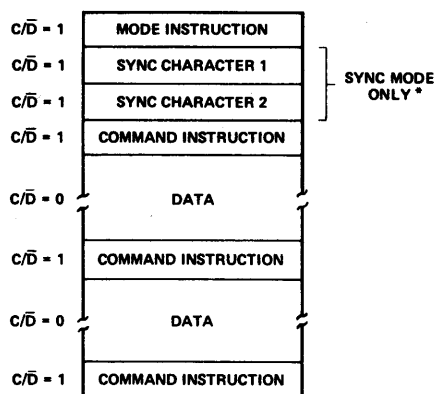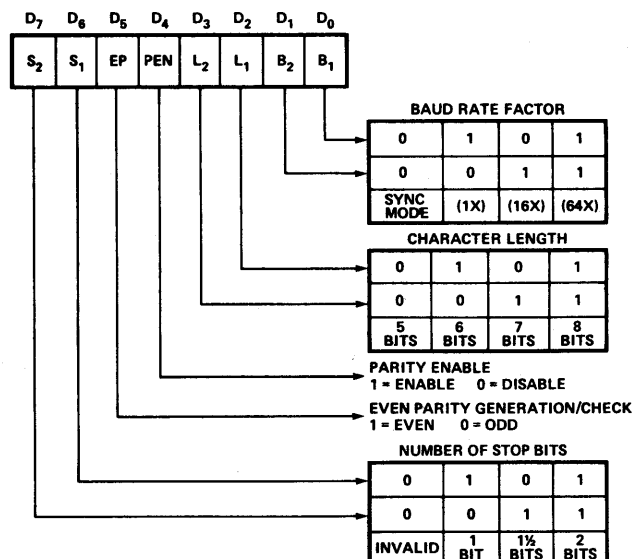

PICTORIAL 5-6

All control words written into the 8251 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251 at any time in the data block during the operation of the 8251. To return to the Mode Instruction format, a bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.

Mode Instruction Definition

The 8251 can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251, the designer can best view the device as two separate components sharing the same package, one Asynchronous, the other Synchronous. The format definition can be changed "on the fly," but for explanation purposes, the two formats will be isolated.
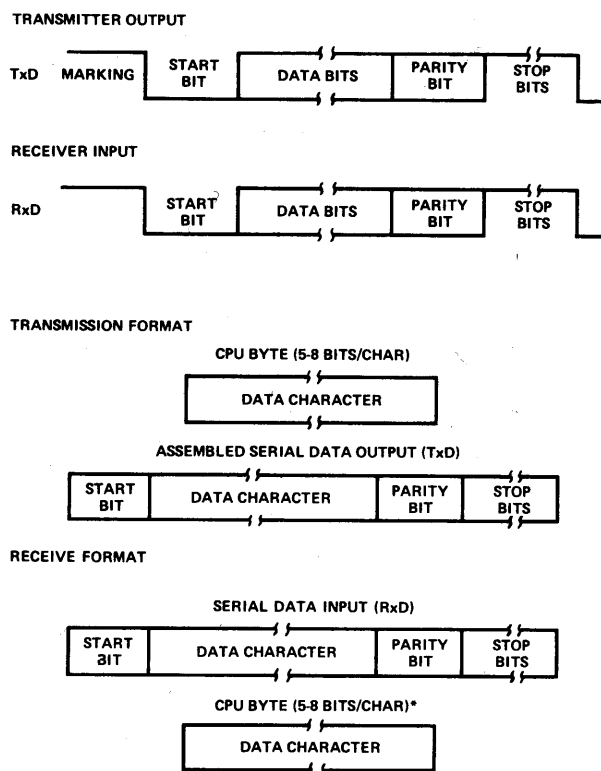
Asynchronous Mode (transmission) — Whenever a data character is sent by the CPU, the 8251 automatically adds a Start bit (low level) and the programmed number of Stop bits to each character. (See Pictorials 5-7 and 5-8). Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of the $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. Break characters can be continuously sent to the TxD if commanded to do so.

PICTORIAL 5-7

When no data characters have loaded into the 8251 the TxD output remains "high" (marking) unless a Break (continuously low) has been programmed.

Asynchronous Mode (Receiver) — The RxD line is normally high. A falling edge on this line triggers the beginning of a Start bit. The validity of this Start bit is checked by again strobing this bit at its nominal center. If a low is detected again, it is a valid Start bit, and the bit counter will start counting. The bit counter locates the center of the data bits, the parity bit (if it exists) and the Stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of the $\overline{RxC}$. If a low level is detected as the Stop bit, the Framing Error flag will be set. The Stop bit signals the

TRANSMITTER OUTPUT

TxD — MARKING — START BIT | DATA BITS | PARITY BIT | STOP BITS

RECEIVER INPUT

RxD — START BIT | DATA BITS | PARITY BIT | STOP BITS

TRANSMISSION FORMAT

CPU BYTE (5-8 BITS/CHAR)

DATA CHARACTER

ASSEMBLED SERIAL DATA OUTPUT (TxD)

START BIT | DATA CHARACTER | PARITY BIT | STOP BITS

RECEIVE FORMAT

SERIAL DATA INPUT (RxD)

START BIT | DATA CHARACTER | PARITY BIT | STOP BITS

CPU BYTE (5-8 BITS/CHAR)*

DATA CHARACTER

*NOTE: IF CHARACTER LENGTH IS DEFINED AS 5, 6, OR 7 BITS, THE UNUSED BITS ARE SET TO "ZERO".

PICTORIAL 5-8

D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0

SCS | ESD | EP | PEN | L_2 | L_1 | 0 | 0

CHARACTER LENGTH

0	1	0	1
0	0	1	1
5 BITS	6 BITS	7 BITS	8 BITS

PARITY ENABLE
(1 = ENABLE)
(0 = DISABLE)

EVEN PARITY GENERATION/CHECK
1 = EVEN
0 = ODD

EXTERNAL SYNC DETECT
1 = SYNDET IS AN INPUT
0 = SYNDET IS AN OUTPUT

SINGLE CHARACTER SYNC
1 = SINGLE SYNC CHARACTER
0 = DOUBLE SYNC CHARACTER

PICTORIAL 5-9

CPU BYTES (5-8 BITS/CHAR)

DATA CHARACTERS

ASSEMBLED SERIAL DATA OUTPUT (TxD)

SYNC CHAR 1 | SYNC CHAR 2 | DATA CHARACTERS

RECEIVE FORMAT

SERIAL DATA INPUT (RxD)

SYNC CHAR 1 | SYNC CHAR 2 | DATA CHARACTERS

CPU BYTES (5-8 BITS/CHAR)

DATA CHARACTERS

PICTORIAL 5-10

end of character. This character is then loaded into the parallel I/O buffer of the 8251. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the Overrun flag is raised (thus the previous character is lost). All of the error flags can be reset by a command instruction. The occurence of any of these errors will not stop the operation of the 8251.

Synchronous Mode (Transmission) — The TxD output is continuously high until the CPU sends its first character to the 8251, which usually is a SYNC character. (See Pictorials 5-9 and 5-10.) When the CTS line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of TxC. Data is shifted out at the same rate as the TxC.
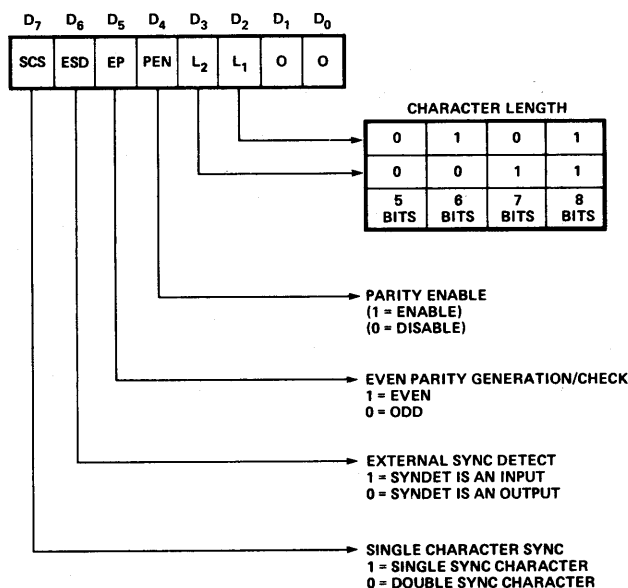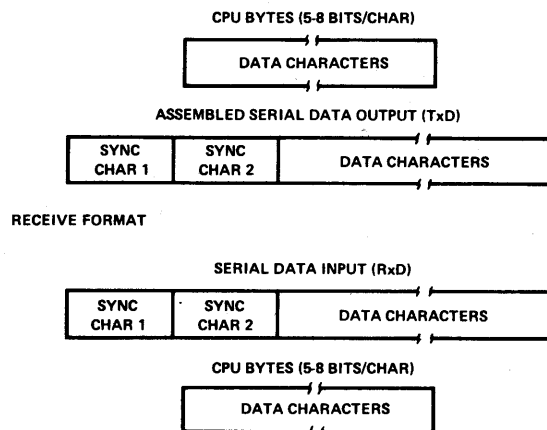
Once transmission has started, the data stream at TxD output must continue at the TxC rate. If the CPU does not provide the 8251 with a character before the 8251 becomes empty, the SYNC characters (or character if in single SYNC word mode) will be automatically inserted in the TxD data stream. In this case, the TxEmpty pin is raised high to signal that the 8251 is empty and SYNC characters are being sent out. The TxEmpty pin is internally reset by the next character being written into the 8251.

Synchronous Mode (Receive) — In this mode, character synchronization can be internally or externally achieved. If the internal SYNC mode has been programmed, the receiver starts in a HUNT mode. Data on the RxD pin is then sampled in on the rising edge of $\overline{RxC}$. The content of the Rx buffer is continuously compared with the first SYNC character until a match occurs. If the 8251 has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a Status Read.
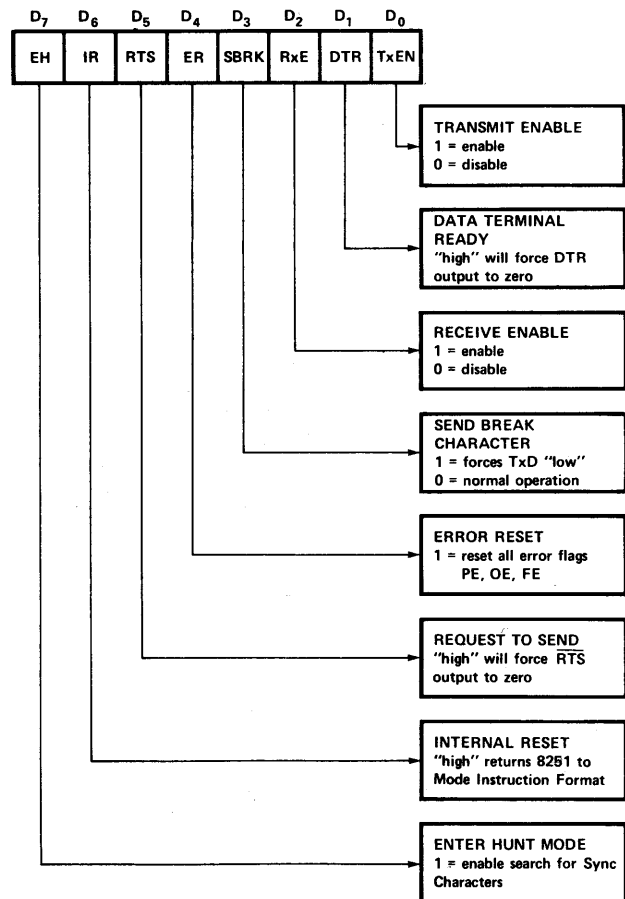
In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin. The high level can be removed after one $\overline{RxC}$ cycle.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode.

The CPU can command the receiver to enter the HUNT mode if synchronization is lost.

COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251 has been programmed by the Mode Insturction and the Sync Characters are loaded (if in Sync Mode), then the device is ready to be used for data communication. (See Pictorial 5-11.) The Command Instruciton controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset, and Modem Controls are provided by the Command Instruction.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
EH	IR	RTS	ER	SBRK	RxE	DTR	TxEN

TRANSMIT ENABLE
1 = enable
0 = disable

DATA TERMINAL READY
"high" will force DTR output to zero

RECEIVE ENABLE
1 = enable
0 = disable

SEND BREAK CHARACTER
1 = forces TxD "low"
0 = normal operation

ERROR RESET
1 = reset all error flags PE, OE, FE

REQUEST TO SEND
"high" will force $\overline{RTS}$ output to zero

INTERNAL RESET
"high" returns 8251 to Mode Instruction Format

ENTER HUNT MODE
1 = enable search for Sync Characters

PICTORIAL 5-11

Once the Mode Instruction has been written into the 8251 and Sync characters inserted, if necessary, then all further "control writes" (C/$\overline{D}$ = 1) will load the Command Instruction. A Reset operation (internal or external) will return the 8251 to the Mode Instruction Format.
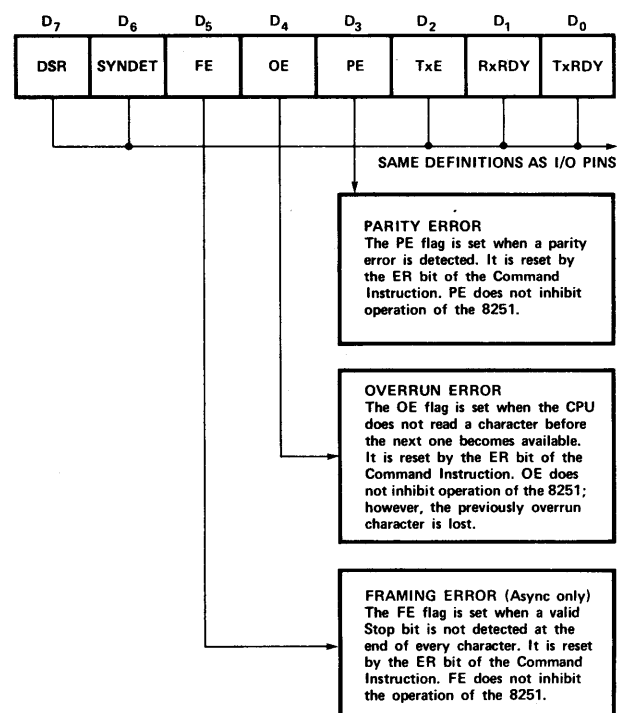
STATUS READ DEFINITION

In data communication systems, it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251 has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. See Pictorial 5-12.

A normal "read" command is issued by the CPU with the C/D̄ input at one to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251 can be used in a completely Polled environment or in an interrupt driven environment.

D7	D6	D5	D4	D3	D2	D1	D0
DSR	SYNDET	FE	OE	PE	TxE	RxRDY	TxRDY

SAME DEFINITIONS AS I/O PINS

PARITY ERROR
The PE flag is set when a parity error is detected. It is reset by the ER bit of the Command Instruction. PE does not inhibit operation of the 8251.

OVERRUN ERROR
The OE flag is set when the CPU does not read a character before the next one becomes available. It is reset by the ER bit of the Command Instruction. OE does not inhibit operation of the 8251; however, the previously overrun character is lost.

FRAMING ERROR (Async only)
The FE flag is set when a valid Stop bit is not detected at the end of every character. It is reset by the ER bit of the Command Instruction. FE does not inhibit the operation of the 8251.

PICTORIAL 5-12