Design of 1-bit full adder using CMOS mirror logic

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Abstract

Adders are one of the main components of majority of circuits and find their application in ALU's, microprocessors, DSP processors. A 1-bit full adder using CMOS mirror logic is designed and implemented in this paper. The implementation will be done in 28nm technology node using Synopsys tools. The reference waveforms [Figure2] will be verified with actual waveforms obtained from simulation.

Keywords— pull-up network, pull-down network, PMOS, CMOS, CMOS inverter,

REFERENCE CIRCUIT DETAILS

A one bit full adder has two circuit blocks, with three inputs and two outputs, one block generates the sum output and the other generates the carry output.

The carry output is generated using the expression

$$Cout = A.B + Cin.(A+B)$$

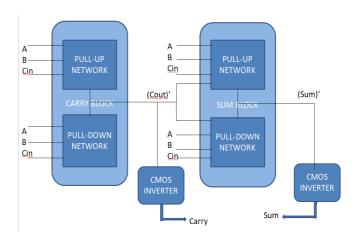
The pull-down network of carry block with three inputs consisting of only NMOS is designed based on CMOS logic and the pull-up network consisting of only PMOS will be exact mirror image of the pull-down network. The output obtained will be in inverted form (Cout)' which will be fed to CMOS inverter to obtain the Cout.

The sum output is generated using the expression

$$Sum = A.B.Cin + (Cout)'.(A+B+Cin)$$

The sum output can be obtained using the inverted Cout obtained from previous carry block which reduces the number of transistors in the circuit. The pull-down network of sum block with four inputs consisting of only NMOS is designed based on CMOS logic with (Cout)' as fourth input and the pull-up network consisting of only PMOS will be exact mirror image of the pull-down network. The output obtained will be in inverted form (Sum)' which will be fed to CMOS inverter to obtain the Sum.

BLOCK DIAGRAM



Reference Circuit

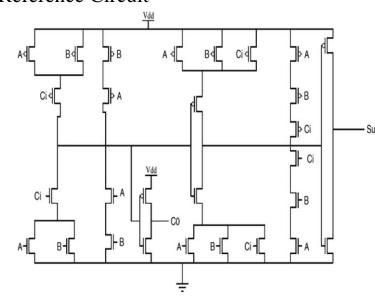


Figure 1: Reference Circuit Diagram [1]

Reference Waveforms

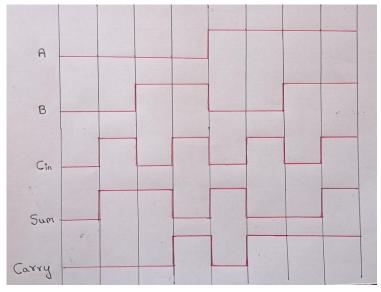


Figure 2: Reference waveform

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