8-Bit Vedic Multiplier

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***Abstract*—Multiplier is an essential functional block of a microprocessor This paper presents the design of a 8-bit Vedic multiplier architecture which implements Urdhva-tiryakbyham sutra of Vedic method of multiplication which reduces hardware as well as the delay compared to other algorithms.**

Keywords—Vedic Multiplier; Urdhva-tiryakbyham; Half adder (HA); Ripple Carry Adder (RCA)

I. DESCRIPTION

Urdhva-tiryakbhyam sutra literally means vertically and cross-wise. The working methodology is described in (Fig. 1).

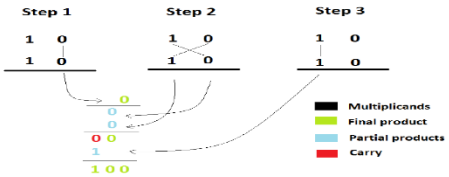


Fig. 1. Working methodology of the sutra

The basic block of the design is Vedic 2x2 multiplier which is implemented using two HA blocks and AND gates (Fig. 2). Four Vedic 2x2 multiplier blocks, one 4-bit RCA and two 6-bit RCA are used to design a Vedic 4x4 multiplier block (Fig. 3). Four Vedic 4x4 multiplier blocks, one 8-bit RCA and two 12-bit RCA are used to design the 8-bit multiplier (Fig. 4). Thus a recursive method is used in the implementation of the design.

II. BLOCK DIAGRAMS

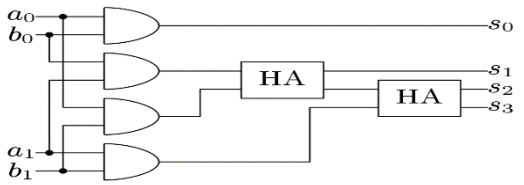


Fig. 2. Vedic 2x2 Multiplier block

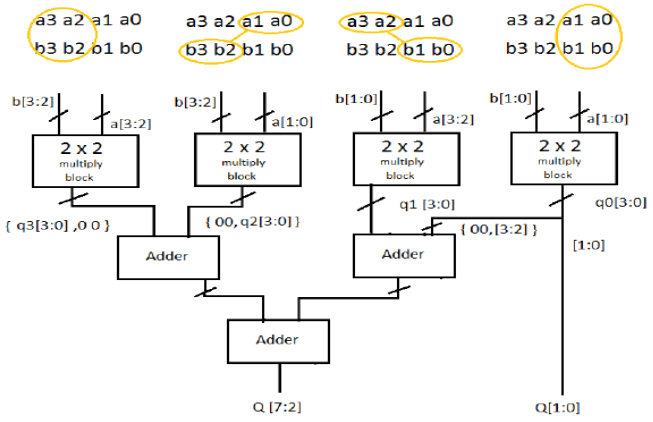


Fig. 3. Vedic 4x4 multiplier block

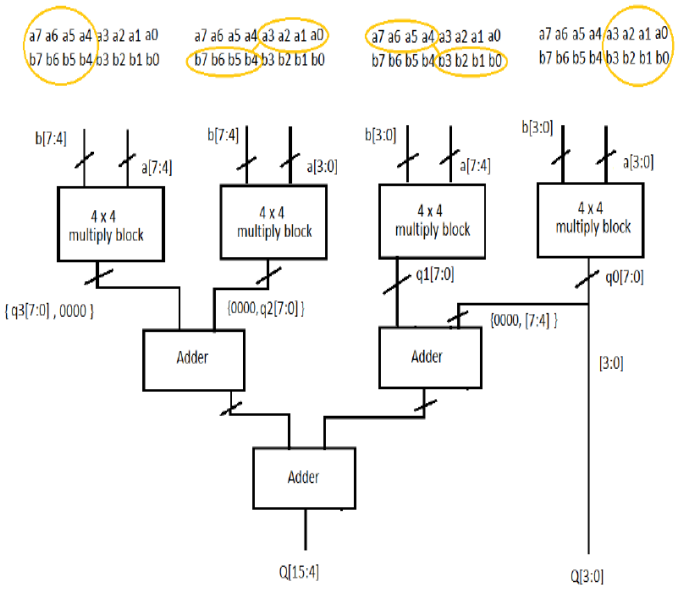
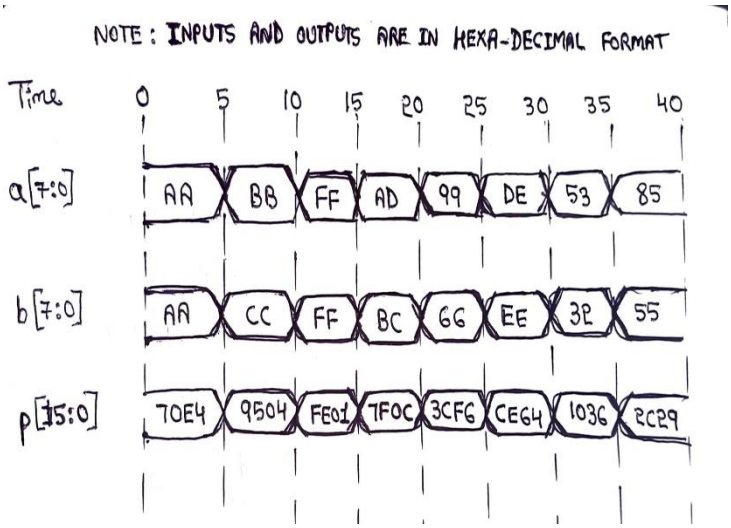


Fig. 4. 8-Bit Vedic Multiplier

III. WAVEFORMS



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[2] https://opencores.org/projects/8bit_vedic_multiplier,Category: Arithmetic core, Language: Verilog, License: LGPL