Project Report

Design of a Two-Stage Operational Transconductance Amplifier (OTA) using g_m/I_d Method

For

Curious Analog IC Design Course

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Abstract

This project report presents the design of a two-stage Operational Transconductance Amplifier (OTA) using the g_m/I_d methodology. The g_m/I_d design approach provides an intuitive and systematic way to size transistors, optimize gain, bandwidth, and power efficiency. The OTA is implemented in 130 nm CMOS technology, targeting low-power and high-performance analog circuit applications. Simulation results are provided to demonstrate the effectiveness of the design methodology.

1 Introduction

Operational Transconductance Amplifiers (OTAs) are key components in analog and mixed-signal circuits, acting as voltage-to-current converters. Their performance significantly affects the efficiency and accuracy of systems such as filters, ADCs, oscillators, and sensor interfaces. With advanced CMOS scaling, achieving high gain, wide bandwidth, low power, and good linearity in OTAs has become increasingly challenging.

The two-stage OTA topology is commonly used to address these requirements. The first stage provides high differential gain, while the second stage serves as a gain or buffering stage to drive large capacitive loads. This structure enables high overall gain while maintaining sufficient phase margin and stability, which are critical for modern analog applications.

Traditional analog design often relies on trial-and-error sizing or simplified calculations, which can be inefficient. The g_m/I_d methodology provides a systematic approach by relating transistor transconductance (g_m) to drain current (I_d), allowing optimal transistor sizing and operation. Using this method, the two-stage OTA is designed in 130 nm CMOS technology, focusing on high gain, low power, and robust performance, with simulations confirming that the design meets the target specifications.

2 Specification

The key specifications of the designed OTA are summarized in Table 1:

Parameters	**Value**
Load Capacitance	4 pF
Open Loop Gain	$\geq$ 60 dB
Phase Margin	$\geq$ 60 Degrees
Unity Gain Frequency	$\geq$ 80 MHz
Power Consumption	$\leq$ 10 mW

Table 1: Specifications of the two-stage OTA

3 Methodology

The g_m/I_d methodology is a modern design technique that relates the transconductance of a MOS transistor (g_m) to its drain current (I_d). This ratio serves as a key figure of merit, allowing designers to choose the optimal operating region—weak, moderate, or strong inversion—based on required performance parameters such as gain, speed, linearity, and power efficiency. By using pre-generated g_m/I_d curves, transistor sizing and biasing can be carried out systematically, making the design process more intuitive and efficient compared to traditional trial-and-error methods.

This methodology provides a structured way to perform transistor-level design, ensuring predictable trade-offs between speed, power, and accuracy. In this project, it is used to determine the sizing of MOS transistors for the two-stage OTA, ensuring that both high gain and power efficiency targets are met.

3.1 Circuit Diagram

The circuit diagram of the designed two-stage OTA is shown in Figure 1. It illustrates the transistor-level implementation of the input differential stage, gain stage, and compensation network.

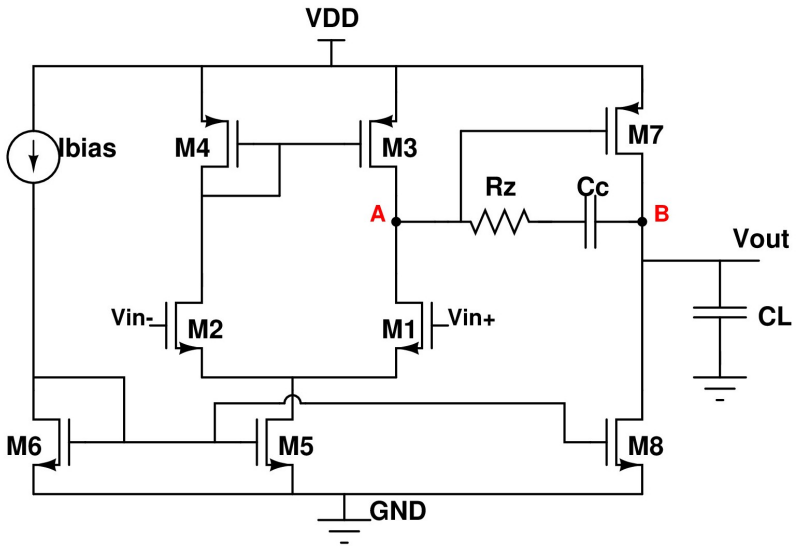


Figure 1: Two-stage OTA circuit diagram

3.2 Overall Voltage Gain

The overall voltage gain ($\boldsymbol{A_v}$) of a two-stage OTA is the product of the gains of the first and second stages:

$$\boldsymbol{A_v = A_{v1} \times A_{v2}}$$

For the first stage (differential amplifier):

$$\boldsymbol{A_{v1} = g_{m1} \cdot (r_{o1} \parallel r_{o3})}$$

For the second stage (common-source amplifier):

$$\boldsymbol{A_{v2} = g_{m7} \cdot (r_{o7} \parallel r_{o8})}$$

Here, $\boldsymbol{g_m}$ represents the transconductance of the MOS transistor, and $\boldsymbol{r_o}$ is the output resistance of the corresponding device. The parallel combination accounts for the effective resistance seen at each output node.

3.3 Miller Compensation

Miller compensation is used in two-stage OTAs to ensure stability by introducing a dominant pole at the output of the first stage. A compensation capacitor ($\boldsymbol{C_c}$) is connected between the output of the first stage and the input of the second stage. This reduces the gain-bandwidth product at higher frequencies and improves phase margin, preventing unwanted oscillations.

The poles before adding Miller capacitor are

$$\boldsymbol{\omega_{p1} = \frac{1}{R_{out1}C_1}} \qquad\qquad \boldsymbol{\omega_{p2} = \frac{1}{R_{out2}C_2}}$$

The Miller compensation capacitance is given by:

$$\boldsymbol{C_c \approx 0.2C_L} \text{ to } \boldsymbol{0.4C_L}$$

3.4 Feed Forward Zero

Adding a *Miller capacitance* results in a feed-forward path that introduces a zero (ω_Z) into the system.

At the feed-forward zero, $V_{out} = 0 \Rightarrow i_{out} = 0$, then applying KCL at V_{out} we get,

$$\boldsymbol{V_{o1}(s_z C_C) + g_{m7} V_{o1} = 0}$$

$$\boldsymbol{s_z = -\frac{g_{m7}}{C_C}}$$

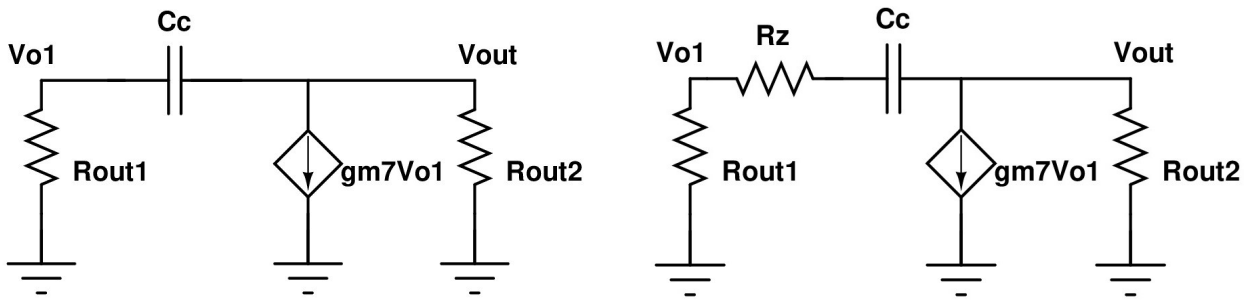
A series resistance R_Z is introduced to cancel this zero. Its value is calculated as follows:

$$\boldsymbol{\frac{V_{o1}}{R_Z + \frac{1}{sZC_C}} = g_{m7} V_{o1}}$$

$$\boldsymbol{g_{m7} R_Z + \frac{g_{m7}}{s_z C_C} = 1 \Rightarrow \frac{g_{m7}}{s_z C_C} = 1 - g_{m7} R_Z}$$

$$\boldsymbol{s_z = \frac{1}{C_C \left(\frac{1}{g_{m7}} - R_Z\right)}}$$

There are two possible approaches for selecting the value of R_Z:



(a) (b)

Figure 2: (a) Small signal model of the Gm gain stage with capacitive feedback (b) Small signal model of second stage with capacitance and Nulling resistor Rz

1. **Zero at Infinity:** To push the zero to infinity, effectively eliminating its impact:

$$\boldsymbol{s_z = \infty \Rightarrow R_Z = \frac{1}{g_{m7}}}$$

2. **Zero at Second Pole:** To place the zero at the second pole for pole-zero cancellation, the value of R_Z is chosen such that:

$$\boldsymbol{s_z = s_{p2} = -\frac{g_{m7}}{C_L}}$$

From the above condition,

$$\boldsymbol{C_L = C_C(R_Z g_{m7} - 1)}$$

$$\boldsymbol{C_L + C_C = C_C(R_Z g_{m7})}$$

$$\boldsymbol{R_Z = \frac{1}{g_{m7}} \cdot \frac{C_L + C_C}{C_C}}$$

By cancelling the second pole using the feed-forward zero, the phase margin of the system improves.

4 Design Procedure

The transconductance of the first stage is calculated as:

$$\boldsymbol{g_{m1} = 2\pi \times \omega_u \times C_c}$$

In typical OTA design, the ratio $\boldsymbol{\omega_{p2}/\omega_u}$ is often chosen to be in the range of **2 *to* 3**. This is a common design choice for achieving a good balance between bandwidth and phase margin.

$$\boldsymbol{\frac{\omega_{p2}}{\omega_u} = 2 = \frac{g_{m7}}{C_L} \times \frac{C_c}{g_{m1,2}}}$$

Rearranging gives:

$$\frac{g_{m7}}{g_{m1,2}} = \frac{2\,C_L}{C_c}$$

$$g_{m7} = \frac{2\,C_L}{C_c} \times g_{m1,2}$$

Since $g_{m1,2} \propto 2\,I_{D1,2}$ and $g_{m7} \propto 2\,I_{D7}$, we get:

$$\frac{I_{D7}}{I_{D1,2}} = \frac{2\,C_L}{C_c}$$

Therefore:

$$\frac{I_{D7}}{I_{D5}} = \frac{C_L}{C_c}$$

4.1 First Stage Design

For the designed OTA, the load capacitance is $\mathbf{C_L = 4\,pF}$. Choosing a factor of 0.22:

$$\mathbf{C_c = 0.22 \times C_L = 0.22 \times 4\,pF = 0.88\,pF \approx 1\,pF}$$

The transconductance of the first stage is given by:

$$\mathbf{g_{m1} = 2\pi \times UGB \times C_c}$$

Let the unity-gain bandwidth (UGB) be taken as $\mathbf{UGB = 100\,MHz}$ and using $\mathbf{C_c = 1\,pF}$:

$$\mathbf{g_{m1} = 2\pi \times 100 \times 10^6 \times 1 \times 10^{-12}\,S \approx 630\,\mu S}$$

Now, let us consider $\mathbf{V_{ov} = 150\,mV}$, which is sufficient to keep the MOS in strong inversion. From the g_m/I_D vs V_{ov} curve, the corresponding value is:

$$\mathbf{\frac{g_m}{I_D} = 12} \quad \text{for} \quad \mathbf{V_{ov} = 150\,mV}$$

Therefore,

$$\mathbf{I_{D1} = \frac{g_{m1}}{(g_m/I_D)} = \frac{630\,\mu S}{12} \approx 52\,\mu A} \text{ (nearly } \mathbf{50\,\mu A}\text{)}$$

We require a total gain of $\mathbf{60\,dB}$, distributed as $\mathbf{40\,dB}$ for the first stage and $\mathbf{30\,dB}$ for the second stage. Using the g_m/g_{ds} vs g_m/I_D curve, the channel length is chosen such that:

$$\mathbf{\frac{g_m}{g_{ds}} \geq 100}$$

Hence, the length is selected as:

$$\mathbf{L_{1,2} = 0.75\,\mu m}$$

From the g_m/I_D vs I_D/W curve, for $g_m/I_D = 12$, $V_{ov} = 150\,mV$, and $L_{1,2} = 0.75\,\mu m$, we get:

$$\mathbf{\frac{I_D}{W} = 4.6\,\mu A/\mu m}$$

Therefore,

$$\mathbf{W = \frac{I_D}{(I_D/W)} = \frac{50}{4.6} \approx 11\,\mu m}$$

Thus,

$$\mathbf{W_{1,2} = 11\,\mu m}$$

For the PMOS load, the channel length remains the same ($\mathbf{L_{3,4} = 0.75\,\mu m}$), but the width is taken as 3 times that of the NMOS, hence:

$$\mathbf{W_{3,4} = 3 \times W_{1,2} = 3 \times 11 = 33\,\mu m}$$

4.2 Second Stage Design

We have calculated the transconductance of the second stage as:

$$\mathbf{g_{m7}} = \frac{2C_L}{C_c} \times g_{m1} = \frac{2 \times 4\,pF}{1\,pF} \times 630\,\mu S \approx 5\,mS$$

The drain current of the second stage is:

$$\mathbf{I_{D7}} = \frac{2C_L}{C_c} \times I_{D1} = \frac{2 \times 4\,pF}{1\,pF} \times 50\,\mu A = 400\,\mu A$$

For the second stage, we require a gain of **30 dB**, which implies:

$$\mathbf{\frac{g_m}{g_{ds}} \geq 30}$$

Using the g_m/g_{ds} vs V_{ov} plot, for $\mathbf{V_{ov} = 150\,mV}$, the channel length is chosen as:

$$\mathbf{L_7 = 0.6\,\mu m}$$

From the I_D/W vs g_m/I_D plot, for $g_m/I_D = 12$, we get:

$$\mathbf{\frac{I_D}{W} = 6 \implies W_7 = \frac{I_{D7}}{6} = \frac{400}{6}\,\mu m \approx 66\,\mu m}$$

Since it is a PMOS load, we multiply by 3 to account for mobility differences:

$$\mathbf{W_7 = 3 \times 66\,\mu m \approx 200\,\mu m}$$

4.3 Current Mirror Design

For current mirror biasing, let us consider an overdrive voltage of $\boldsymbol{V_{ov} = 200\,mV}$ with a corresponding value of $\boldsymbol{g_m/I_D = 10}$. The channel length is chosen as $\boldsymbol{L = 1\,\mu m}$ to mitigate channel length modulation. The reference bias current is taken as $\boldsymbol{I_{D6} = 20\,\mu A}$.

From the I_D/W vs g_m/I_D plot, for $g_m/I_D = 10$, we obtain:

$$\frac{I_D}{W} = 5 \implies W_6 = \frac{I_{D6}}{5} = \frac{20}{5} \approx 4\,\mu m$$

To bias the first stage, we require $\boldsymbol{I_{D5} = 100\,\mu A}$. Using the current mirror relation:

$$\frac{I_{D5}}{I_{D6}} = \frac{W_5}{W_6} \implies W_5 = \frac{I_{D5}}{I_{D6}} \times W_6 = \frac{100}{20} \times 4 = 20\,\mu m$$

Similarly, to bias the second stage, we require $\boldsymbol{I_{D8} = 400\,\mu A}$. Therefore:

$$\frac{I_{D8}}{I_{D6}} = \frac{W_8}{W_6} \implies W_8 = \frac{I_{D8}}{I_{D6}} \times W_6 = \frac{400}{20} \times 4 = 80\,\mu m$$

4.4 Nulling Resistor

To improve the phase margin and compensate for the right-half-plane zero caused by the output stage, a nulling resistor $\boldsymbol{R_z}$ is added in series with the Miller compensation capacitor $\boldsymbol{C_c}$.

The value of the nulling resistor can be calculated as:

$$\boldsymbol{R_z = \frac{1}{g_{m7}} \times \frac{C_L + C_c}{C_c}}$$

where $\boldsymbol{g_{m7}}$ is the transconductance of the second stage transistor, $\boldsymbol{C_L}$ is the load capacitance, and $\boldsymbol{C_c}$ is the compensation capacitor.

Using the calculated values $\boldsymbol{g_{m7} = 5\,mS}$, $\boldsymbol{C_L = 4\,pF}$, and $\boldsymbol{C_c = 1\,pF}$:

$$\boldsymbol{R_z = \frac{1}{5 \times 10^{-3}} \times \frac{4+1}{1} = 200 \times 5 = 1000\,\Omega}$$

The nulling resistor helps to move the zero to a higher frequency, improving the phase margin and overall stability of the OTA.

5 Results

5.1 DC Simulation

The DC analysis was carried out to validate the biasing conditions of the transistors and ensure correct circuit operation. Table 2 highlights a comparison between theoretical estimates and simulated values for important parameters such as drain currents (I_D), transconductance (g_m), and open-loop gain (A_V). The simulated bias currents show good agreement with the expected values, with slight differences attributed to second-order effects like mobility reduction and channel length modulation. The obtained transconductance values remain very close to the design targets, confirming proper sizing of devices. The simulated DC gain is 65 dB, slightly higher than the target of 60 dB, which can be explained by increased output resistance in the devices. Overall, the OTA achieves reliable operation with minimal deviation from design specifications, while consuming only 0.9 mW of power, demonstrating an efficient low-power design.The DC simulation results are summarized in Table 2, comparing theoretical and obtained values.

Table 2: DC Simulation Results

Parameter	Theoretical Value	Obtained Value
Gain (dB)	60	63
$g_{m1,2}$ (μS)	630	576
g_{m7} (mS)	5	3.7
$I_{D1,2}$ (μA)	50	48.18
I_{D7} (μA)	400	436

5.2 AC Simulation

From the AC simulation, the OTA exhibits an open-loop gain of 63 dB, along with a phase margin of 59°, ensuring stable operation. The unity-gain bandwidth (UGB) is observed to be 103 MHz, which closely aligns with the design target, confirming that the OTA meets both speed and stability requirements.

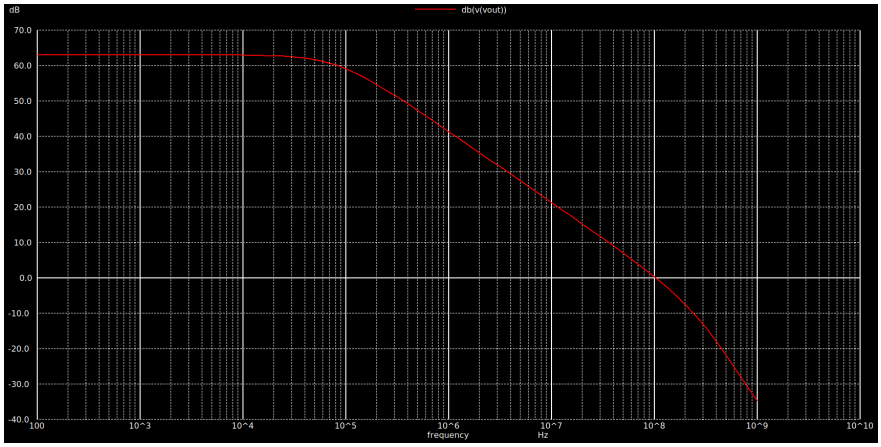


Figure 3: AC Simulation: Open-loop gain response of the OTA.

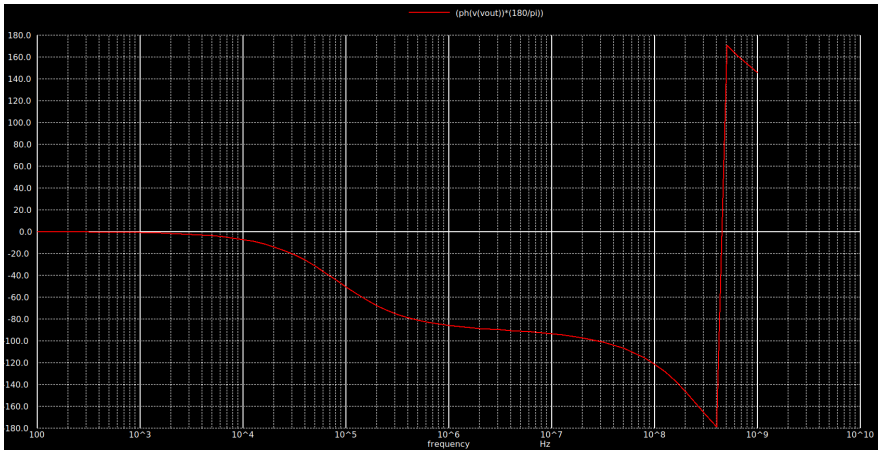


Figure 4: AC Simulation: Phase response of the OTA.

6 Conclusion

The design of a two-stage OTA using the g_m/I_d methodology has been successfully carried out and validated through simulation. The step-by-step procedure, including device sizing, bias current allocation, and compensation techniques, ensured that the target specifications of gain, bandwidth, and phase margin were achieved.

Simulation results confirmed that the OTA achieves a DC gain of over 60 dB, a unity-gain bandwidth above 100 MHz, and a stable phase margin close to 60°, making it suitable for high-speed and low-power analog applications. The power consumption of only 0.9 mW demonstrates the efficiency of the design while maintaining robust performance.

Overall, the project highlights the effectiveness of the g_m/I_d methodology as a systematic and intuitive approach for modern analog circuit design, providing both accuracy and design flexibility. This methodology can be extended to other analog building blocks, offering a reliable path toward low-power, high-performance circuit solutions in advanced CMOS technologies.

Acknowledgment

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