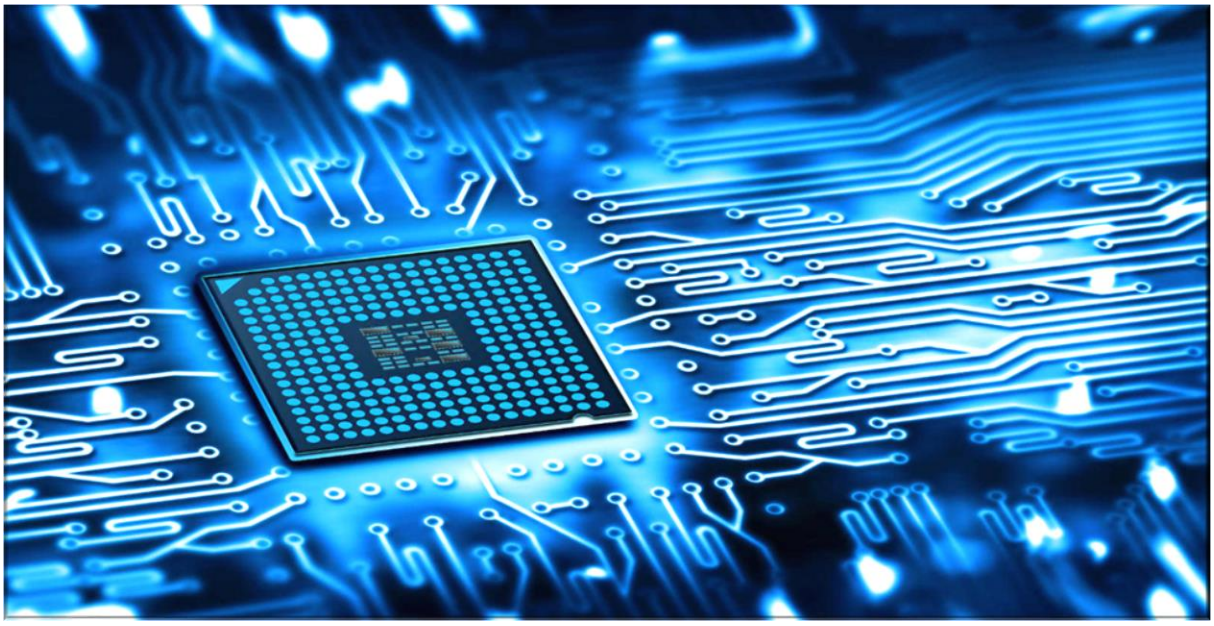
DIGITAL VLSI DESIGN

Project Report

Full Adder Schematic, Implementation of Mirror and Conventional Circuit



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Problem statement

Q) Design a full adder using mirror circuit concept. Use all MOS devices with W/L ratio of 400n/180n

1) **Using Convention CMOS logic.**
2) **Mirror Circuit Concept.**
3) **Calculate the worst propagation delay for 1) and 2) and comment.**
4) **Draw the layout for the Mirror circuit using Minimum area, the pull up and the pull down layout should be symmetric.**

Introduction

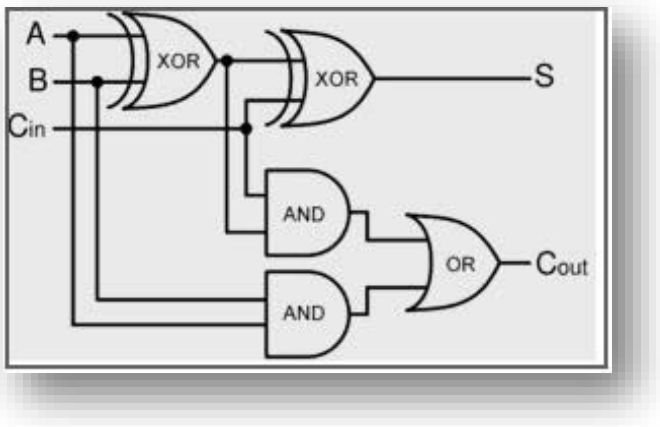
Full adder is a combinational logic circuit which is used for the purpose of adding three inputs and produces two outputs. Full adders are implemented with logic gates in hardware. It adds three one-bit binary numbers, two operands and a carry bit, and it outputs two numbers, a sum and a carry bit.

Truth Table

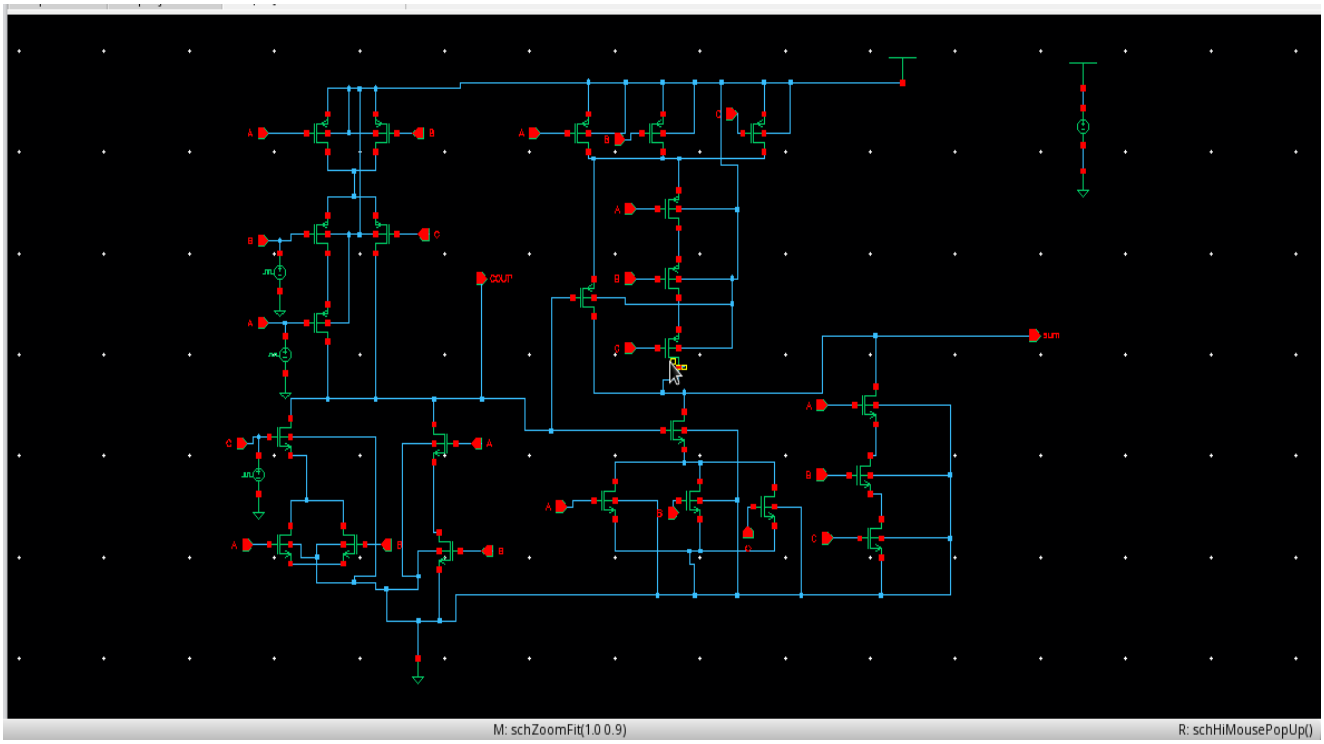
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

SUM = A’B’Cin + A’BCin’+AB’Cin’+ABCin CARRY = AB+ACin+BCin

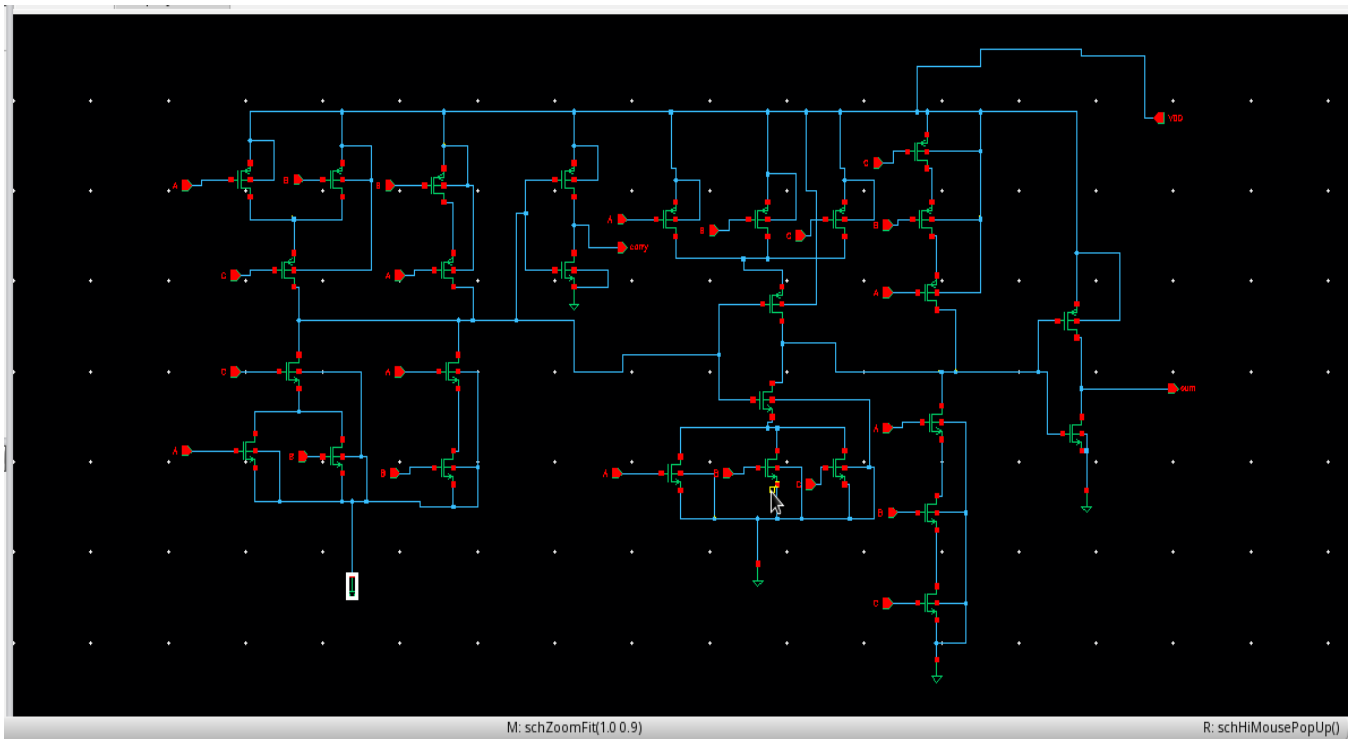
Logic Gate Diagram



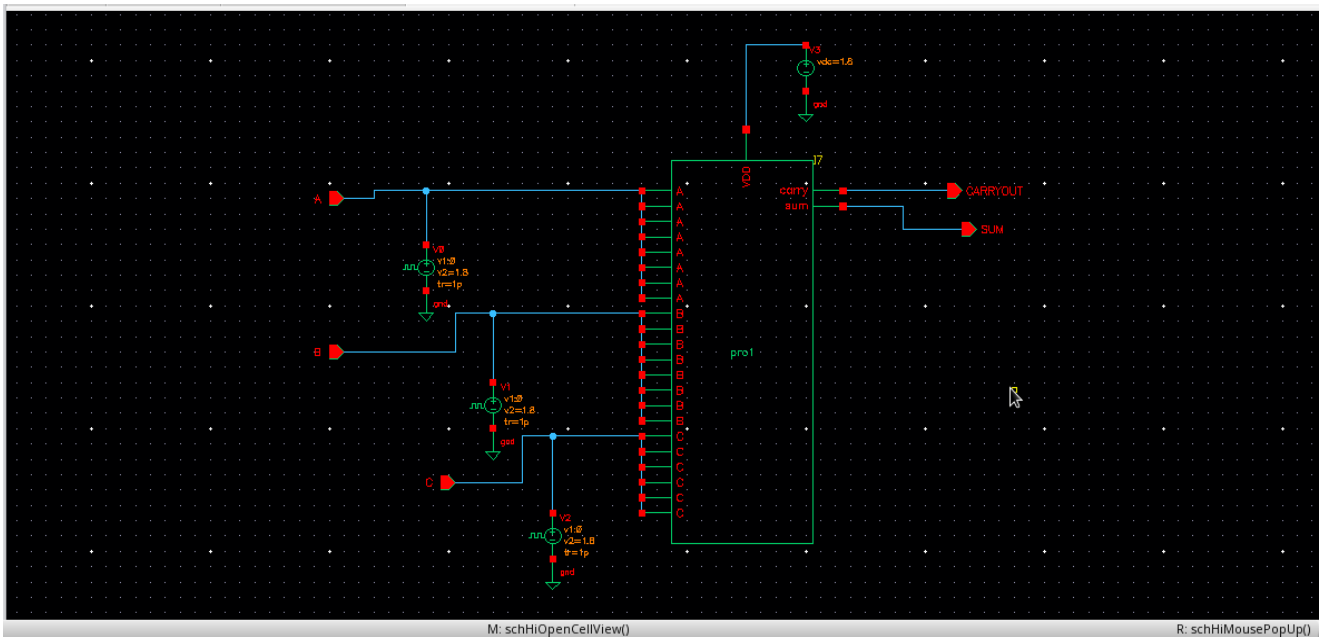
Conventional Circuit Schematic



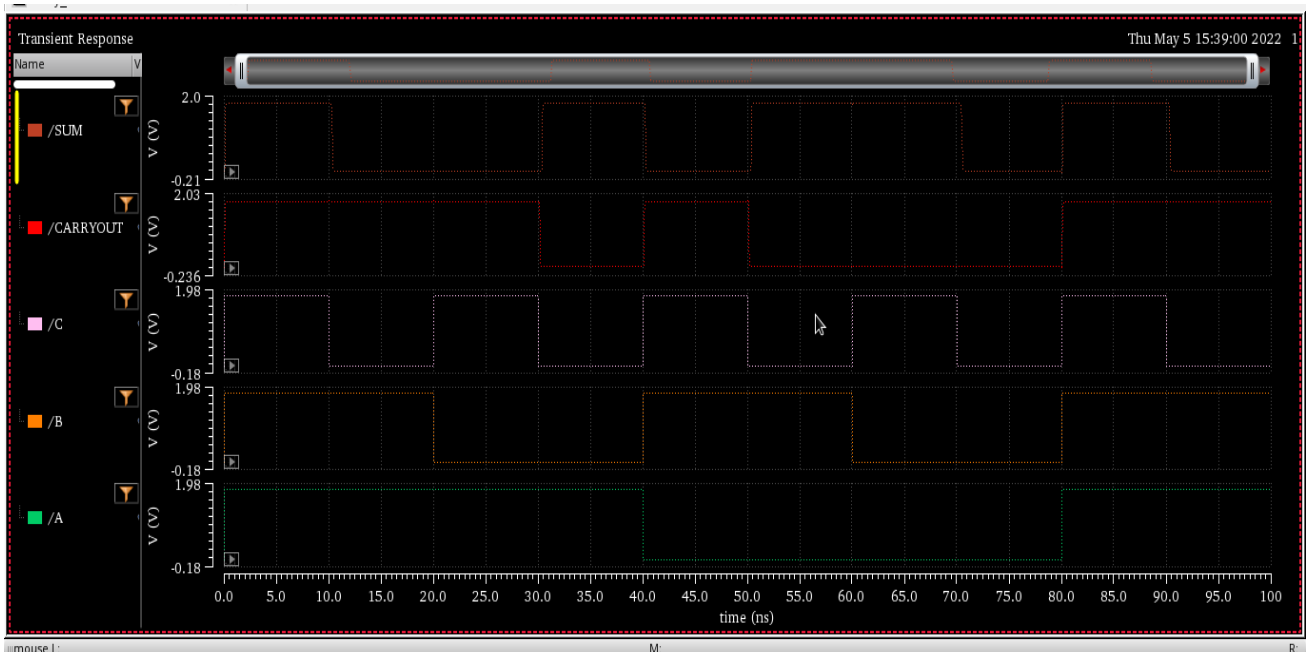
Mirror Circuit Schematic



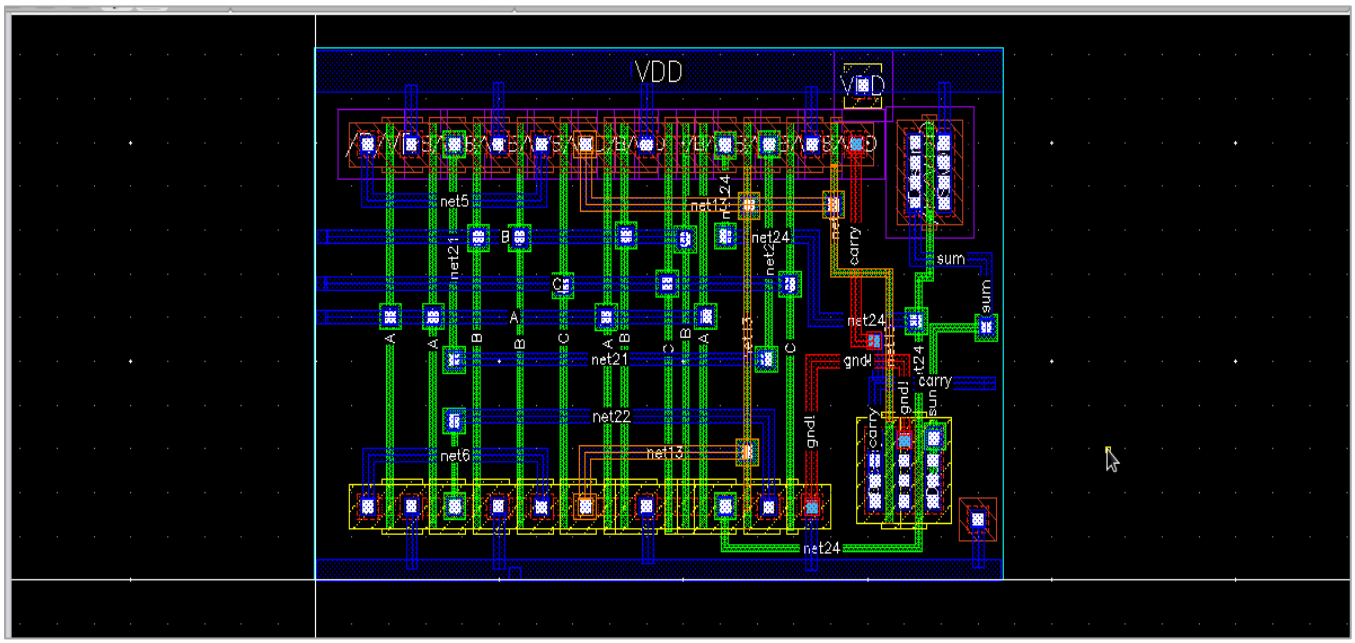
Mirror Circuit Symbol



Output



Layout of Mirror Circuit



Conclusion

The mirror circuit and conventional circuit of Full Adder uses total of 28 transistors.

The propagation delay in

a) Mirror Circuit is

b) Conventional circuit is