Lambton College In Toronto

Course Number	Ese 2005
Section Number	**EMBT TERM 2**
Course Title	Embedded Systems Architecture 1
Semester/Year	EMBT Term2/2019

Instructor	**Mohsen Salahi**

Lab No.	**3**

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Lab No.3

Program:

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.std_logic_arith.all;
4   use ieee.std_logic_unsigned.all;
5   entity g is
6   port(
7   clk:in std_logic;
8   p:in std_logic;
9   reset:in std_logic;
10  R:out std_logic);
11  end g;
12
13  architecture behav of g is
14  type state_type is (state0,state1,state2,state3,state4,state5,state6);
15  signal current_state: state_type;
16
17  begin
18  process(clk,reset)
19  begin
20  if (reset='1') then
21  current_state<=state0;
22  elsif(clk'event and clk='1')then
23  case current_state is
24  when state0=>
25  if p='1' then
26  current_state<=state1;
27  else
```

```
25  if p='1' then
26  current_state<=state1;
27  else
28  current_state<=state2;
29  end if;
30
31  when state1=>
32  if p='1' then
33  current_state<=state2;
34  else
35  current_state<=state1;
36  end if;
37
38  when state2=>
39  if p='1' then
40  current_state<=state3;
41  else
42  current_state<=state2;
43  end if;
44
45  when state3=>
46  if p='1' then
47  current_state<=state4;
48  end if;
49
50  when state4=>
51  if p='1' then
```

```
42      current_state<=state2;
43      end if;
44
45      when state3=>
46      if p='1' then
47      current_state<=state4;
48      end if;
49
50      when state4=>
51      if p='1' then
52      current_state<=state5;
53      else
54      current_state<=state6;
55      end if;
56
57      when others=>
58      current_state<=state0;
59
60      end case;
61      end if;
62      end process;
63
64      R<='1' when current_state = state6 else '0';
65
66      end behav;
67
68
```

TB:-

```
 1  library ieee;
 2  use ieee.std_logic_1164.all;
 3  use ieee.std_logic_arith.all;
 4  use ieee.std_logic_unsigned.all;
 5  entity test is
 6  end test;
 7  architecture behavioral of test is
 8  component g
 9  port (
10  clk:in std_logic;
11  p: in std_logic;
12  reset:in std_logic;
13  R:out std_logic
14  );
15  end component;
16
17  signal clk:std_logic:='0';
18  signal p:std_logic:='0';
19  signal reset:std_logic:='0';
20
21  signal R :std_logic;
22
23  constant clk_period:time:= 10 ns;
24  begin
25  uut: g port map (
26  clk=>clk,
27  p=>p,
```

```
25  uut: g port map (
26  clk=>clk,
27  p=>p,
28  reset=>reset,
29  R=>R
30  );
31  clk_process: process
32  begin
33  clk<='0';
34  wait for clk_period/2;
35  clk<='1';
36  wait for clk_period/2;
37  end process;
38
39  stim_proc: process
40  begin
41  wait for 100 ns;
42  wait for clk_period *10;
43  wait;
44  end process;
45
46  p_process :process
47  begin
48  p<='1';
49  wait for 100 ns;
50  p<='1';
51  wait for 100 ns;
```

```
31  clk_process: process
32  begin
33  clk<='0';
34  wait for clk_period/2;
35  clk<='1';
36  wait for clk_period/2;
37  end process;
38
39  stim_proc: process
40  begin
41  wait for 100 ns;
42  wait for clk_period *10;
43  wait;
44  end process;
45
46  p_process :process
47  begin
48  p<='1';
49  wait for 100 ns;
50  p<='1';
51  wait for 100 ns;
52  p<='0';
53  wait for 100 ns;
54  end process;
55  end behavioral;
56
57
```

OUTPUT:.