Distributed DMA Support for PCI Systems

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Revision 6.0

Scope of this Revision

This is the first public release of the Distributed DMA Support for PCI Systems specification.

Revision History

Revision	Date	Comments
6.0	9/1/95	First public release

Table of Contents

1.0 Scope

This document describes a new DMA approach for a PC system that does not have an ISA bus as the main system bus, and with a system requirement that two or more devices on this non-ISA bus support legacy DMA. This specification describes an approach which distributes independent, standard programming model Bus Master channels among the devices and, for clarity purposes only, describes a method to make these independent channels appear to be the legacy DMA channels of the PC.

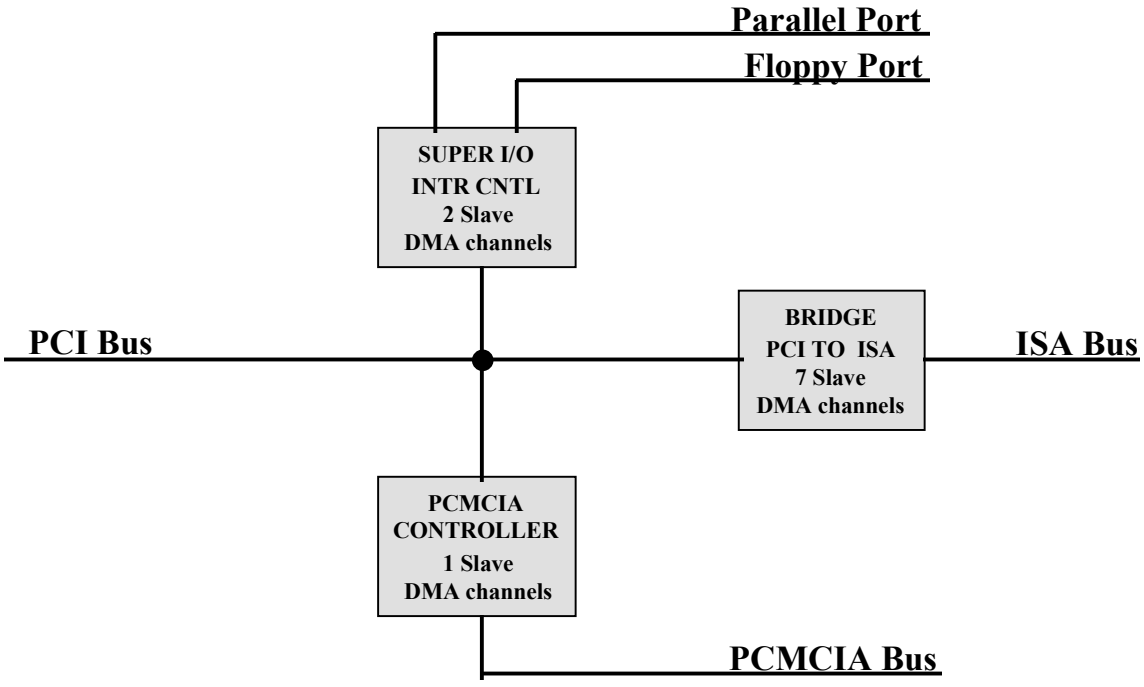
This specification describes a programming model for a Bus Master that is bus independent and implementation independent. By having a standard programming model for a Bus Master, system implementers can tie them together using whatever means they have available to them.

This specification is not an implementation document. It does describe a possible implementation that uses the PCI bus as the main system bus and uses some of the features of this bus; this possible implementation is here for clarity purposes only. This specification does not endorse this method or suggest that it is the only method.

Companies involved in the creation of this spec are:

Cirrus Logic/PicoPower	Standard Microsystems Corporation (SMC)
Compaq Computer Corporation	Texas Instruments
National Semiconductor	VLSI Technology
OPTi	

2.0 Example Block Diagram



3.0 Specification

Each device in the system that has a legacy DMA programming model requirement, must have at least one compatible programming model Bus Master, which will be called a DMA Slave channel. This has the effect of breaking the legacy 8237 DMA controllers into separate channels, existing in different devices. The method defined here allows this separation in the hardware architecture, and yet to the OS and application base there are still two 8237-compatible DMA controllers.

3.1 DMA Slave channel

Each DMA Slave channel has a block of 16, 8 bit registers, defined below. This block is locatable anywhere in the legacy 64k I/O space, by programming the DMA Slave Configuration Register, defined in section 3.6.2. As stated earlier, all DMA Slave channels must have an identical programming model. The DMA Master, not described yet, will be programmed with the base address of each DMA Slave by having a matching base address register for each channel. This is described in section 3.6.1.

Slave address	R/W	Register Name
base + 0h	W	Base Address 0-7
base + 0h	R	Current Address 0-7
base + 1h	W	Base Address 8-15
base + 1h	R	Current Address 8-15
base + 2h	W	Base Address 16-23
base + 2h	R	Current Address 16-23
base + 3h	W	Base Address 24-31
base + 3h	R	Current Address 24-31
base + 4h	W	Base Word Count 0-7
base + 4h	R	Current Word Count 0-7
base + 5h	W	Base Word Count 8-15
base + 5h	R	Current Word Count 8-15
base + 6h	W	Base Word Count 16-23
base + 6h	R	Current Word Count 16-23
base + 7h	N/A	Reserved
base + 8h	W	Command
base + 8h	R	Status
base + 9h	W	Request
base + Ah	N/A	Reserved
base + Bh	W	Mode
base + Ch	W	Reserved
base + Dh	W	Master Clear
base + Eh	N/A	Reserved
base + Fh	R/W	Multi-Channel Mask

Programming Model for Single DMA Slave Channel

Notes:
1. All Reserved addresses must be decoded by the DMA Slave Channel for both write and read access.
2. Read access to a Reserved address must return all zeros.
3. Read access to a write only address is undefined.

3.2 DMA Master

This section describes the concept of the DMA Master. It is the function of the DMA Master to translate I/O cycles to/from the legacy DMA controllers into I/O cycles to/from the DMA Slave channels. To aid in the understanding of this concept, a method that performs this translation which assumes that the PCI bus is the main system bus is described in this section.

NOTE: When implementing this specification, there must always be at least one device in the system that supports the DMA Master function. It must translate all the PCI I/O reads and writes to the legacy DMA I/O addresses into DMA Slave I/O reads and writes. The control of these reads/writes is described next. The DMA Master is required to handle accesses to unassigned legacy DMA channels.

NOTE: If the DMA Master is not in the CPU bridge, all legacy DMA read/write accesses are handled in a special way by the DMA Master which is described below.

1. When the CPU bridge attempts to read/write a legacy DMA register, a PCI I/O cycle will be initiated on the PCI bus with a legacy DMA address. The device designated as the DMA Master will take control this cycle by driving DEVSEL# active, driving its PCI REQ pin active, and issuing a PCI retry to terminate this cycle.

2. The CPU bridge that issued the PCI legacy I/O cycle must drive its PCI REQ pin inactive, which is in accordance to the PCI spec. The period of REQ inactive, beyond what is specified in the PCI spec, is left up to the designer. However, if the DMA Master and the system arbiter exist in the same device or sideband signals are used between the DMA Master and the system arbiter, then a special hardware handler can be designed to make the remainder of this procedure function more smoothly.

3. When granted the PCI bus, the DMA Master will run up to four PCI I/O byte read/writes. The purpose of these read/writes is to return/send the individual channel read/write information. DMA Slave devices must only respond to the slave address assigned to them and not any legacy DMA address.

4. At the end of the last read/write the DMA Master will set an internal flag indicating completion and will drive its REQ line inactive and wait for the retried PCI I/O read/write from the CPU bridge.

5. The PCI I/O read/write will be retried. If it was a read, the DMA Master will return the data. If it was a write, the DMA Master will simply terminate the cycle. Then the DMA Master will reset the internal flag.

NOTE: Channel 4 in a legacy PC is used to connect the two DMA controllers together as a system. It is therefore programmed in cascade mode during POST and programmed again. Since the channels are separated into the different system devices in a PCI bus based system, support for Channel 4 is actually not required. However for compatibility reasons the device designated as the DMA Master device via the PCI Special DMA Configuration Register must support register compatibility of channel 4.

3.3 DMA Control Registers

The DMA Master must support the function of the registers defined in this section and the next two, 3.4 & 3.5. Since there are two physical DMA controllers in a legacy PC system, one for byte transfers and one for word transfers, there are two registers for each register defined. The byte transfer channels are channels 0-3 and the word transfer channels are channels 4-7. Channel 4 is used for cascading the two DMA controllers together in an ISA system, so it is not a usable channel.

3.3.1 Command Register

I/O address	Byte Device	Legacy Address	0008h
		Slave Address	Base + 8h
	Word Device	Legacy Address	00D0h
		Slave Address	Base + 8h
Size			8 bits
Type			Write only
Power up			00000000b

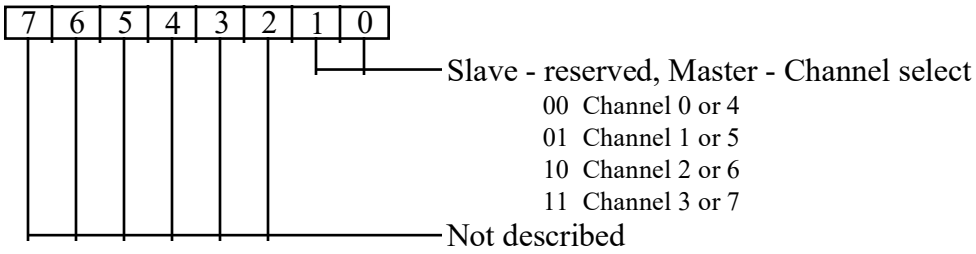
The DMA Master device will handle a write to this legacy address in the special way described at the beginning of section 3.2. Four I/O writes are done if the write is to the Byte legacy DMA device and three I/O writes are done if the write is to the Word legacy DMA device.

For the DMA Slave, the function of this register is the same as for legacy DMA, which also means that Memory to Memory functionality is not required to be supported because it is not supported in a legacy PC. Any programming references to this mode of operation are not required to be functionally supported; however, register compatibility is.

The register contents and functionality are not described here. There are several manufacturer's data books that fully describe the functionality of this register.

3.3.2 Mode Register

I/O address	Byte Device	Legacy Address	000Bh
		Slave Address	Base + Bh
	Word Device	Legacy Address	00D6h
		Slave Address	Base + Bh
Size			8 bits
Type			Write only
Power up			00000000b



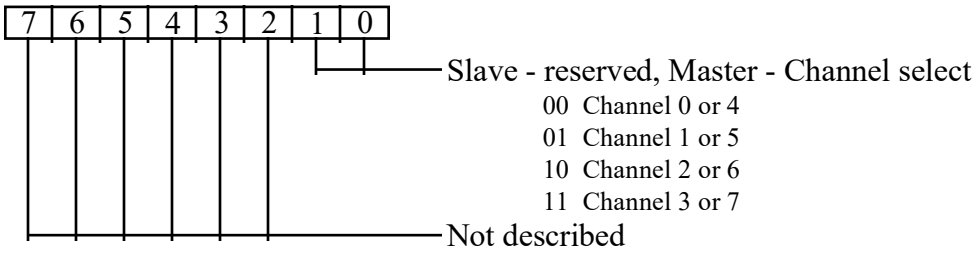
Data bits 0 & 1 of this legacy DMA address indicate which legacy channel to apply the other 6 bits. The DMA Master uses these bits to determine which DMA Slave channel will receive this data. The DMA Master device will handle writes to this legacy address in the special way described at the beginning of section 3.2.

For the DMA Slave, data bits 0 & 1 are considered reserved and will be written **undefined** by the DMA Master. The functionality of the remainder of this register is identical to the legacy DMA controller when applicable.

The remainder of the register contents and functionality are not described here. There are numerous manufacturer's data books that describe the functionality of this register.

3.3.3 Request Register

I/O address	Byte Device	Legacy Address	0009h
		Slave Address	Base + 9h
	Word Device	Legacy Address	00D2h
		Slave Address	Base + 9h
Size			8 bits
Type			Write only
Power up			00000000b



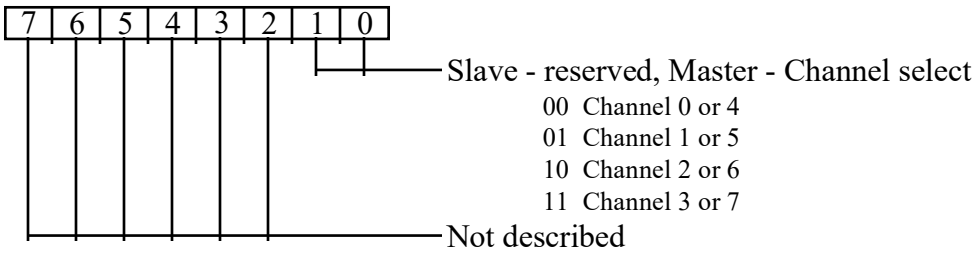
Data bits 0 & 1 of this legacy DMA address indicate which legacy channel to apply the other 6 bits. The DMA Master uses these bits to determine which DMA Slave channel will receive this data. The DMA Master device will handle writes to this legacy address in the special way described at the beginning of this section.

For the DMA Slave, data bits 0 & 1 are considered reserved and will be written **undefined** by the DMA Master. The functionality of the remainder of this register is identical to the legacy DMA controller when applicable.

The remainder of the register contents and functionality are not described here. There are numerous manufacturer's data books that describe the functionality of this register.

3.3.4 Single Channel Mask Register

I/O address	Byte Device	Legacy Address	000Ah
		Slave Address	Base + Fh
	Word Device	Legacy Address	00D4h
		Slave Address	Base + Fh
Size			8 bits
Type			Write only
Power up			00000000b



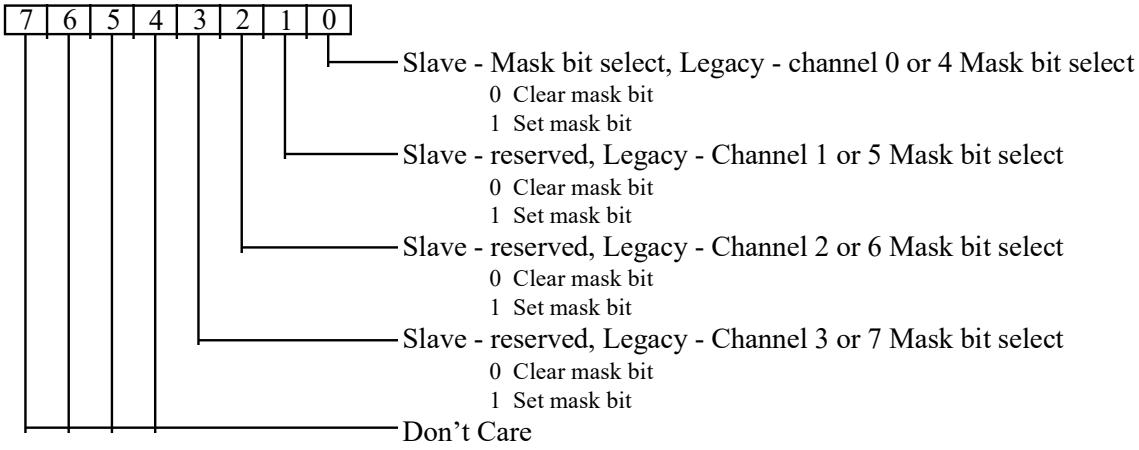
Data bits 0 & 1 of this legacy DMA address indicate which legacy channel to apply the other bit. The DMA Master uses these bits to determine which DMA Slave channel will receive this data. The DMA Master device will handle writes to this legacy address in the special way described at the beginning of this section.

NOTE: The DMA Slave does not have a corresponding single channel Mask register. A write to this legacy address will cause the DMA Master to write to the **Multi-channel Mask Register** (described next) in the specified DMA Slave, with bit 0 carrying the new mask status.

The remainder of the register contents and functionality are not described here. There are numerous manufacturer's data books that describe the functionality of this register.

3.3.5 Multi-Channel Mask Register

I/O address	Byte Device	Legacy Address	000Fh
		Slave Address	Base + Fh
	Word Device	Legacy Address	00DEh
		Slave Address	Base + Fh
Size			8 bits
Type			Write/Read
Power up			00000000b



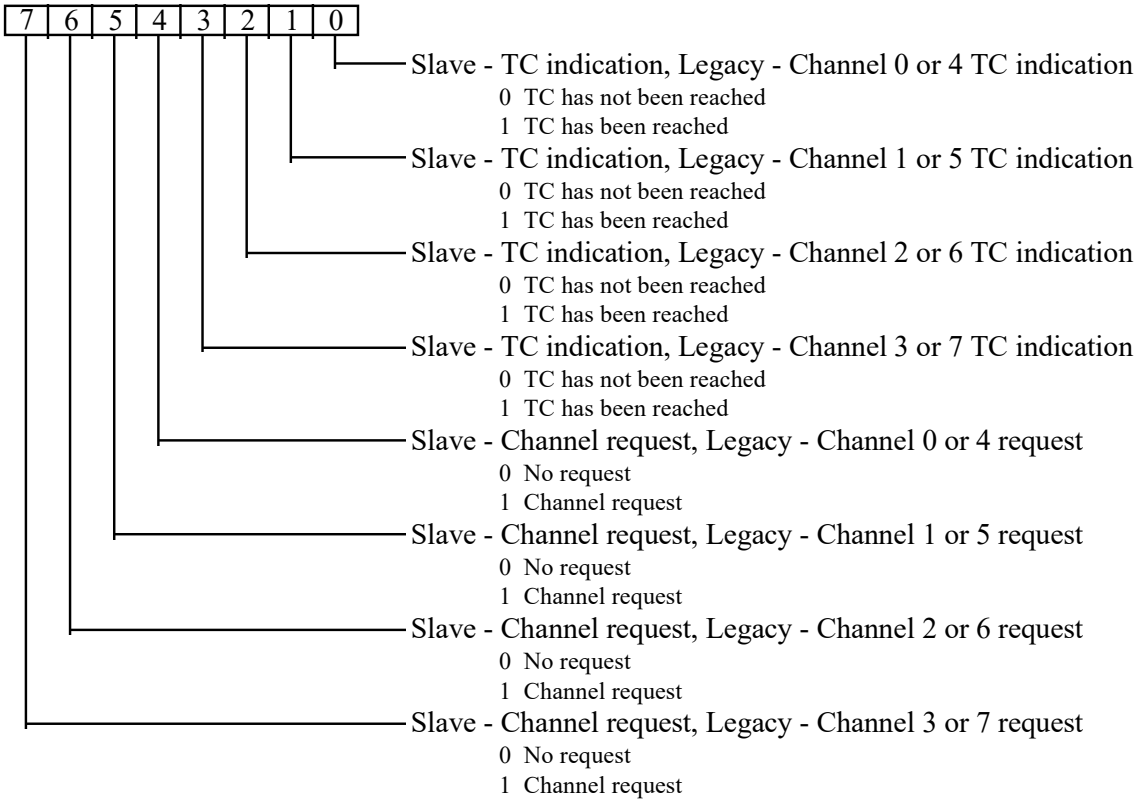
Data bit positions 0 - 3 of this legacy DMA address indicate the legacy channels to apply the data to. The DMA Master uses these bits positions to determine the DMA Slave channels that will receive this data. The DMA Master device will handle writes to this legacy address in the special way described at the beginning of this section. There are 4 I/O slave writes if the legacy address is to the byte DMA, and there are 3 I/O slave writes if the legacy address is to the word DMA.

It is the Master DMA responsibility to remap the Legacy bits for the DMA Slave channel since only bit 0 is valid and the other seven are considered reserved and will be written **undefined**.

The remainder of the register contents and functionality are not described here. There are numerous manufacturer's data books that describe the functionality of this register.

3.3.6 Status Register

I/O address	Byte Device	Legacy Address	0008h
		Slave Address	Base + 8h
	Word Device	Legacy Address	00D0h
		Slave Address	Base + 8h
Size			8 bits
Type			Read only
Power up			XXXX0000b



The DMA Master device will handle reads to this legacy address in the special way described at the beginning of this section. There are 4 I/O slave reads if the legacy address is to the byte DMA, and there are 3 I/O slave reads if the legacy address is to the word DMA. It is the DMA Master's responsibility to properly assemble the contents of this register.

NOTE: The DMA Slave must return the same TC indication on bits 0-3 and the same channel request on bits 4-7.

3.3.7 Temporary Register

Legacy Address	000Dh for byte	00DAh for word
Size	16 bits	
Type	Read only	
Power up	0000h	

The DMA Master will respond to and terminate a PCI I/O read to this legacy address, and will drive the data bits **undefined**.

3.4 DMA Software Commands

3.4.1 Clear First/Last Flip-Flop

I/O address	Byte Device	Legacy Address	000Ch
		Slave Address	N/A
	Word Device	Legacy Address	00D8h
		Slave Address	N/A
Size			1 bit
Type			Write only
Power up			Xb

The act of writing this address clears the first, last Flip-Flop. The data is a don't care. The DMA Master device will handle a write to this legacy address, and keep track of the state of this Flip-Flop. The Slave channels do not need this Flip-Flop.

3.42 Master Clear

I/O address	Byte Device	Legacy Address	000Dh
		Slave Address	Base + Dh
	Word Device	Legacy Address	00DAh
		Slave Address	Base + Dh
Size			0 bits
Type			Write only
Power up			N/A

The act of writing this address performs the same function as a hardware reset. The data is a don't care. The DMA Master device will handle a write to this legacy address in the special way described at the beginning of this section. There are 4 I/O DMA Slave writes if the legacy address is to the byte DMA, and there are 3 I/O DMA Slave writes if the legacy address is to the word DMA.

3.4.3 Clear Mask Register

I/O address	Byte Device	Legacy Address	000Eh
		Slave Address	Base + Fh
	Word Device	Legacy Address	00DCh
		Slave Address	Base + Fh
Size			0 bits
Type			Write only
Power up			N/A

NOTE: A write to this legacy address will cause the DMA Master to write to the **Multi-channel Mask Registers** (described above) of the DMA Slave channel, with bit 0 set to zero. There are 4 I/O DMA Slave channel writes if the legacy address is to the byte DMA, and there are 3 I/O DMA Slave channel writes if the legacy address is to the word DMA.

The act of writing this address enables all 4 channels to accept DMA requests. The data is a don't care. The DMA Master device will handle a write to this register in the special way described at the beginning of this section.

3.5 DMA Base, Count, Memory Page and Extended Addressing Registers

Each legacy DMA channel has two legacy addresses defined to store the base memory address and count information. Located at these byte legacy address are 16 bit registers. The state of the first/last Flip-Flop determines which byte, high or low, is being accessed. The DMA Slave does not suffer this problem. It has fully decoded these registers. The table below shows the relationship between legacy DMA addressing for Base, Count, and Memory Page registers and where this information is programmed into the DMA Slave. For the Byte legacy DMA, bits 0-7 represent address 0-7, however for the Word legacy DMA, bits 0-7 represent address 1-8. This carries forward to the next address byte. The Memory page register realigns the bit position to the address. This relationship is maintained in the DMA Slave. A DMA Slave can be programmed to be in 8/16 bit transfer mode from its PCI configuration space, defined in section 3.32. This mode information, shown below, defines how the DMA Slave treats the data in the registers. The last part of the table defines **optional** Non legacy addressing extensions for the Slave.

Legacy Channel	**Base Address**	**Base Address**	**Memory Page**	**Count Address**	**Count Address**
	Address 0-7 First / Last FF Low	Address 8-15 First / Last FF High	Base address 16-23	Address 0-7 First / Last FF Low	Address 8-15 First / Last FF High
Channel 0	0000h	0000h	0087h	0001h	0001h
Channel 1	0002h	0002h	0083h	0003h	0003h
Channel 2	0004h	0004h	0081h	0005h	0005h
Channel 3	0006h	0006h	0082h	0007h	0007h
	Address 1-8	Address 9-16	Address 17-23	Address 1-8	Address 9-16
Channel 4	00C0h	00C0h	N/A	00C2h	00C2h
Channel 5	00C4h	00C4h	008Bh	00C6h	00C6h
Channel 6	00C8h	00C8h	0089h	00CAh	00CAh
Channel 7	00CCh	00CCh	008Ah	00CEh	00CEh
Channels above map to DMA Slave address	**Base + 0h**	**Base + 1h**	**Base +2h**	**Base + 4h**	**Base + 5h**
8 bit mode	Address 0-7	Address 8-15	Address 16-23	Address 0-7	Address 8-15
16 bit mode	Address 1-8	Address 9-16	Address 17-23	Address 1-8	Address 9-16
Non legacy DMA Slave Addressing Extensions*	**Base Address** **Base + 3h**			**Count Address** **Base + 6h**	
8 bit mode	Address 24-31			Address 16-23	
16 bit mode	Address 24-31			Address 17-23	

***NOTE**: Any DMA Slave that does not support these extensions must always return 00h from these locations when read.

NOTE: It is the responsibility of the DMA Master to support the reserved Memory Page Registers.

The remainder of the register contents are not described here. There are numerous manufacturer's data books that describe the functionality of these registers.

3.6 PCI Special DMA Configuration Register

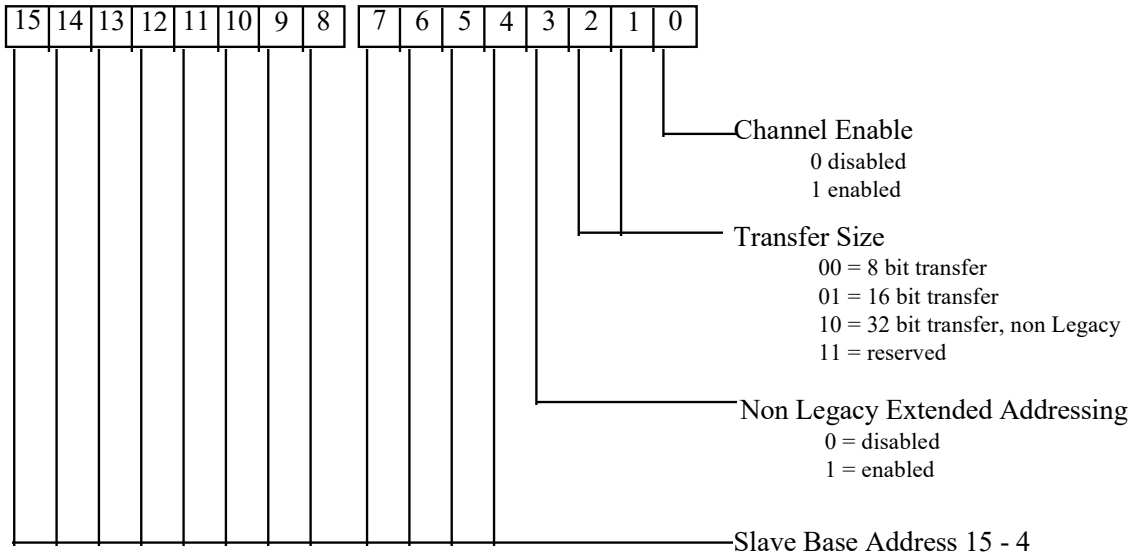
3.6.1 DMA Master Configuration Register(s)

PCI Configuration address	Between 40h-FCh
Size	32 bits or larger
Type	Write / Read
Power up	00000000h

The DMA Master configuration register is not defined in this specification. The requirements of it are however. The DMA Master must have at least one Slave Base Address Configuration Register. If there is only one, then all of the legacy DMA channels will be grouped into a 128 byte block; 16 bytes times 8 channels, even though channel 4 is not a usable channel and could be droped from the block. The 128 byte block is chosen for logical consistency. At the other extreme, if there are seven Slave Base Configuration Registers, then each legacy DMA channel is mappable totally independent from all the others. There must be a Master enable bit and its power up condition is disabled.

3.6.2 DMA Slave Configuration Register

PCI Configuration address	Between 40h-FCh
Size	32 bits
Type	Write / Read
Power up	00000000h



There must be one Slave Configuration Register for each slave channel in a device, with the channel's enable bit. This Channel Enable bit, when disabled, will at a minimum disable the DMA Slave PCI interface from accepting any PCI cycles within the 16 byte range of its programmable base address. The Base Address along with a matching base address in the DMA Master indicates which DMA channel the DMA Slave is mapped to. No two devices in a system should ever be programmed with the same Slave Base Address.

The DMA Slave is only required to support one Transfer Size. If the DMA Slave only supports 8 bit then bits 2 and 1 must always be read 00b. If the DMA Slave supports 8/16 bit only then bit 2 must always be read 0b. If the DMA Slave only supports 16 bit transfers then bits 2 and 1 must be read 01b. And so on.....

The 32 bit mode, if supported, is programmed like 8 bit mode. The count will simply increment or decrement by 4 instead of 1 on each transfer.

Non Legacy Extended Addressing bit, if supported increases both the addressing (Base + 3) and the word count (Base + 6) by a byte, effectively bring the total addressable space to 32 bit and the byte count up to 24 bits. However if this extension is not supported, the DMA Slave channel is required to accept writes to these addresses with reads returning zeros for data.