



EE301:- Analog Circuits Course Project

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Submitted By:-

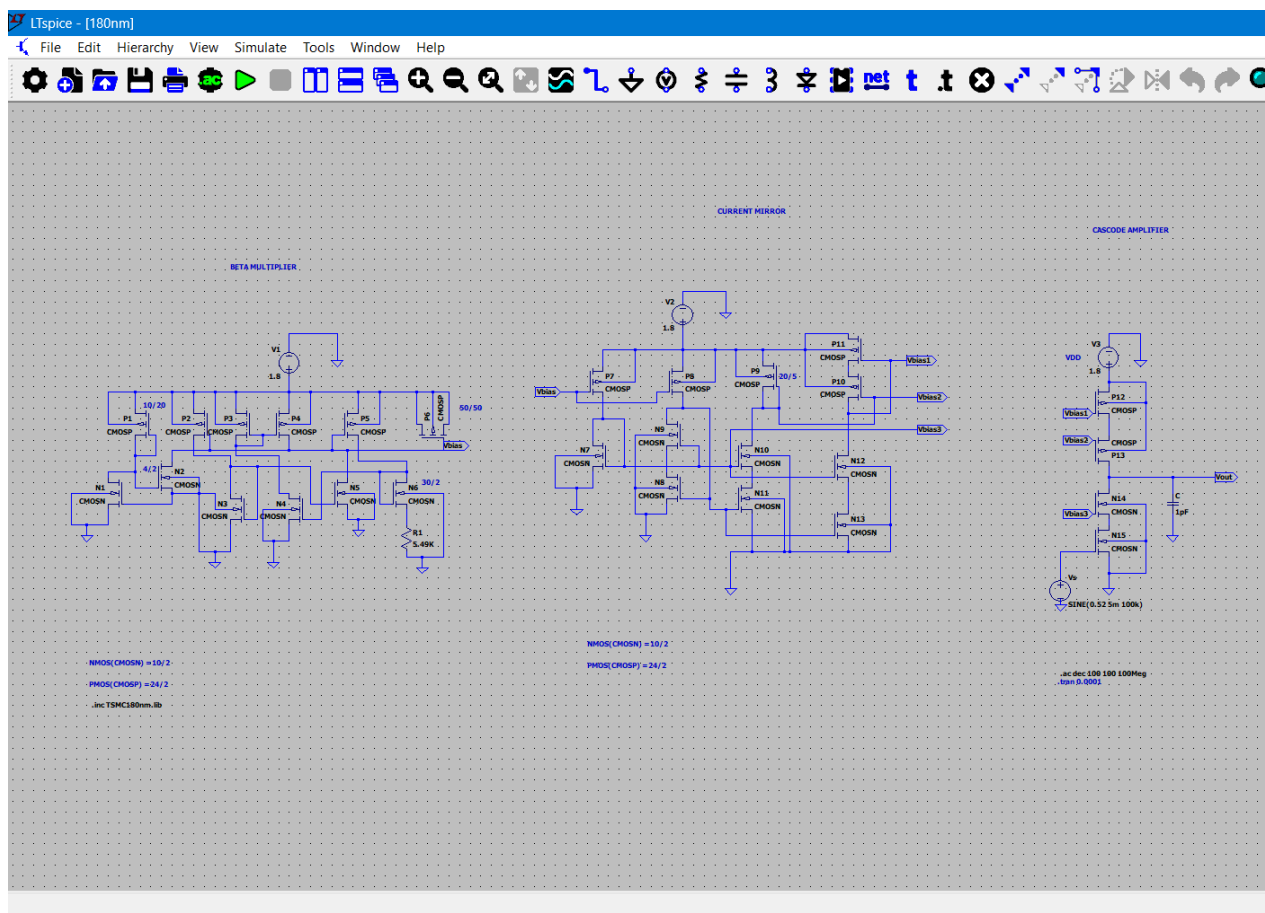
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Objective:-

Design of cascode amplifier and cascode current mirror in schematic and layout using LTspice or Cadence and Magic/Cadence tools in 180 nm (supply 1.8 V) technology and only schematic of cascode amplifier, beta multiplier and cascode current mirror in 22 nm (supply 0.8 V) technology node to see the effect of lowering the technology node.

180nm technology schematics:-



Given specifications to be followed and values obtained from spec file:-

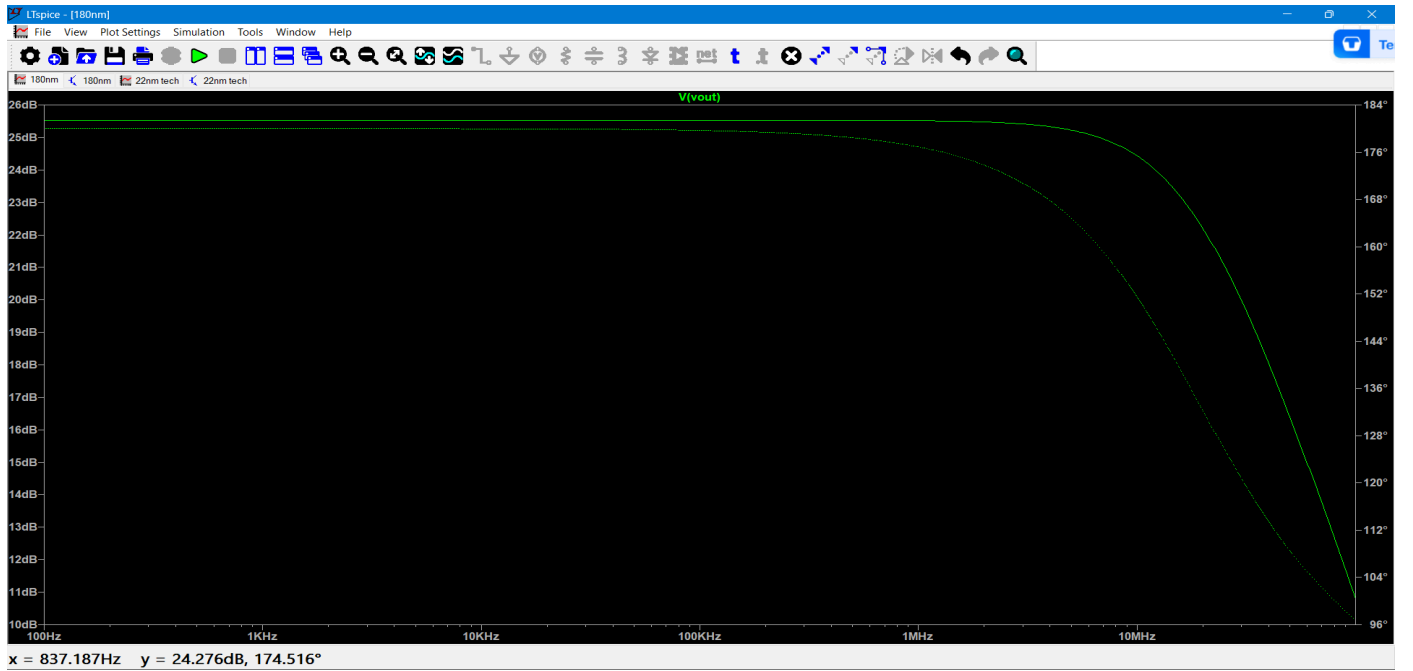
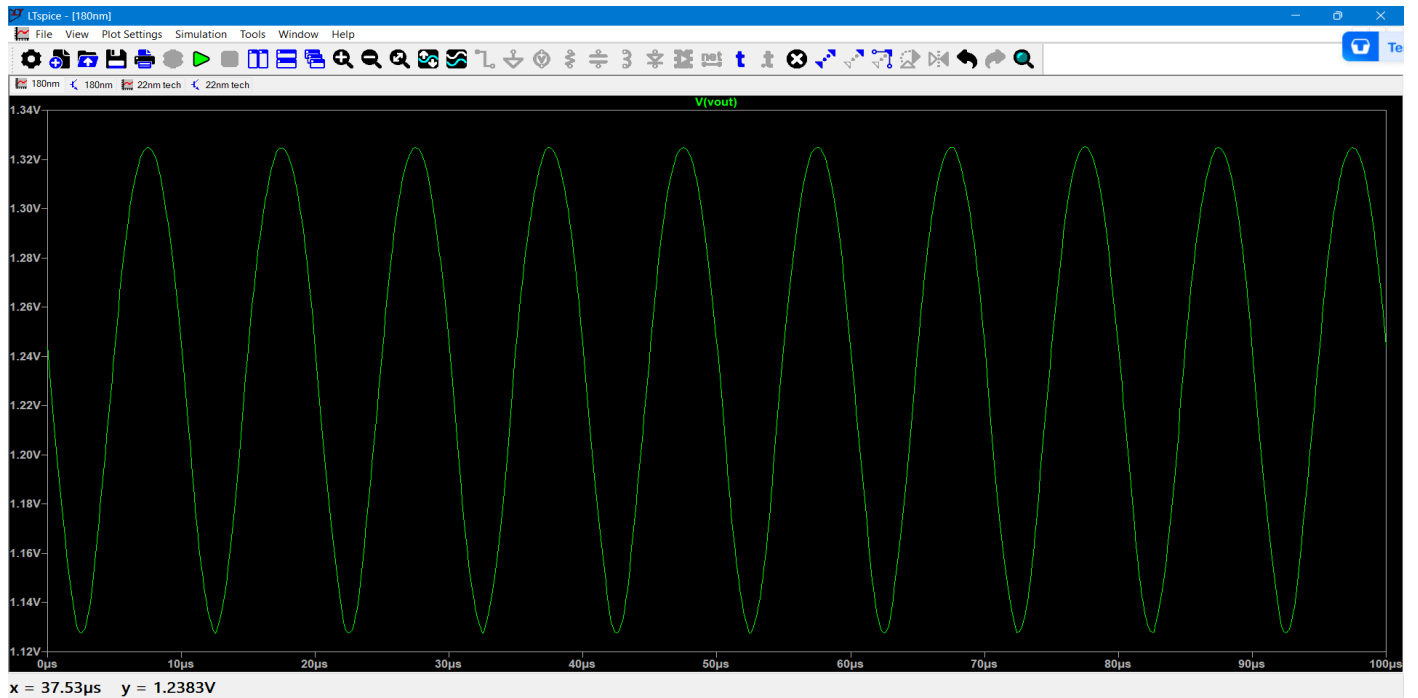
- $V_{DD} = 1.8 \text{ V}$
- $A_v = 20 \text{ V/V} = 26.02 \text{ dB}$
- Power dissipation (P_D) $< 5 \text{ mW}$
- Load Capacitance (C_L) $= 1 \text{ pF}$
- Unity Gain Bandwidth (UGB) $> 500 \text{ KHz}$.
- $V_{th_n} = V_{th_p} = 0.5 \text{ V}$
- $\mu_n C_{ox} = 350.8 \text{ } \mu\text{A/V}^2$
- $\mu_p C_{ox} = 71.2 \text{ } \mu\text{A/V}^2$

Calculations:-

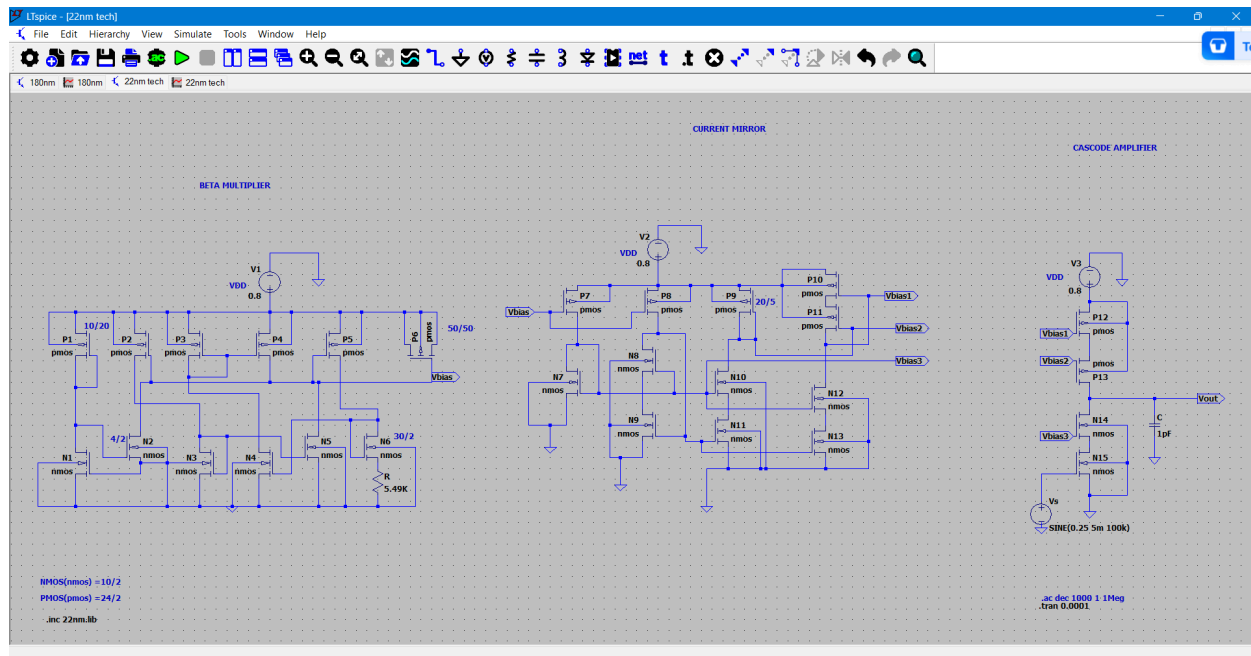
For 180nm tech:-
 → By given 2 specifications we have:-
 $V_{DD} = 1.8 \text{ V}$; $V_{th_n} = V_{th_p} = 0.5 \text{ V}$; $P_D < 5 \text{ mW}$; $A_v = 20 \text{ V/V}$
 $V_{DD} I_{DD} < 5 \text{ mW}$
 $\Rightarrow 1.8 I_{DD} < 5 \text{ mW}$
 $\therefore I_{DD} < 2.78 \text{ mA}$
 Assuming $I_{DD} = 2.5 \text{ mA}$
 → 1st stage on Cascode Amplifier.
 I though each will be equal
 2 @ Saturation:-
 $I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_N [V_{b_{bias1}} - V_{th_n}]^2$
 # For n-MOS :- [MOSFETs(3,4)]
 → From specifications, we have $\mu_n C_{ox} = 350.8 \text{ } \mu\text{A/V}^2$
 $\Rightarrow 350.8 \times 10^{-6} \times \frac{1}{2} \times \left(\frac{W}{L}\right)_N [V_{b_{bias1}} - 0.5]^2 = 2.5 \times 10^{-3}$
 $\Rightarrow \left(\frac{W}{L}\right)_N [V_{b_{bias1}} - 0.5]^2 = 14.25 \text{ --- (i)}$
 # For p-MOS :- [MOSFETs(1,2)] $\rightarrow \mu_p C_{ox} = 71.2 \text{ } \mu\text{A/V}^2$
 $\Rightarrow 71.2 \times 10^{-6} \times \frac{1}{2} \times \left(\frac{W}{L}\right)_P [V_{b_{bias2}} - 0.5]^2 = 2.5$
 $\Rightarrow \left(\frac{W}{L}\right)_P [V_{b_{bias2}} - 0.5]^2 = 35.21 \text{ --- (ii)}$

→ For individual MOSFETs we have,
 $M_3 \rightarrow 14.25 = \left(\frac{W}{L}\right)_N [V_{b_{bias3}} - V_{th_n} - 0.5]^2$
 $M_4 \rightarrow 14.25 = \left(\frac{W}{L}\right)_N [V_{b_{bias4}} - 0.5]^2$
 $\Rightarrow V_{b_{bias3}} = V_{b_{bias4}} = V_3 \text{ --- (iii)}$
 $M_2 \rightarrow 35.21 = \left(\frac{W}{L}\right)_P [V_{b_{bias2}} - V_{th_p} - 0.5]^2$
 $M_1 \rightarrow 35.21 = \left(\frac{W}{L}\right)_P [V_{b_{bias1}} - V_{DD} - 0.5]^2$
 $\Rightarrow V_{b_{bias1}} - V_{DD} = V_{b_{bias2}} - V_{th_p} - 0.5$
 $\therefore V_1 = V_{b_{bias2}} - V_{b_{bias1}} + V_{DD} \text{ --- (iv)}$
 Now, Assuming Equal drops across the PMOS & NMOS
 we have, $V_{DD} - V_1 = V_1 - V_2$ & $V_2 - V_3 = V_3 - 0$
 $V_2 = 2V_1 - V_{DD} \text{ --- (v)}$ & $V_3 = \frac{V_2}{2} \text{ --- (vi)}$
 # through schematic we got:-
 $V_{b_{bias1}} = 0.409 \text{ V}$
 $V_{b_{bias2}} = 0.165 \text{ V}$
 $V_{b_{bias3}} = 1.45 \text{ V}$
 so, putting all values in (iii) - (vi) we got
 $V_1 = 1.556$
 $V_2 = 1.31 \text{ V}$
 $V_3 = 0.656 \text{ V}$
 $V_{b_{bias4}} = 0.734 \text{ V}$
 → Putting all in M1, M4:-
 $\left(\frac{W}{L}\right)_P = 9.846$
 $\left(\frac{W}{L}\right)_N = 104.862$

LTspice Plots - Vout And Gain:-



22nm technology schematics:-



Given specifications to be followed and values obtained from spec file:-

- $V_{DD} = 0.8 \text{ V}$
- $A_V = 20 \text{ V/V} = 26.02 \text{ dB}$
- Power dissipation (P_D) $< 5 \text{ mW}$
- Load Capacitance (C_L) $= 1 \text{ pF}$
- Unity Gain Bandwidth (UGB) $> 500 \text{ KHz}$.
- $V_{th_n} = V_{th_p} = 0.3 \text{ V}$
- $\mu_n C_{ox} = 100 \text{ } \mu\text{A/V}^2$
- $\mu_p C_{ox} = 50 \text{ } \mu\text{A/V}^2$

Calculations:-

For 22nm tech:-

When $V_{DD} = 0.7V$; $V_{thn} = V_{thp} = 0.4V$, $\beta_0 \leq 5mW$; $A_v \geq 10$

$\mu_n C_{ox} = 100 \mu A/V^2$
 $\mu_p C_{ox} = 50 \mu A/V^2$

$I_{D1} V_{DD} \leq 0.5 \times 10^{-3}$
 $\Rightarrow I_{D1} \leq \frac{5}{0.7} \leq 6.95$

$\therefore I_{D1} = 10 \mu A$

n-mos:- $(\omega/L)_N [V_{bias1} - 0.4]^2 = \frac{2I_{D1}}{\mu_n C_{ox}} = \frac{2 \times 10}{100} = 0.2$

p-mos:- $(\omega/L)_P [V_{DD} - V_{bias1}]^2 = \frac{2I_{D1}}{\mu_p C_{ox}} = \frac{2 \times 10}{50} = 0.4$

• $M_1 \rightarrow 0.9 = (\omega/L)_N [V_{bias1} - V_t - 0.4]^2$
 • $M_2 \rightarrow 0.2 = (\omega/L)_N [V_{bias2} - 0.4]^2$
 • $M_3 \rightarrow 0.4 = (\omega/L)_P [V_{bias2} - V_t - 0.4]^2$
 • $M_1 \rightarrow 0.4 = (\omega/L)_P [V_{bias1} - V_{DD} - 0.4]^2$

through Simulations:-

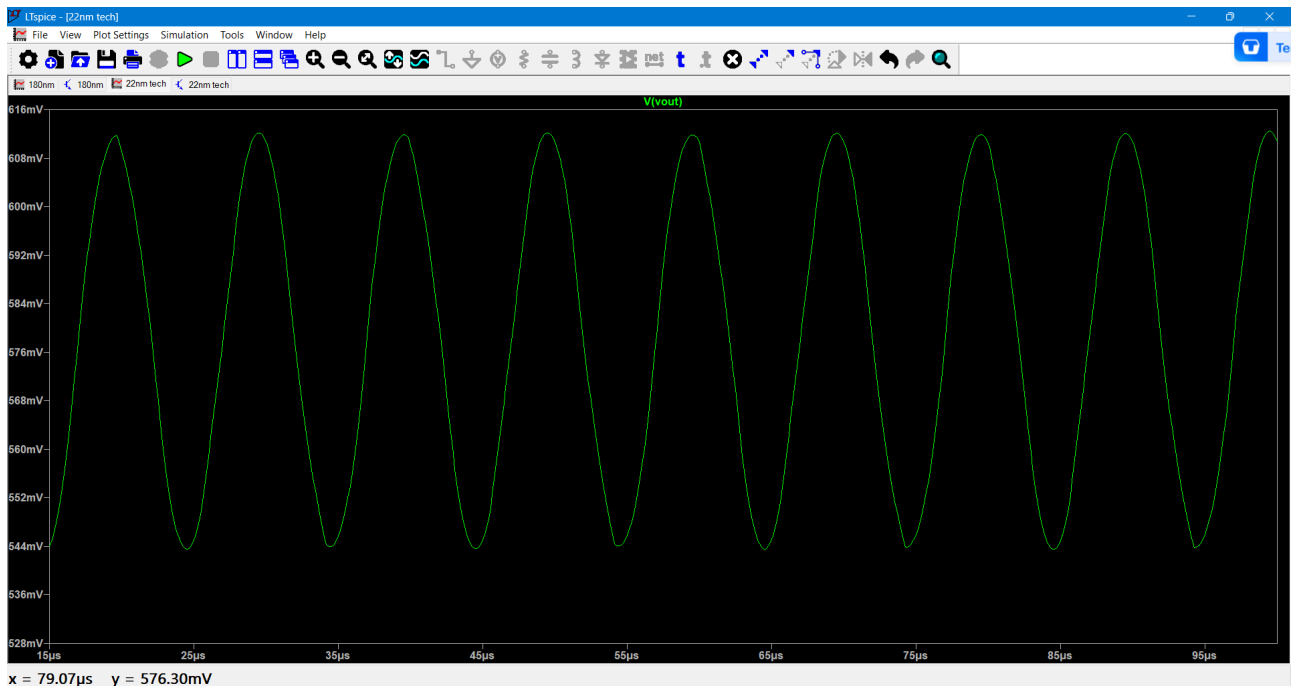
$V_{bias1} = 0.182V$
 $V_{bias2} = 0.068V$
 $V_{bias3} = 0.635V$

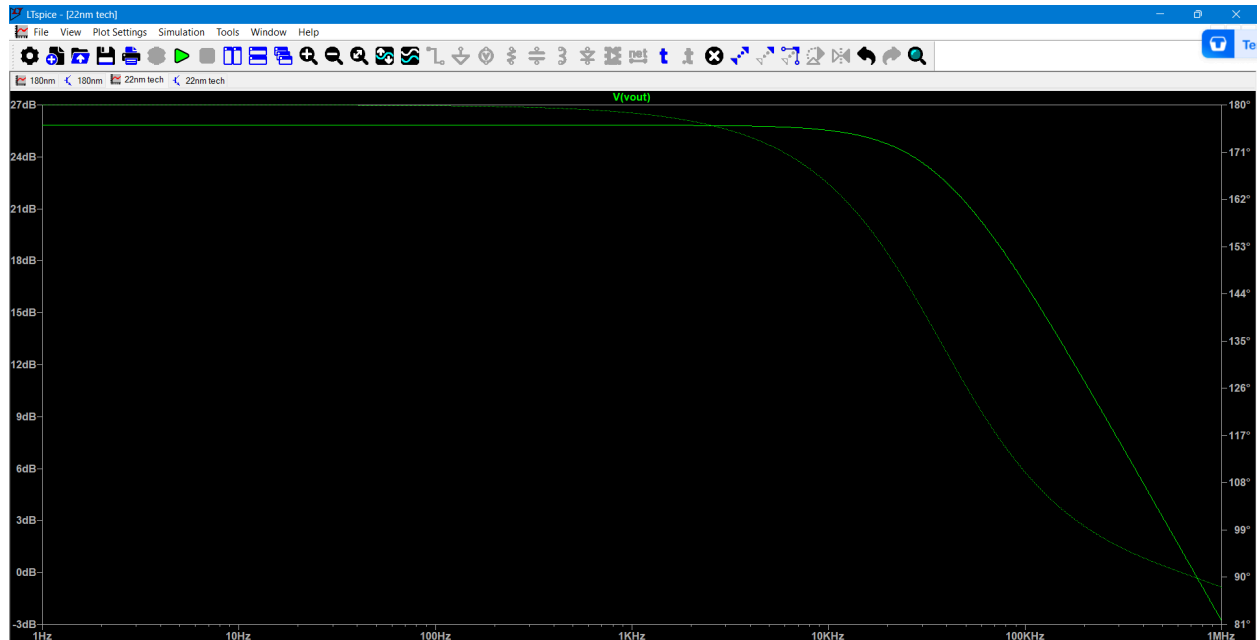
→ Putting in (i) - (vi) & $M_1 - M_4$

$V_1 = 0.686V$
 $V_2 = 0.572V$
 $V_3 = 0.186V$
 $V_{biasing} = 0.304V$

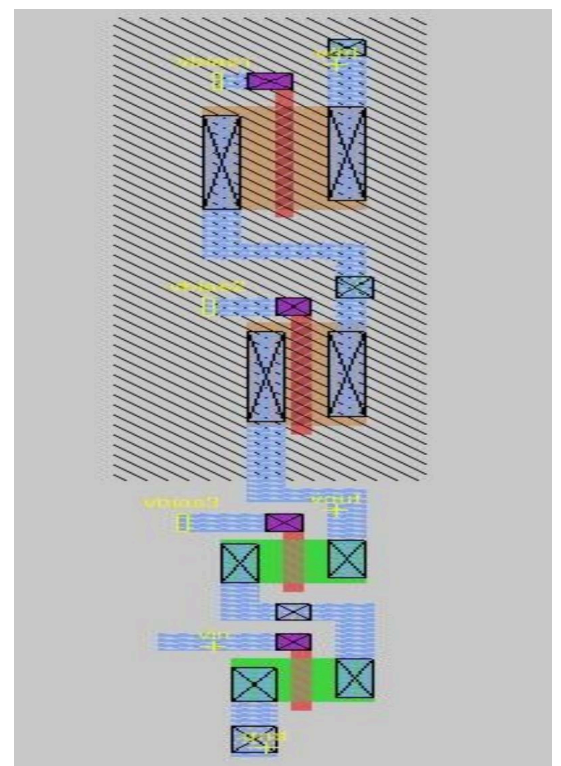
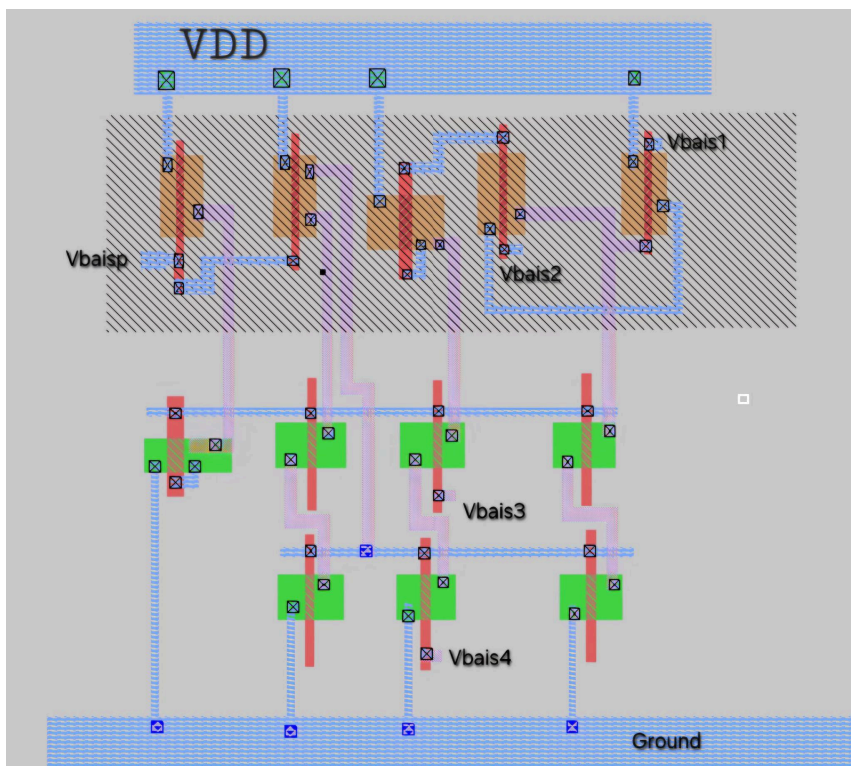
$(\omega/L)_N = 76.89$
 $(\omega/L)_P = 0.235$

LTspice Vout and Gain plots:-





180nm Magic Layout:-



Results:-

Add tabulated results(calculated and practical) for both technologies containing values of all specified parameters. Results from ngspice simulations should be included as well.

Observations:-

- All simulated results thus obtained are under specified performance limits for both the technologies.
- Biasing voltages for 180nm technology are greater than 22nm technology.
- Unity Gain Bandwidth for 180nm = 2MHz
- Unity Gain Bandwidth for 22nm = 350MHz
- Both technology's gain plots show that the given systems are low pass filters.

Conclusions:-

We conducted simulations of the Beta Multiplier, Cascode Current Mirror, and Cascode Amplifier circuits in LTspice for both 180nm and 22nm technology nodes. The simulated results closely matched theoretical expectations and met the necessary performance specifications. Additionally, we designed the layout for the Cascode Current Mirror and Cascode Amplifier in Magic software, for the 180nm technology. Finally, we analyzed and compared the results from both 180nm and 22nm technologies based on LTspice simulations and the layout design in Magic (only for 180nm technology).