Ozayr Raazi

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Education

University of Waterloo Sept. 2022 – April 2027
Honours Computer Engineering *Waterloo, ON*

Skills

Languages: C, C++, Python, SystemVerilog, ARMv7 Assembly, VHDL, Bash
PCB/Embedded: Cadence OrCAD X, KiCAD, STM32, Arduino, DediProg, Fusion Digital Power, PowIRCenter
Protocols: I2C, PMBus, Segment-Routing, MPLS, L2VPN
Other: AMD Vivado, GDB/LLDB, Logisim, Quartus Prime, OpenOCD, Git, Linux, Windows, macOS

Experience

Untether AI Jan. 2025 – April 2025
Hardware Engineer (Co-op) *Toronto, ON*

- Designed 4-layer evaluation **Printed Circuit Board** from scratch using Cadence OrCAD X, including component research, schematic diagram, and layout, enabling testing of new Power-Management ICs
- Verified functionality of **40+** AI Accelerator Cards by conducting physical inspections, short checks, performance benchmarks, and neural network correctness tests, while ensuring power/thermal compliance
- Reduced current sensing IC's error to $<$**1%** by sweeping configuration registers and comparing current values measured via **STM32** to adjustable current load's readout, simulating an active board

Untether AI May 2024 – Aug. 2024
Firmware Engineer (Co-op) *Toronto, ON*

- Developed firmware for an **AI Accelerator Card** (PCIe Gen5 x16), enabling key features such as power sequencing, temperature sensing, power monitoring, and fan control, using the **I2C** and **PMBus** protocols
- Brought-up first batch of cards by writing firmware, conducting hardware checks, flashing PMICs, power sequencers and ASICs, and debugging issues, achieving fully booted cards in **under 3 days**
- Researched and proposed switching a voltage rail from single-phase to dual-phase, potentially reducing power loss by **46%** and increasing efficiency by **10%**

Ciena Sept. 2023 – Dec. 2023
Embedded Software Engineer (Co-op) *Ottawa, ON*

- Accelerated iteration and testing of a Segment-Routing module by developing an **event-based** client for simple user interfacing and by configuring CMAKE to enable independent compilation
- Improved error-detection of a TCP-transport library by creating **C++ GoogleTest** unit tests, allowing for send and receive functionalities to be tested concurrently using **multi-threading**
- Increased thread safety of **C code** and protected internal data structures by converting APIs to signal-based

Projects

Biro-1 | *KiCAD, C++, Project Management* Feb. 2025 – Present

- Ideated and planned a fully-custom **media controller device** to address a real-world need of keyboard not having hardware media keys, and created a team of 5 people to help realize the project
- Defined **product requirements**, set timelines, organized subsystems, and created high-level tasks for delegation among team members
- Researched components, designed block and schematic diagrams, and started layout for **prototype board**, while assisting in firmware and RTOS development

MVM Engine + Tanh Circuit | *SystemVerilog, AMD Vivado* July 2025

- Implemented a **Matrix-Vector Multiplication** engine from Microsoft's Project Brainwave deep learning accelerator by designing a pipelined dot-product module, accumulator module, and control FSM
- Built a fully pipelined circuit that calculates the Taylor approximation of the hyperbolic tangent function, used for neural network activation, and optimized it to run at **561MHz** on a Pynq-Z1 FPGA using **DSP48E1** blocks